International Journal of Future Generation Communication and Networking
Vol. 13, No. 1, (2020), pp.732 -744

Turbo Decoder for LTE High Speed band Efficient Architecture

Rashmi R*, Manju Devi**
**Asst Professor, Department of Electronics and Communication Engineering, Vemana Institute of Technology , affiliated to Visvesvaraya Technological University, Belagavi, Karnataka, India*
*** Professor,H o D, Department of Electronics and commutation Engineering, The Oxford College of engineering, affiliated to Visvesvaraya Technological University, Belagavi, Karnataka, India*

Abstract

The evolution of wireless communications for the next generation is well beyond 3 Gbps of wireless communication standards. Hence, reliable data communication is possible because of Wireless communication system. Turbo codes that is used by the Channel decoder delivers good bit rate performance and also performs error-correction, making the code widely acceptable by numerous wireless communication standard. Wireless communication that is 3G and 4G includes turbo codes within it for accurate error correction. The turbo decoder is restricted by the inherent iterative process to compile the data at a higher rate. Bit error rate (BER) is calculated depending on the size of the frame and the interleaver type that is required in the implementation of encoder and decoder. A coding loss of around 0.2 dB is exhibited by the decoder while comparing BER performance with simulated BER values. High decoding latency is the major flaw of Turbo coding implementation. The three major obstacles faced in turbo coding architecture are: The forward recursions or recursions occurring backward in maximum a posteriori (MAP) decoder, the repetitive nature of the decoding algorithm and interleaver or de-interleaver units between the MAP decoders. The above-mentioned obstacles are of utmost importance when we integrate the codes written using turbo coding in a communication standard of throughput which is high like LTE. To predict latency reduction and parallelization methods in the implementation of hardware components of Turbo decoder, we fulfill the data rates mentioned above. A serial data dependency imposed is the problem of decoding a received signal. The severe bottleneck is created conventional turbo decoder by the limited processing throughput of the.

Keywords-*wireless communication; 5G communication; FEC - Forward Error Correcting channel Coding; Turbo Codes; LTE - Long Term Evolution; Cellular Technology*

I. THE NEED FOR TURBO CODES

The easy accessibility of unwired technology has altered the way the world communicates today. Technologies like cellular and others makes it possible for individuals to be connected to others around the globe from anywhere, at any time. Every wireless network requires transmission of information quickly and timely, at a high rate accurately. To ensure that there is optimal accuracy or for recovering the unaltered signal at the receiver's end, there has been implementation of forward error correction. There are various categories of techniques for error correction that can be used like convolution method of coding. However, this method does not succeed in maintaining the signal's lower bound values to the noise ratio with the increase in code length. To overcome this, turbo coding which is a latter version of coding, was introduced which helps in achieving performance levels which is closer to theoretical bounds compared to the conventional coding systems.

ISSN: 2233-7857 IJFGCN

One of the most proficient type of Forward Error-Correcting channel type of coding is Turbo coding. With the rise in systems of communication done digitally, there is a need for rectification of errors. This issue arises because of the non-idealistic nature of realistic channels for communication, often with disturbance caused due to noise. To reimburse for the errors that get produced by this noise, there is a requirement for error correction. An effective solution is forward error channel coding. The reason turbo code is widely accepted in wireless network of communication that are wireless in nature is the power over other correction codes. The turbo encoder and decoder are a recent progress done in the area of forward error correction (FEC) codes that is useful in the achievement of Shannon-limit performance. This encoder and decoder fulfill the requirement of high throughput in Wimax/LTE network by providing a relatively good performance. The key feature of these turbo codes is decoding algorithms which improves BER performance of wireless networks. To achieve optimized performance, we then will have to find the best option of turbo codes.

There is no need for a back-channel hence avoiding retransmission of data which can be an advantage of forward error correction. Hence where retransmitting can be relatively impossible to be done or costly, FEC is applied. The coding scheme for Long Term Evolution (LTE) Turbo coding. Some of the characteristic features of turbo codes are its repetitive decoding mechanism, reoccurring systematic encoders and also the use of interleavers. This paper presents the structure of turbo encoder and decoder and its respective operations. The above-mentioned operations are further defined by various techniques. An integral part of wireless communication system is a channel decoder which is responsible for communication of data that is reliable in nature. A decoder for channel employing turbo codes for correction of errors produces bit-error-rate performance that can be excellent which makes various wireless communication standards accept this code [1]. Peak data-rates of standards of 3G and 4G communication wireless in nature which include turbo codes for the correction of errors are shown in Fig. 1

These components must be created which in turn must incorporate the criteria that can be applicable.

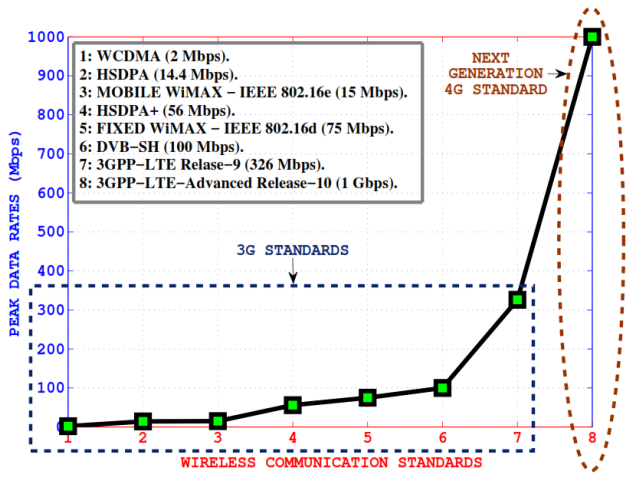

Fig 1: Ever increasing peak data rates of various wireless communication standards which include turbo code as their error.

II. RELATED WORKS

Lekha S. Yeldi, Jagdish D. Kene et al [1], proposed the key features of turbo coding method are the algorithms for decoding which improve the wireless network's BER performance. To have an optimized performance, the paper attempts to find the best possible option that exists of turbo code. The simulation results that are produced that of the BER performance of that of log map and of max-log

ISSN: 2233-7857 IJFGCN

Map show that these maps of log functions scans be implemented much easily thereby giving a bit error rate which has low SNR, desired in nature. This also reduces additional complexity by performing with lesser number of states. The paper also shows the results produced in Log-Map which has different quantized levels and values of that of forward, backward and branch metric. Log MAP best suits the decoding algorithm with low bit error rate in comparison to max-log map and MAP.

Prabhavathi D Bahirgonde, S K Dixit et al [2], presented that the extremely challenging task is to reduce the complexity produced in computation of Turbo decoding implementation in 3GPP-LTE that is wireless communication standard. The difficulty in execution of a turbo encoder is much lesser than the complexity in that of turbo decoder. This difficulty of Turbo decoder depends on decoding algorithm. The performance degrades with less complexity in decoding. The number of iterations also influences Turbo decoder performance during decoding. Different types of iterative Turbo decoding algorithm are described in this paper. Discussion is done about the factor of correction and how it changes when in different algorithms. Different Turbo decoding algorithms go through BER. MATLAB simulation is used to show how the number of iterations has an effect on Max-Log-MAP decoding. A good method of testing the performance of coding using Turbo code is BER analysis. The number of parameters can be used to test the performance over using hardware of Turbo decoder, the BER analysis becomes difficult to carry. A simulation tool used for performing BER analysis is MATLAB. BER analysis can also be used for algorithms for decoding, the number of interactions and the frame size is carried out in this paper.

Yogesh Beeharry, Tulsi Pawanfowdur, Krishnaraj M. S. Soyjaudah et al [3], proposed that between two concatenated decoders, Turbo codes affect a mechanism for message passing which is iterative. Code Division and Long-Term Evolution for Multiple Access 2000 are some of the communication standards in which there is their widespread adoption due to their astounding performance. When there is usage of Sign Difference Ratio, it has been observed that as there is increase in Eb/N0, the decoding methods' complexity decreases strikingly. Moreover, assessment of Bit Error Rate performance of these methods was also compared for multiple schemes of modulation. These results show that performance differs when varying methods are applied in the waterfall and in the error-floor regions with multiple schemes of variation. Moreover, it is also seen that the Method 2 needs less overall computation steps when compared to those in Methods 1 and 3 in the computational complexity analysis. When considering Binary LTE Turbo codes with BPSK, Binary LTE Turbo with Q-PSK and Binary LTE Turbo of 16-QAM, three varying methods of decoding have been shown. These methods have performance which is similar in general Eb⁄N0range, with BPSK modulation. With QPSK modulation, it is seen that these methods have extremely similar performance over Eb⁄N0 range. Gaining 0.1dB avg. when considering the range Eb⁄N0 > 2.4 dB, the method 2 and method 3 perform better than method 1, with 16-QAM.

Zhongfeng Wang, Zhipei Chi, Keshab K. Parhi et al [4], presented that the decoding done by turbo decoder have throughput which is low and large decoding inactivity due to decoding iteratively. Decoding schemes that are high speed in nature must be used to increase this low throughput and to reduce the value of latency. Comparison on the number of units of computation, the general inactivity in decoding and storage requirement is also mentioned in this paper for different decoding schemes which have different parallelism levels. For the implementation of very high level parallelism, an attractive solution are Hybrid parallel decoding schemes. While some overhead must be paid when it comes to power and area, Turbo decoders which employ these decoding schemes are presumed to gain multiple times the value of throughput of a serial decoding decoder. Simulation results have shown that performance degradations do not occur when considering decoding schemes that are parallel and area-efficient.

ISSN: 2233-7857 IJFGCN

Rahul Shrestha, Roy P. Paily et al [5], focused their work on the design aspect concerning the VLSI of maximum *a posteriori* (MAP) probability decoders that are high-speed in nature which are also are intrinsic building-blocks of parallel turbo decoders. For the computation of backward state metrics, the paper has presented a non-grouped backward recursion technique for the algorithm used in MAP decoders which is logarithmic-Bahl–Cocke–Jelinek–Raviv (LBCJR). To achieve higher clock frequency, based on this technique, MAP decoder can be extensively pipelined and retimed which is unlike such conventional decoder architectures. Additionally, in the state metric normalization technique, there has been reduction critical with 8 and 64 parallel MAP decoders in 90nm CMOS technology, which is employed in designing an add-compare-select-unit (ACSU). An achievement of maximum throughput of the rate 439 Mbps with 0.11 nJ/bit/iteration energy-efficiency was received in an 8-parallel turbo-decoder with VLSI implementation. Similarly, maximum throughput of 3.3 Gbps was achieved in 64 parallel turbo-decoder which has an energy-efficiency of 0.079 nJ/bit/iteration. 3GPP-LTE's peak data-rates and that of LTE-Advanced standards have been met by these high - throughput decoders.

Ardimas Andi Purwita, Arnaud Setio, Trio Adiono et al [6], presented that coding using Turbo code is able to closely reach Shannon limits' channel capacity which is also a high-performance channel coding. A new architecture of encoder based on Turbo coding which is based on 3GPP standard is also mentioned in the paper. By the implementation of dual RAM in internal interleaver, with an optimized parallel architecture that has 8-level, this architecture is developed. To simulate the system and to profile the system, the paper also uses MATLAB software which ensures functionality of the algorithm being proposed and even the architecture. To increase hardware implementation performances of system, compare the performance between un-optimized, un-parallelized, and an optimized encoder of turbo coding which is 8 level. Parallel processing architecture is employed in the algorithm defined to improve inactivity of the clock and to reduce the encoders' size. In order to reduce clock latency, double RAM has also been implemented in internal interleaver of the type turbo coding, When compared to conventional architecture with size smaller than 50%, this proposed architecture increases the efficiency of the encoder by increasing its' speed by 16 times.

Liang Li, Robert G. Maunder, Bashir M. Al-Hashimi, Lajos Hanzo et al [7], recently they have considered turbo codes for the application of wireless communication that can be restrained by energy, as turbo codes help in low energy consumption when it comes to transmission. Here, the usage of magnitude which is a few gates lesser than the architectures of latest LUT-Log-BCJR, which further facilitates a reduction in the consumption of energy by 71%, 71% lower of 0.4 nJ/bit/iteration in this architecture is demonstrated.

Cristian Anghel, Constantin Paleologu et al [8], presents that advantage was taken of the quadratic permutation polynomial (QPP) interleaver proprieties and also when a few of the characteristics of FPGA block memory were considered, a simplified parallel decoding architecture are proposed in this paper. When high decoding latency is introduced by the serial decoding, it should be especially used for large data blocks. N, that is the parallelization factor is usually in the powers of two, 8 is the maximum considered value. The serial decoding latency is N times greater than the received parallel decoding latency. Only one interleaver is used with the cost of very low latency added to proposed parallel architecture, independent of N's value. The serial wise implemented turbo decoder architecture was implemented and developed in a methodical manner, which especially is done from the view of the interleave or the deinterleaver. To make sure the interleaver process works effectively when implemented other than in the process of a decoder especially, the interleaver memory ILM was introduced. The data fed as input together with ILM was typed, whereas the block predecessor to the current block was still decoding. Using this method, the architecture shifted to parallel wise by the use of concatenated values only when in similar memory locations.

ISSN: 2233-7857 IJFGCN

Lohith Kumar H G, Manjunatha K N, Suma M S, C K Raju, Prof. Cyril Prasanna Raj P. et al [9], presented in the paper for a turbo decoder that is 3GPP advanced by the use of an interleaver convolutional in nature, proposed to design and to develop VLSI architecture that is efficient in nature. This advanced Turbo code needs implementation of turbo decoder to produce high throughput. The main obstacle to the decoder implementation is an interleaver and the introduction of latency which arises due to the collisions that occur during memory access. This paper also places a proposition of a Soft Input Soft Output (SISO) turbo decoder which has low complexity for the architecture of memory which thereby enables the decoding to achieve least latency. Trade-offs that occur in design in terms of throughput efficiency and area are then explored to find the architecture optimal in nature. Simulink is used to model the proposed Turbo decoder; and to estimate the performances various test cases are used. The Bit Error Rate (BER) and Turbo decoder and channel specifications are analysed for the rate of 3 samples which is 0.000254 which is of the order of (10-3).

Guohui Wang, Aida Vosoughi, HaoShen, Joseph R. Cavallaro, and Yuanbin Guo et al [10], present that there is a need for parallel architecture to produce a high throughput using a decoder; this can be implemented to meet the requirements of the data rate of the communication systems that are wireless in nature. However, the major challenge that causes the desired interleaver designs' throughput to become unachievable is due to conflict in memory. Furthermore, the hardware for generation of parallel interleaving address becomes difficult to execute because of the increasing complexity of the interleaver algorithm. An interleaver architecture that is parallel in nature and can generate multiple addresses of interleaving is proposed in this paper. A scheduling scheme is proposed which has better and efficient buffer structures that can be used to get rid of contention of memory. The produced results show that with new scheduling scheme, proposed architecture can reduce complexity in hardware and usage of memory significantly. Great flexibility along with scalability can be shown in proposed architecture.

Samir Jasim Mohammed, Ansam Abbas Obaid et al [11], proposed that after many decoder types have been introduced which include multiple parameters, with work design and implementation of turbo code, obtain the Ber for each of the cases, and comparing the results. To study each of the parameters' effect on the turbo codes' performance, multiple parameters have been described that give the desired result of these codes. The UMTS interleaver and the BPSK modulation are assumed for the proposed system. After that, changing many parameters, many types of decoders were done from this work and the results conclude that BER decrease for the same and the performance improves when the number of iteration increased the. The increase in length of code and number of frames improves the performance, different code length applied (256,512,1024 and 4096) and number of frame (512 and 1024) were performed and comparison was done between the results obtained for each case. The results of the SOVA and MAX-Log-MAP is in comparison worse than other types of decoding techniques applied (SOVA, Log-MAP and MAX-Log-MAP) by using log–MAP technique when applied for the same conditions of the system (512 b/f, 1024 f, 4 iterations and), also the gain is obtained about in log-MAP compare with SOVA and in log-MAP comparison with MAX-Log-MAP. To increase the rate of the system, puncturing technique was used, but the BER degrades by increasing the rate. Also the generator polynomial of the system was changed and compared with the standard generator polynomial, where two addition generators polynomials are used, finally two types of channel used in this simulation obtained results for each case and comparison as done when using AWGN channel the performance is best than the fading channel.

Christoph Studer, Christian Benkeser et al [12], proposed the use of turbo decoding for 3GPP LTE standard for communication that occurs in wireless way is a challenging task when considering consumption of power and complexity in computation of the related cellular devices. The implementation aspect of the turbo decoders occurring parallelly that cross 326.4 Mb/s LTE peak data-

ISSN: 2233-7857 IJFGCN

rate using various Soft Input Soft Output decoders that work parallelly are also researched in this paper. When a more realistic 100 Mb/s LTE milestone is considered that is required by the industry today, the decoder implementing turbo code only consumes 69 mW. On analysing the throughput/area trade-offs that are usually associated with the parallelly implemented turbo decoders, it is noticed that in the combination of radix-4 and instances of eight M-BCJR are needed to reach maximum data rate of 0.13 μm in LTE in CMOS technology. There was achievement of parallel access and access of interleaving to memory spaces with high throughput by developing master-slave Batcher network. Optimizing the radix-4 M-BCJR unit has caused to reach a performance higher and lesser area of architecture of turbo decoder ; including the setting record in the throughput achieved which are both ultralow-power and cost effective in implementation.

Prabhavati D. Bahirgonde, Shantanu K. Dixit et al [14], implemented trellis of 8 state which is of the form of radix-2 and the radix-4 form. When considering a system that is practical, the foremost MAP algorithm is much more difficult to implement. To calculate LLR values, all the branch metrics required are stored in a RAM. There is implementation of the Max function to increase the performance with the correction factor. The algorithm defined when implemented is similar to the max. function. While there is increase in the need for various rates of data and services that come with system of communication re-configurability becomes necessary. Constant Log-MAP algorithm is proposed to use the MAP algorithm in the domain of log, and this produces result that are extremely similar to those produced by max Log-MAP algorithm.

Shivshankar Mishra et al [15] presents a paper that implements Turbo encoding algorithm, where two parallel concatenated RSC codes are used to design 1/3 rate encoder. MAX-LOG-MAP algorithm is used for decoding along with Turbo, results of simulation were obtained as expected at the side of the receiver. The paper also analyzes and simulates the mentioned algorithm and the observation was made with the increase in number of iterations, the BER gets better. This performance of BER depends on even the type of interleaver and the size of the frame that has been used for implementing decoder and encoder.

Cristin Anghel et al [16] proposed with the use of decoding architecture that is parallel in nature, the main methods used for sorting is turbo codes that are used in LTE systems. Mostly, the number of required interleavers is represented by the parallelization factor N. The paper proposes an architecture of a decoder which has a single Quadratic Permutation Polynomial (QPP) interleaver. On same memory location, every interleaved address is then placed as a result of the properties of algebraic QPP interleaver. But there must be sorting to be performed before the correct should be sent to each of the decoder unit. Comparison is done for all the methods of sorting to find the one that suits implementation of Field Programmable Gate Array (FPGA) mostly.

III. OBJECTVIES OF THE RESEARCH WORK

A. Need for the Research Problem

A major drawback of implementation of turbo code is its high inactivity in the decoding. There are three important issues which are presented in architectures of turbo codes : the recursions that take place both in forward and backward direction in the maximum a posteriori (MAP) decoders in this repetitive process, the repeating nature of the algorithm for decoding, and the interleaver and the deinterleaver units that are present between the MAP decoders. When there is integration of turbo in the codes of high throughput standard of communication like LTE, these above mentioned challenged become important. To fulfill the rate of data that is mentioned, there must be foretelling of parallelization and reduction in inactivity techniques in turbo decoders' implementation of hardware. A serial data dependency is imposed to overcome the problem of decoding received signal; a severe

ISSN: 2233-7857 IJFGCN

bottleneck is imposed by limiting the throughput of procession of the standard implementation of the turbo decoder upon the general throughput of the schemes of communication in real-time.

- Decoding algorithm
- Signal to noise ratio (Eb/No)
- BER
- Frame size
- Puncture/un-puncture
- Maximum iterations
- Number of errors in the frame that need to be terminated

B. Primary Objective

The primary objectives of this proposed research work are to develop efficient Turbo Decoder Architecture when considering the throughput of processing, the inactivity of processing, the energy consumed by each frame and normalized core area. Another objective is for reviewing literature on Turbo Decoder Architecture in LTE communication based on BER. This objective also focuses on validation of effective Turbo Decoder Architecture when con considering processing of the throughput, the latency's processing, consumption of energy in every area along with normalized core region. This primary objective includes evaluation of efficiency of Turbo Decoder Architecture when considering the throughput processed, procession of latency, energy taken by the individual frames with the normalized care but definitely not limited to these above-mentioned objectives.

IV. RESEARCH CONDUCTED

This section discusses about the work carried out till date. The entire work is classified into Preliminary Review, Research methodology, and Possible Outcomes.

A. Preliminary Review

The preliminary research phase is the phase where the motive was to investigate the existing issues that are associated with turbo decoder's performance analysis and to propose areas in which the execution of the turbo decoder may be further upgraded by in turn improving BER performance of wireless networks, by ensuring balance in the network and for obtaining better performance for turbo decoders.

The study outcome of the preliminary phase of research performed is published in a review paper titled "*Evolution of Wireless Communication Along with Encoders".* In "International Journal of Innovative technology and Exploring Engineering (IJITEE)", the paper is published.

B. Research Methodology

The methodologies adopted by the proposed system are as listed below:

- Conduction of literature surveys on different Architectures of Decoders implemented using Turbo Coding in LTE Communication (as per BER) and then will be carried out from IEEE papers, white papers and journals.
- Development of efficient architecture of turbo decoder for wireless LTE communication standards must also be carried out.
- Literature survey on LTE Communication and challenges that can be faced in LTE Communication (asper BER) must be carried out from different IEEE papers, white papers and journals.
- Validation of efficient Turbo Decoder Architecture when considering processing latency, processing throughput, energy consumption for each frame and area of the core that is normalized will be carried out.

ISSN: 2233-7857 IJFGCN

- Evaluating and optimization the Turbo Decoder Architecture when considering to process the throughput, the latency, and the consumption of energy by each and normalized core area must also be carried out.

C. Possible Outcomes

In all wireless telecommunications systems, the channel coding procedure which is also known as Forward Error Coding (FEC), is used in such a way to identify and also correct any potential errors which may occur during radio transmission the constituent encoder and the interleaver are the main components of a turbo code. Turbo codes are used in Long Term Evolution (LTE) systems and Universal Mobile Telecommunications Systems (UMTS), respectively. Parallel decoding architectures are considered to solve this problem.

We propose an architecture that are decoding in nature with just a single Quadratic Permutation Polynomial (QPP) interleaver. On the same memory location, every address interleaved are placed as a result of algebraic properties of QPP interleaver, but this needs the data to be sorted before the correct data is sent to each unit of decoder. Comparison of these methods of sorting are performed to find the most fitting for Field Programmable Gate Array (FPGA) implementation. The method of sorting selected is even-odd merge sorting method, and the results that are found are in terms of resources occupied and maximum speed.

The performance measured based on the Bit-error-rate (BER) of the decoder implemented has shown coding loss of approximately 0.2 dB when compared with the simulated BER values.

V. FURTHER RESEARCH

With the discussion and researched carried out, it is seen that the proposed study has helped in accomplishing the first objective of the study designing of low BER turbo decoder. Hence, the next phase that must be accomplished will be focusing on achieving the remaining objective of the study, which also includes focusing on three different challenges that become very important to focus on when integration of codes produced by turbo coding must be performed in standards of communication that has high throughput such as LTE. To fulfil the data rates that are mentioned, one must foretell parallelization and methods for reducing the latency in the implementation of hardware/e of turbo decoders.

A. Implementation Techniques

The proposed solution must perform implementation on MATLAB for software side and CMOS VLSI architecture will be used for hardware side. The proposed communication system must follow the following block diagram which includes stages such as Formatting Digitization, Source Coding, Channel Coding, Multiplexing, Modulation and Access techniques. The data transmission and receiving order is represented with the help of arrows.

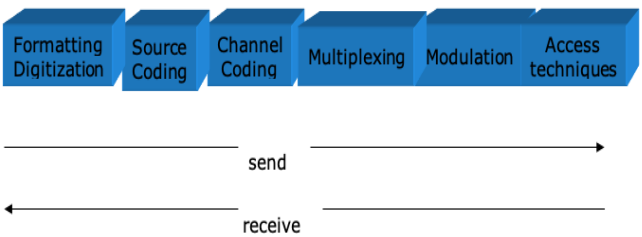

Fig 2: Communication System

ISSN: 2233-7857 IJFGCN

The proposed channel encoder performs encoding using an input sequence of k bits and encoding to to produce an output sequence of k bits with a code rate k/n and the redundancy factor of (n-k). The diagram of the encoder block of the channel is represented below

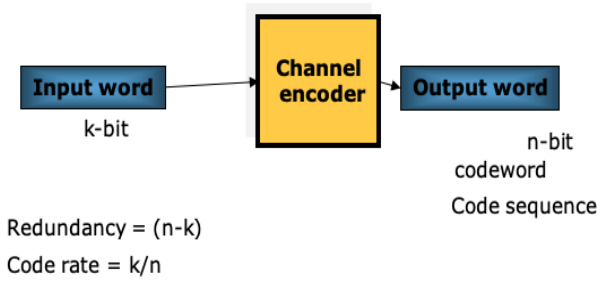

Fig 3: The channel encoders' block diagram

The encoding performed by the channel encoder faces challenges in the form of

1. The performance of error vs. Bandwidth with High redundancy consumption bandwidth
2. Power vs. Bandwidth that has Reduction in Eb/N0
3. The data rate vs. Bandwidth in a Higher Rate

In the architecture represented below, the inputs pass through the Recursive Systematic module which then generates systematic code word. This is again passed through an Interleaver module and then Recursive Systematic module for further systematic code word.

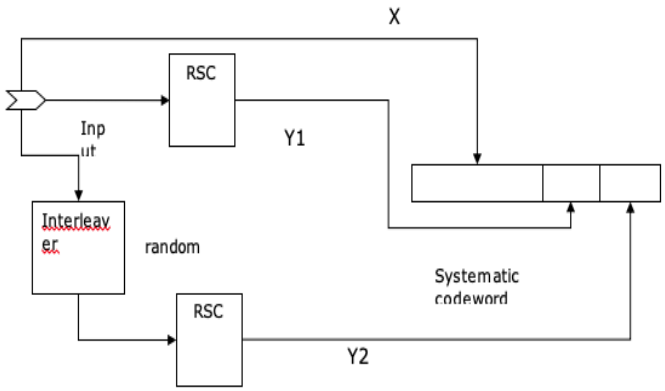

Fig 4: Coding Architecture

To develop the system model of iterative turbo code decoder, attesting frames are generated which are an integer to a vector of binary bits. At the receiver's end, serial to parallel de-multiplex has been designed. to encode the frames, recursive Systematic Convolutional encoder has been developed which uses turbo encoding process. To complete the decoding process, the encoded data is converted from vector of bits to integer, and set up trellis for the encoded data. For the simulation of the turbo encoding and turbo decoding system, assuming a uniform distribution, the information bits are randomly generated. There is generation of a random interleaver for bits of each frame. The code performance is calculated from the average performance among all interleavers.

ISSN: 2233-7857 IJFGCN

VI. RESULTS

The performance of turbo decoder has been realized on developed communication model with AWGN channel. Number of iterations has been tried on developed communication model. Plotted result has been shown in in Fig 5. Fig 5 shows the bit error rate gradually reduces with increase of signal to noise ratio. Number of iteration affects the bit error rate as shown in fig 5.

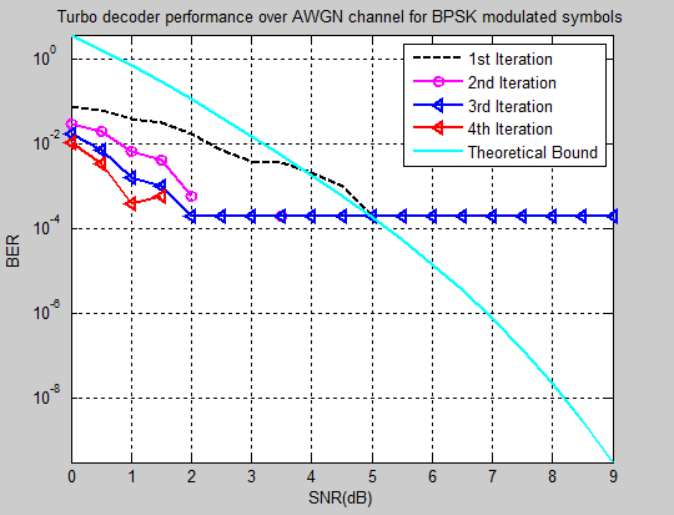

Fig 5 : Turbo decoder performance for BPSK modulated system over AWGN channel.

Developed communication model of turbo decoder is verified with different AWGN channels and different iterations. Result has been plotted and shown in Fig 6. In Fig 6 bit error rate behaviour are almost same in different AWGN channels, The SNR value increases when compared to the initial channel.

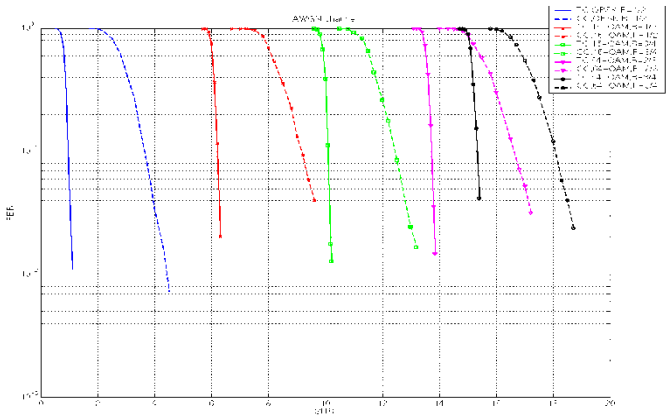

Fig 6 : Comparison between SNR(x-axis) and BER(y-axis) in AWGN channel

The number of iterations can be then adjusted to acheieve better performance and complexity trade – off. The coding system comparision graph of BER (bit error rate) and SNR(signal to noise ratio) obtained from the coding architechture is shown below.

ISSN: 2233-7857 IJFGCN

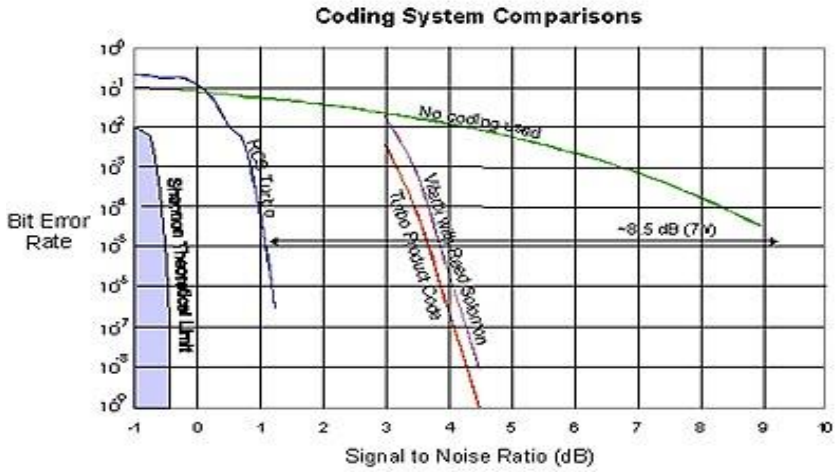

Fig 7 : Comparision of the SNR and BER of Coding system

CONCLUSION

Cellular and other technology makes it possible for people to be connected to the rest of the world from anywhere, anytime. All these wireless networks demand for high rate of transmission quickly, timely and accurately. For providing the good accuracy or to recover the original signal at the receiver end, forward error correction codes have been implemented. There are several types of error correcting techniques used like convolution coding, but it fails to maintain the lower values of signal to noise ratio as the length of code increases. So a new version of coding called turbo coding was introduced that can achieve a level of performance that comes closer to theoretical bounds than more conventional coding systems. The inherent iterative process of decoding restricts turbo decoder to process data at higher data-rate. BER performance also depends on frame size and interleaver type used for implementation of encoder and decoder. Bit-error-rate (BER) performance of the implemented decoder has shown a coding loss of approximately 0.2 dB in comparison with the simulated BER values. We have investigated the techniques of message ling and state metric normalization, which improve the BER performance and prevent potential overflow, respectively. Furthermore, a bypass mechanism is proposed for allowing a hard-wired interleaver to support the decoding of frames having different lengths and interleaver patterns. In order to fulfil the data rates mentioned above, The performance of turbo decoder has been realized on developed communication model with AWGN channel and The problem of decoding in received signal has been realized.for further hardware implementation of turbo decoder for LTE standard communication with efficient hardware architecture.

REFERENCES

[1] Rashmi R and Manju Devi , "Evolution of Wireless Communication along with Encoders" International Journal of Innovative Technology and Exploring Engineering (IJITEE), Volume 9, Issue 1, November 2019,Page No 2589-2593.

[2] Lekha S and Jagdish D. kene, "Review on Role of Turbo Encoder and Decoder in LTE Network" International Journal of Science, Engineering and Technology Research (IJSETR), Volume 5, Issue 1, January 2016.

[3] Prabhavati D. Bahirgonde and S. K. Dixit, "BER Analysis of Turbo Decoding Algorithms" Foundation of Computer Science FCS, New York, USA Volume 4– No.3. 26-29, 2016.

ISSN: 2233-7857 IJFGCN

[4] Yogesh BEEHARRY, Krishnaraj M. S. SOYJAUDAH and Tulsi Pawan FOWDUR, "Performance of Bit-Level Decoding Algorithms for Binary LTE Turbo Codes with Early Stopping" Yogesh BEEHARRY et al. / IU-JEEE Vol. 17(2), 3399-3415, 2017.
[5] Zhongfeng Wang, Zhipei Chi and Keshab K. Parhi, "Area-Efficient High-Speed Decoding Schemes for Turbo Decoders" IEEE transactions on very large scale integraton(VLSI systems, VOL. 10, NO. 6. 902-912, 2002.
[6] Rahul Shrestha and Roy P. Paily, "High-Throughput Turbo Decoder with Parallel Architecture for LTE Wireless Communication Standards" IEEE transactions on circuits and systems-1: REGULAR PAPERS. 1-12, 2017.
[7] Ardimas Andi Purwita, Arnaud Setio and Trio Adiono, "Optimized 8-Level Turbo Encoder Algorithm and VLSI Architecture for LTE" I2011 International Conference on Electrical Engineering and Informatics. 17-19, 2011.
[8] Liang Li, Robert G, Maunder, Bashir M. Al-Hashimi and Lajos Hanzo, "A Low-Complexity Turbo Decoder Architecture for Energy-Efficient Wireless Sensor Networks" 1-9.
[9] Cristian Anghel and Constantin Paleologu, "Simplified Parallel Architecture for LTE-A Turbo Decoder Implemented on FPGA" Advances in Circuits, Systems, Signal Processing and Telecommunications. 102-111, 2009.
[10] Lohith Kumar H G, Manjunatha K N, Suma M S, C K Raju and Prof.Cyril Prasanna Raj P, "Design and Performance analysis of a 3GPP LTE/LTE-Advance turbo decoder using software reference models" International Journal of Scientific & Engineering Research Volume 2, 1-4, July-2011.
[11] Guohui Wang, Aida Vosoughi, Hao Shen, Joseph R. Cavallaro, and Yuanbin Guo, "Parallel Interleaver Architecture with New Scheduling Scheme for High Throughput Configurable Turbo Decoder".
[12] Samir Jasim Mohammed and Ansam Abbas Obaid, " Design and Implementation Different Types of Turbo Decoder with Various Parameters ", International Journal of Computer Applications (0975-8887), Volume 166 –NO 11, May 2017.
[13] Christoph Studer, Christian Benkeser, Sandro Belfanti and Qiuting Huang Fellow" Design and Implementation of a Parallel Turbo-Decoder ASIC for 3GPP-LTE" ITO APPEAR IN IEEE JOURNAL OF SOLID-STATE CIRCUITS, 1-9, 2011.
[14] Prabhavati D. Bahirgonde, Shantanu K. Dixit, " Low Complexity Modified Constant Log- Map Algorithm for Radix-4 Turbo Decoder" 2015 International Conference on Pervasive Computing (ICPC)
[15] Shivshankar Mishra and Harshit Shukla and Suneel Madhekar," Implementation of Turbo Decoder Using MAX-LOG-MAP Algorithm in VHDL " IEEE INDICON 2015 1570169743.
[16] Cristian Anghel and Cristian Stanciu and Constantin Paleologu, " Sorting Methods Used in Parallel Turbo Decoding for LTE Systems ".
[17] C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon Limit Error-Correcting Coding and Decoding: Turbo-Codes," in Proc. 1993 *InternationalConference on Communications* (ICC '93), Geneva, Switzerland May 1993, pp. 1064–1070.
[18] Claude Berrou, Alain Glavieux and Punya Thitimajshima "Near shannon limit error – correcting Coding and decoding turbo-codes" IEEE Transactions on Communications, 44:1261 – 1271,Oct.1996.
[19] Third Generation Partnership Project, "3GPP home page" www.3gpp.org.
[20] Vogt.J and Finger.A, "Improving the max-log-MAP turboDecoder," Electron. Lett., vol. 36, no.23, pp.1937 1939, Nov 2000.

ISSN: 2233-7857 IJFGCN

[21] K. Loo, T. Alukaidey, and S. Jimaa, “High performance parallelised 3GPP turbo decoder," in *IEEE Personal Mobile Communications Conference*, April 2003, pp. 337- 342.
[22] A.J. Viterbi. An intuitive justification and a simplified implementation of the MAP decoder for convolutional codes. *IEEE J.Sel. Areas Commun.*, vol.16:pp.260–264,Feb.1998.
[23] R. Dobkin, M.Peleg, and R.Ginosar. Parallel interleaver design and vlsi architecture for low-latency map turbo decoders. *IEEE Trans.VLSI Syst.*, 13(4):427–438,200.

ISSN: 2233-7857 IJFGCN