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Investigation on Variable Latency Speculative Approach in Parallel Prefix Adders

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Abstract

In many digital circuits, adders are the most important block. The entire performance of the circuit is influenced by the characterization of the adder circuit. The conventional adders such as carry lookahead adder, ripple carry adder, etc., produce huge amount of path delay in the intermediate stage of computation. This problem can be solved by developing the approximation adders. The variable latency adder is one of the approximation adders which have the inbuilt error detection and correction scheme. Prefix computation is the part of the VLSA which is performed by parallel prefix adders. In this paper, we performed an efficient FPGA implementation of parallel prefix adders such as Sklansky, Kogge-Stone, Han-Carlson and Ladner Fisher adders. The performance of the above adders are analyzed and Kogge Stone adder performed 89% better than Sklansky adder, 50% better than han carlson and 66.6% better than Ladner Fisher adder.

Keywords—*VLSA, parallel prefix adders, latency, generate and propagate signals, EDC.*

I. INTRODUCTION (*HEADING 1*)

Adder is one of the important blocks in many digital circuits. In today's digitalized computers, processors and controllers had inbuilt arithmetic logic unit. This ALU performs the addition and multiplication simultaneously. In processor end, the adder is not only employed for ALU unit but also used for measuring the table indices, increment / decrement operators, addresses, etc.,. This type of adders can be represented for many numbering systems like BCD, excess-3. Hence, most of the adder operations based on the binary numbering format. Digital computer arithmetic is one of the important features in the logic design. It has the aim to design the appropriate algorithm to meet out the better utilization of the available hardware. Basic and ancient set of Boolean functions, arithmetic operation which are depended on the hierarchy of functions. This function can be constructed in a simple manner. The parameters like power, speed, LUT and chip area are the most important aspects for measuring the efficiency of the particular algorithm. Hence, there is an unbreakable bonding between the algorithm and the implementation technology.

To improve the performance of adder, two important methods are available. The primary method is called as 'System Level viewpoint' and the secondary approach is known as 'critical Style view point'. In ripple address, the primary method contains longest signal path. It is often used to minimize the trail to obtain full signal path delay. The outcome carry bit in the MSB is used to calculate this longest path delay. The secondary approach is based on the transistor level. The designing performance of the FA is depended upon the design skills of the semiconducting materials.

An optimized design is required to prevent any decrease in signal magnitude, provide small delays, consume less power in critical paths and even at low supply voltage maintain consistency while moving headed for smaller designs such as in nanometer range. There are many approximation design methodologies available for minimizing the hardware utilization, complexity and critical path of the

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adder. Speculative operation is a vital approximation methodology to meet out the above requirements. In this speculative adder, the final sum bit is calculated from the past k LSB (i.e.) (n > k). The main advantage of the speculative design is to make the addition operation faster than the convention adder. Segmented adder is also another type of approximation adder. It is constructed by many small adders which are performed in the parallel manner. So, the chain of the carry propagation is reduced into smaller segments. The concept of segmentation is fully used but the incoming bits for carry generation are chosen differently. Then this adder is called as carry select adder. The conventional full adder is designed to produce the approximate output sum and carry bits. This approximation approach reduces the power dissipation and critical path delay.

In this paper, efficient FPGA implementations of the speculative approximation adders are implemented to overcome the above mentioned issues. Hence, Section 2 represents the various literature surveys, Section 3 represents the background methodology, Section 4 represents the proposed design of approximation adder and Section 5 ends with the corresponding conclusion.

II. Literature Survey

Adders are the fundamental building block and they are found anywhere in the digital system. The performance improvement of these adders is really a challenging aspect. Variable Latency Speculative Adder (VLSA) is the one to develop the performance of the adder design. D. Esposito et al 2015 [1] presented a novel Han- Carlson based VLSA. In this approach, the EDC unit is designed with the prefix adder network. Subhashinee A and Rajasekaran C 2016 [2] presented a combined approach of speculation technique and the error correction. By this combined mannerism, the adder achieved better performance based on the area minimization compared to the conventional adders. I. Lin et al 2015 [3] discussed a brief design architecture of carry speculative adder (CSPA). The presented adder shown the best performance and low power consumption. In this approach, the carry and the sum generators are designed separately. The critical path delay and area are reduced by the block adder. This block adder contains only sum generator. X. Chen et al 2017 [4] mainly focused the approximation adder computation accuracy. The author [4] designed the Aware Predictor (CAP) which uses the spatial-temporal correlation information of incoming streams. This is used for predicting the incoming carry values for subordinate adders. The adder latency can be significantly reduced by CAP which utilizes the fewer amounts of prediction bits. A. Chakraborty et al 2017 [5] extended the usage of speculative adders to design the 1D/2D DWT architecture. The presented design includes cost effective and high speed architecture. S. Daphni and K. S. V. Grace 2017 [6] briefly explained the design methodology and performance analysis of the variety of PPA. The performance analysis is done by comparing the parameters like power, area and delay with the existing adders.

Marouf et al 2017 [7] implemented a FPGA based PPA. The designing approach contains five parallel prefix network called Han-Carlson Adder (HCA), Kogge-Stone Adder (KSA), Sklansky Adder (SkA), Brent-Kung Adder (BKA), and Ladner-Fischer Adder (LFA). They are implemented in 60nm Altera Cyclone IV. S. Muthyala Sudhakar et al 2012 [8] explored the one of the prefix adder called Han-Carlson adder. It is computed for longer word size bits. The author designed his method with one Kogge-Stone adder and two Brent-Kung adders. Hence, the Brent-Kung adders are placed in the beginning and end level of the prefix network. The Kogge-Stone adder performed in the middle stage. So this adder is termed as hybrid Han-Carlson adder. S. Gedam et al 2014 [9] presented a modified hybrid design of Han Carlson prefix adders. This adder significantly decreases the area, power consumption and hardware complexity. Z. Moudallal et al 2011 [10] presented a new design for reshaping the Kogge-Stone adder to reduce the PDP. The author designed this adder for multimedia applications.

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III. VARIABLE LATENCY SPECULATIVE ADDERS

The VLSA are mainly designed to reduce the critical path delay. It consists of five stages of processing steps. The initial step is pre-processing which perform the XOR and AND operations of the incoming bits. Prefix processing, error detection and correction are held in the intermediate processing. The final processing includes the post processing which computes the final sum and carry bits. A simple mathematical operation involved in the pre – processing and post processing steps. Speculative adder performance is mainly based on the calculations performed in the prefix processing, error detection and correction stages. Fig. 1 shows the generalized block diagram of the variable latency speculative adder.

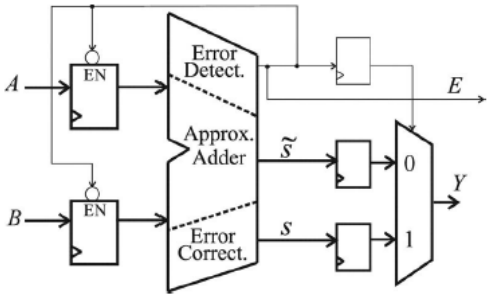

Fig. 1 Variable latency speculative adder

The speculative scheme employed in the VLA. The accurate arithmetic operations are modified as the approximate operation. The aim of this approximation technique is to improve the adder faster and produces the exact results. But it does not perform correct manner in all time. Sometimes, it produces the approximate results too. Fig. 1 illustrates the VLSA (D. Esposito et al 2016) [11]. The approximation adder is constructed with EDC network. The output signal E becomes high, then the speculation failed and the error can be detected. The EDC performed the correction process by introducing the clock cycle. When there is no error, the addition time requires only one clock cycle. When error is detected or speculation is failed, it requires two clock cycles. Then the averaging of addition time requirement is calculated from (1).

$$T_a = P_E \cdot 2 \cdot T_c + (1 - P_E) \cdot T_c = T_c(1 + P_E) \qquad (1)$$

In (1), the clock period is denoted as T_c. Similarly, the error probability is denoted as P_E.

The speculative prefix processing is the intermediate stage of VLSA. In this stage, the generate $g_{[m:0]}$ and propagate signals $p_{[m:0]}$ for each block can be calculated. The mathematical form of this stage is shown in (2).

$$(g_{[m:k]}, p_{[m:k]}) = (g_{[m:n]}, p_{[m:n]}). (g_{[l:k]}, p_{[l:k]})$$
$$= (g_{[m:n]} + p_{[m:n]}\, g_{[l:k]}, p_{[m:n]}\, p_{[l:k]}) \qquad (2)$$

A. Kogge Stone Prefix and Han Carlson Adders based Precomputation Block

Fig. 2 illustrates prefix computation block which is constructed by employing Kogge-Stone and Han-Carlson and prefix adders. The prefix operator simply represents the black dots. The placeholders are represented by white dots.

The KSA adder is made-up of $\log_2(n)$ levels and contains two fanout bits in each level. This KSA adder is constructed by huge number and black cells and many wire bonding. The Han-Carlson adder provides the better trade-off between the logic levels, fanout and black cells. The BKA are performed in the final rows of the HCA. The intermediate rows are processed with the help of KSA graphs. Fig.

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2 shows the HCA which consists of BKA at the initial and final level of processing. The number of logic level processed by HCA is $1+\log_2(n)$.

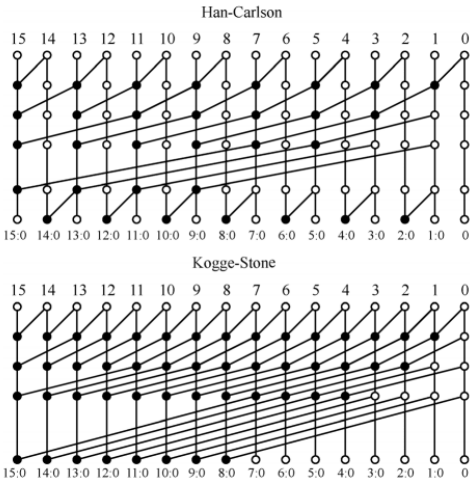

Fig. 2 Han-Carlson and Kogge-Stone parallel-prefix topologies n=16.

B. Speculative based Prefix-Processing

The speculative based prefix-processing stage is slightly modified in the conventional prefix adder which are described in the past section. In this type of prefix-processing stage, the generate and propagate signal of the subset blocks are computed for calculating the accurate carry values. But in the conventional processing, the entire blocks are processed for carry generation. The out coming bits from the speculative processing are also used in the next EDC stage.

C. Post-Processing

In the stage, the approximate carries $c_i`$ and sum $S_i`$ bits are calculated. The post processing stage involves the XOR operation which is performed between the p_i and previous stage carry $ci_{-1}`$.

$$S_i` = p_i \oplus c_{i-1}` \quad (3)$$

The approximate carries are calculated from the generate signals those are presented in the final level of the prefix processing stage.

D. Error Detection

The error detection is processed when the approximate carries produces the wrong output bits. This mis-prediction can be found by the error detection unit in the VLSA. Once, the error is detected, the correction stage performed to produce the accurate sum bit to the upcoming clock period.

E. Error Correction

The prefix-processing levels are used to compose the error correction stage. These levels are reduced to design the speculative adder. The introduction of the error correction stage maximizes the fanout which also affects the speed of the adder.

IV. PROPOSED MULTIPLEXER BASED PARALLEL PREFIX ADDERS

The existing CLA architectures have huge amount of delay for processing the incoming bits. This conventional architecture is slightly modified by using the PPA to reduce propagation delay problem. The PPA is the modified carry look ahead adder. These are worked in the parallel prefix form. The main benefit of the PPA is to reduce the carry chain delay for bits 8, 16, 32, 64 and 128. The PPA

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shows the better efficiency even for high order bits are processed. Logarithmic delay is produced by the PPA. Hence, the faster transformation of carries from previous stage to the next stage is done.

These adders perform parallel addition which is important aspect in microprocessors, Digital signal processing and other high speed applications. Parallel Prefix adder lowers logic complexity and time delay thereby improve performance. So Parallel Prefix adders are required elements in the high speed arithmetic circuits.

Tree adders generate carries in parallel so that they compute fast but with increased area and power. The tree adder reduces the logic level to N. This reduction is done by employing the parallel mechanism. This is also one of the important merits of the parallel prefix adders. The carry path of the PPA is more reliable in terms of speed when compared to other exact adders. The delay complexity of the PPA is calculated as O (log2N). The prefix computation of the parallel adder consists of two main steps. One is Computing carry generation (G) and another is carry propagation (P). These two steps are performed on the incoming bits X and Y. The propagate and generate signals are calculated and mathematically expressed in (4) and (5).

$$P_i = X_i \oplus Y_i \quad (4)$$

$$G_i = X_i \,.\, Y_i \quad (5)$$

Prefix computation is calculating all carry signals in parallel. This step consists of generate and propagate carries generation respecting to each bit. Parallel approach is used for this execution. Once the carry generation is done, they are divided into sub-segments. Carry propagate P_i and generate bits G_i are used as midway signals. Carry generating operation block is important in parallel prefix adders, and consists three types of components called black cell, graycell and buffer.

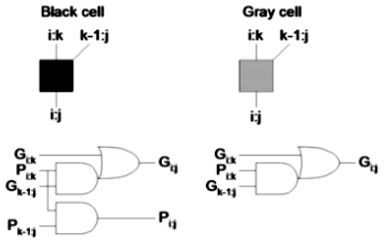

Fig. 3 Black and gray cell architecture (N Aruna Kumari et al 2019) [12]

In Fig. 3, the black cell and gray cell are implemented by employing basic gates such as AND, OR. The black cell illustrated in Fig. 3 accepts the four inputs and produce the generate and propagate signals. Similarly, the gray cell accepts the three inputs and produce the generate signal alone. In our proposed design, the AND-OR logic of these cells can be replaced by the multiplexer unit. The mux unit also accepts the four inputs for black cell and produce the generate and propagate signals. It also accepts three inputs for gray cell and produces the generate signal. The proposed implementations of the gray and black cells are shown in Fig. 4.

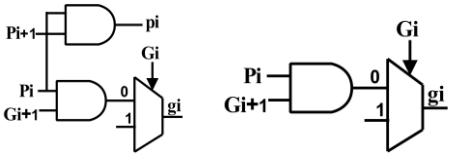

Fig. 4 (a) Proposed Black cell and (b) Gray cell

The conventional gray cell provides the generate signal as '1' when G_i is high or Pi and $G_{k-1,j}$ are in high. This operation is modified into mux unit. The proposed gray cell accepts the two inputs Pi and $G_{k-1,j}$ are combined and given to the one input of the 2:1 multiplexer. The third input G_i is considered as selection line for the proposed gray cell. The proposed architecture simplifies the conventional gray cell and it consumes the lesser amount of area.

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Similarly, the proposed black cell is implemented by means of the proposed gray cell and AND gate. The proposed black cell also produces the same output which is described in the conventional black cell.

Next to the propagate and generate signal generation, the parallel prefix computation takes place in the proposed method. The proposed design consists the same architecture for the prefix computation block. Fig. 5 – Fig. 8 shows the different parallel prefix adder configurations (D. Esposito et al 2016) [11]. The black and gray cells presented in following Fig. 5 – Fig. 8 was replaced by the proposed black and gray cells.

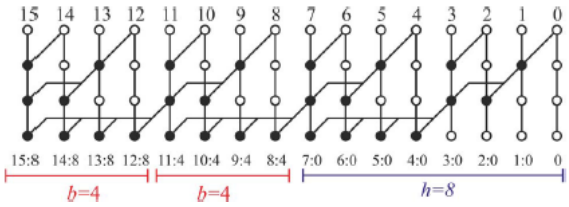

Fig. 5 16 bit Sklansky speculative Prefix Adder

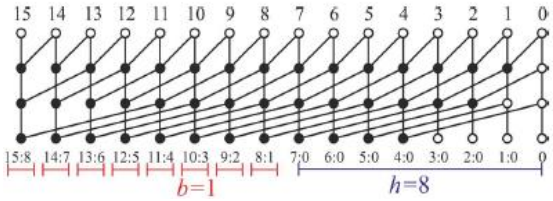

Fig. 6 16 bit Kogge Stone speculative Prefix Adder

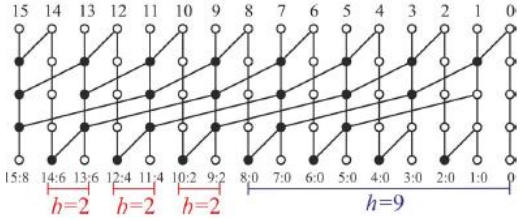

Fig. 7 16 bit Han Carlson speculative Prefix Adder

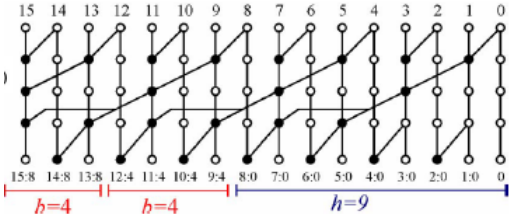

Fig. 8 16 bit Han Carlson speculative Prefix Adder

V. EXPERIMENTAL RESULTS

The overall implementation of the existing and proposed prefix adders are implemented by using the Altera Quartus II 9.1 software platform. This platform is well known for many FPGA based implementation methodologies. It contains variety of FPGA devices such cyclone, max and stratix families. These are come under different nm CMOS process such as 90nm and 65 nm. The operating voltage and temperature are varied based on the device configuration.

In this paper, two FPGA devices are selected for implementation. Both existing and proposed design of prefix adders are implemented in Cyclone and Stratix devices. The proposed design is justified by measuring the parameter such LUT, power and delay. Table. 1 to Table. 4 shows the parameter measures of existing parallel speculative prefix adders. The proposed parameter measures are shown in Table. 5 to Table. 8.

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TABLE I. PARAMETER MEASURES OF 16 BIT SKLANSKY SPECULATIVE PREFIX ADDER [11]

FPGA	***LUT***			***Power(mW)***	***Delay (nS)***
	Available	Used	Utilization		
C-II	4608	62	2 %	46.38	10.437
C-III	5136	62	1 %	68.22	9.182
S-II	12480	61	< 1 %	345.19	9.919
S-III	38000	61	< 1 %	406.94	10.030

TABLE II. PARAMETER MEASURES OF 16 BIT LADNER FISHER SPECULATIVE PREFIX ADDER [11]

FPGA	***LUT***			***Power(mW)***	***Delay (nS)***
	Available	Used	Utilization		
C-II	4608	37	< 1 %	161.02	13.414
C-III	5136	37	< 1 %	120.47	10.429
S-II	12480	26	< 1 %	450.57	11.613
S-III	38000	26	< 1 %	480.28	12.736

TABLE III. PARAMETER MEASURES OF PROPOSED 16 BIT SKLANSKY SPECULATIVE PREFIX ADDER

FPGA	***LUT***			***Power(mW)***	***Delay (nS)***
	Available	Used	Utilization		
C-II	4608	37	< 1 %	184.16	12.745
C-III	5136	37	< 1 %	131.37	10.758
S-II	12480	31	< 1 %	467.48	10.819
S-III	38000	31	< 1 %	491.82	12.498

TABLE IV. PARAMETER MEASURES OF PROPOSED 16 BIT LADNER FISHER SPECULATIVE PREFIX ADDER

FPGA	***LUT***			***Power(mW)***	***Delay (nS)***
	Available	Used	Utilization		
C-II	4608	12	< 1 %	122.00	11.098
C-III	5136	12	< 1 %	100.55	9.849
S-II	12480	9	< 1 %	413.49	10.507
S-III	38000	9	< 1 %	449.59	9.514

CONCLUSION

A parallel prefix adder is one of the approximate adders which are used in many arithmetic circuits. The PPA have inbuilt EDC unit which are used for error detection and correction. This error detection and correction is done for achieving the significant error probability in the digital circuits. In this paper, 4 different schemes of parallel prefix adders are designed with the help of multiplexer unit. The proposed adder designs are verified with the existing adder architecture in terms of LUT, power and delay. The proposed design also implemented in two different nm CMOS technology. Overall, the proposed Sklansky prefix adder is improved by 40% when compared to existing Sklansky adder. Similarly Kogge stone adder is improvised by 50%, Han Carlson adder is improvised by 52% and Ladner Fisher adder is improvised by 67%. By comparing all proposed prefix adders, Kogge stone

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adder produced better performance. The presented prefix adder is further used in the VLSI based signal processing applications.

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