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A MACHINE LEARNING BASED ARCHITECTURE IMPLEMENTATION FOR OBJECT DETECTION

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Abstract

The ConvNet (CNN) is a neural network technique that has been extensively employed in detect and recognize object, video analytics and image classification. ConvNet based algorithms aren't easy to be deployed in the embedded devices as the ConvNet is memory expensive and compute-intensive. There are many studies that have reviewed the implementation of ConvNet based classification models on hardware, a vast area of implementation ConvNet on FPGA is yet to be explored. This work proposed the half-precision floating point ConvNet implementation to detect object with Tiny YOLO v2 on Intel Altera Cyclone-IV FPGA using Verilog HDL. In view of the resource constrains of an FPGA in relationswith memory bandwidth, computational resources along with on-chip memory, the pre-processing of data is planned so that the concatenationof batch normalization addicted to convolution layer.

2. INTRODUCTION

YOLO is a solitaryConvNet that predicts the multiple object alongside with the box's class probability. The full image is trained and the detection process is optimized by the YOLO. This technique has numerous benefits than the traditional methods (RCNN, Fast RCNN) of the object detection.YOLO works extremely faster than the previous methods of detecting the object. Though the detection is considered as a regression process, it doesn't require any complex pipeline process.YOLO archives twice the mean average (mAP) precision than the other system. The image is globally reasoned by YOLO while predicting objects of the given input. Similar to regional proposal and sliding window techniques, YOLO also considers the entire image while training and testing the image hence the image classes contextual information and their appearance are encoded.The natural images are trained and tested in the network, the various detection methods such as DPM, R-CNN areoutperformed by YOLO. YOLO is generalizable and is less possible to break when employed in new domains. Here in our proposed work we use the Tiny YOLO v2.

3. LITERATURE SURVEY

Caiwen Ding et al., presented a work to prevail the substantial accuracy loss, decreased utilization of DSP blocks in FPGAs. The proposed architecture is REQ-YOLO which is the basis for detecting objects that is aware of resources and weight quantization which includes the method of block-circulant matrix and a diversified weight quantization employing ADMM[1]. Ren et al., introduced a RP technique for the object detection framework facilitating image convolution features through Regional Proposal Network (RPN).The convolutional features can be shared by training Fast R-CNN and alternating optimization RPN. High class Region proposals (RP) is generated with the training of Regional Proposal networks (RPN) that is employed with Fast Region-based CNN in the object detection process [2].

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Wei.L et al., proposed a technique for the detecting the objects in the input images with the insight of single DNN. The method known as Single-Shot MultiBox Detection discretizes bounding boxes output space into a default boxes based on various aspect ratios including the feature map measure per location[3].Lin Bai et al., introduced a scalable, high performance accelerator using ConvNet deployed on FPGA employing the technique of Depth wise Separable Convolution. The CNNs including MobileNet Version 2, Xception employs the embedded systems with Depth wise distinguishable convolution which in turn reduces the operations and parameters with reduced loss in accuracy. The proposed technique provides the balance between processing speed and resources of the hardware, the accelerator fits different size FPGAs[4].

4. EXISTING SYSTEM

The prevailing system that proposes a hardware computing architecture to identify face that classify the given input image as human face or not. This digital architecture was designed and verified in MATLAB Simulink using Xilinx block set. This was also released in a FPGA platform.Learned filter were deployed to classify based fully on features than the assumptions used by the image processing methods.

4.1 Digital Hardware Architecture

In hardware realization of this proposal, the architecture functions as a multi-stage filtering, decimation, sub-sampling and non-linear ConvNet decision making algorithm. There are two stages in this realization.

In the initial stage, each and every frame of the input video is filtered and sub-sampled with a factor of two in all the dimensions. It is then convolved by four different linear FIR kernels with a mask size 5x5. The obtained filtered output images from FIR kernels are scaled, biased and further biased with dissimilar values represented as $b_{1,k}$, α_k and $b_{1,2,k}$ where k = 1, 2, 3,4. Four sets of intermediate output images are provided by scaling, filtering, biasing and non-linear decision blocks(DEC). The above operations are applied for all frames in the video. The decision regions from this stage form sub-images which are then applied to the succeeding stage of CovnNet algorithm.

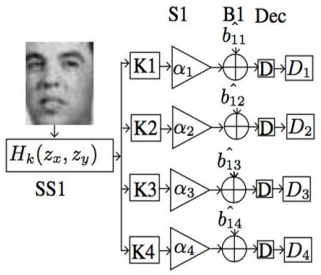

Fig. 4.1 First stage

In the next stage, sub-image outputs of the starting stage are given as input to this stage. This stage is further sub-divided into two architecture. In first architecture, the first quad images are sub-sampled and further convoluted with 8 diverse kernels represented as M1, M2, M3…, and M8 with a kernel of size 3x3. The operations performed in first stage is again implemented in this step of this stage. While the second algorithm pairs with output of former stage in an order denoted by (P_k, Q_k) and using 6 FIR filter kernels, sub-sampling and convolution is performed again. These pairs are separately summed and scaled, biased with distinct values represented as $b_{2,p}$, β_p and $b_{2,2,p}$ where p = 9,10, …,14. The resulting output is processed over DEC. The first architecture produces 8 images

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while the second architecture produces 6 output images. Thus, overall 14 images areattained as output.

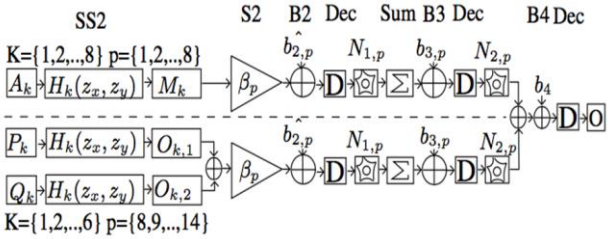

Fig. 4.2 Second stage

These images of size 6x7 are vectorized and a classical dot product operation is undergone with its respective neuron block(6x7) represented as $N_{1,p}$ where p=1,2,3,4,…,14 providing 14 different output images of same size. Weight metric is calculated and 14 dissimilar values are obtained. Now these are again biased and then perform dot product function with the next or second layer of neural network represented as $N_{2,p}$. Then obtained values are summed, biased (b4) and sent through the final DEC to attain the desired output. From this obtained value, the segregation of a given sample image as face or not is done. If the result is positive, then the given sample image is a face whereas the negative result indicates that the given sample image is not a face.

Implementing the face detection using MATLAB Simulink with 1164 test images, the implementation provided an accuracy of 96.56% where 1124 images where correctly detected. While realizing this in a FPGA provided accuracy above 90%. This proposed work could be a fair candidate in different face recognition and face detection tasks.

5. PROPOSED SYSTEM

In our proposed method, we desire to implement Tiny YOLO v2 in Intel FPGA to detect object using a Half-precision (16-bit) floating point. It is realized using Verilog HDL.

5.1 Tiny YOLO v2 Architecture

YOLO possess a unique approach that apply a single ConvNet on the whole image and identifies the multiple objects with boxes bounding it. Whereas the previous methodologies repurpose classifiers to detect object information in the frame or image. The Tiny YOLO v2 consists of nine convolutional layers, where each layer is equipped by means of a ReLU activation function in additionwith batch normalization operation strew with 6 max pooling layers and region layer. The resolution of the given input image to the Tiny YOLO v2 is 416 × 416 pixel.

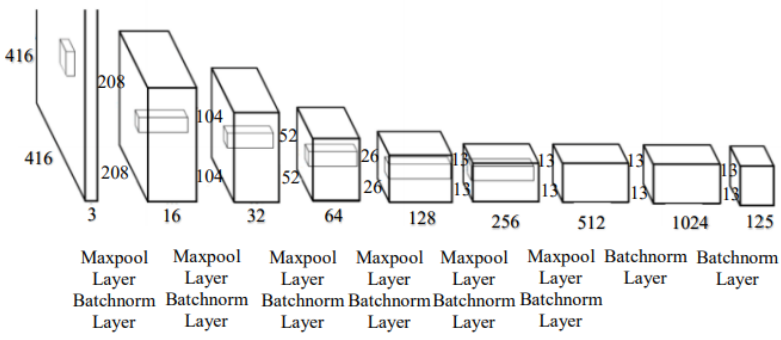

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Fig. 5.1 Architecture of Tiny YOLO v2

5.2 Convolution Layer

The feedforward process is employed to detect object in Tiny YOLO v2. In feed forward computation period, convolution layer itself occupies over 90%. So, in Tiny YOLO v2,convolution layer is reduced to progress the accelerator performance. For a solitary input image, billions of additions and multiplication operations are performed between filters and local regions in convolution layer.

$$X^{(i)} = \sum_{i=1}^{n} (x^{(n)} \times w^{(k)}) + b$$

where,$X^{(i)}$is theOutput feature Pixel, $x^{(j)}$ is theInput feature Pixel, $w^{(k)}$represents Convolution weights and b is the Convolution bias.

The overallsum of operations performed by the convolution layer can be calculated using the following equation.

$$\text{Operations} = 2 \times N_{in} \times K \times K \times N_{out} \times H_{out} \times W_{out}$$

where,N_{in} is the No. of input channels, K representing Filter size, N_{out} is count of filters, $H_{out}$is theOutput feature Height and W_{out} = Output feature Width

The above equation disregards the determination of the amount of operations of batch normalization processing and ReLU activation at every layer. Space complexity describes the memory requirement. Weight is the important parameter in Tiny YOLO v2 in convolution layer. The total sum of weights in convolutional layer represented as

$$\text{Weights} = N_{in} \times K \times K \times N_{out}$$

5.3 Activation Function

The need of activation function in CNN architecture is to perform a transformation process on the given input before it proceeds to the pooling layer. The most frequently used activation functions of CNN are Sigmoidal activation function. This activation function is bounded by minimum and maximum value and thus initiating saturation neuron in the top layers of the network. Leaky ReLU can likewise be used and it may cause the change in weight that makes the functions to never activate again in any data point.

5.4 Pooling layer

Dimensional reduction of the given input in ConvNet can be done using the Pooling layer. The pooling layer removes the redundant information and retains the most critical information. Average pooling and maximum pooling are the characteristic pooling functions. The Max pooling function returns the highest value and the average function returns the average value. The equations of the pooling function are

$$S[i, j] = \max\{S[i;, j']: i \leq i' < i+, j \leq j' < j + p\}$$

$$S[i, j] = \text{average}\{S[i;, j']: i \leq i' < i+, j \leq j' < j+ p\}$$

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5.5 Batch Normalization

The latter layer in network is batch normalization which provide unit variance or zero mean for input at any layer of Tiny YOLO v2. The normalization function is done to the preceding output by subtracting and dividing the batch mean and batch variance respectively that has been obtainedfrom the convolution layer. After this operation,output isshifted, scaled. During the CNN training stage,values of the variance, scale, bias and means are generated. These obtained values make each layer to learn independently and the overfitting is reduced due to the regularization effect. The batch normalization equationis represented as

$$X^{(J)} = \frac{(X^{(I)} - \mu)}{\sqrt{\sigma^2 + \xi}}$$

where, $X^{(J)}$is Output Pixel after batch normalization, $X^{(I)}$represents Output Pixel after convolution, μ is the Mean value, $\sigma^2$is the Variance, ξrepresents the Constant value.

5.6 Block Diagram

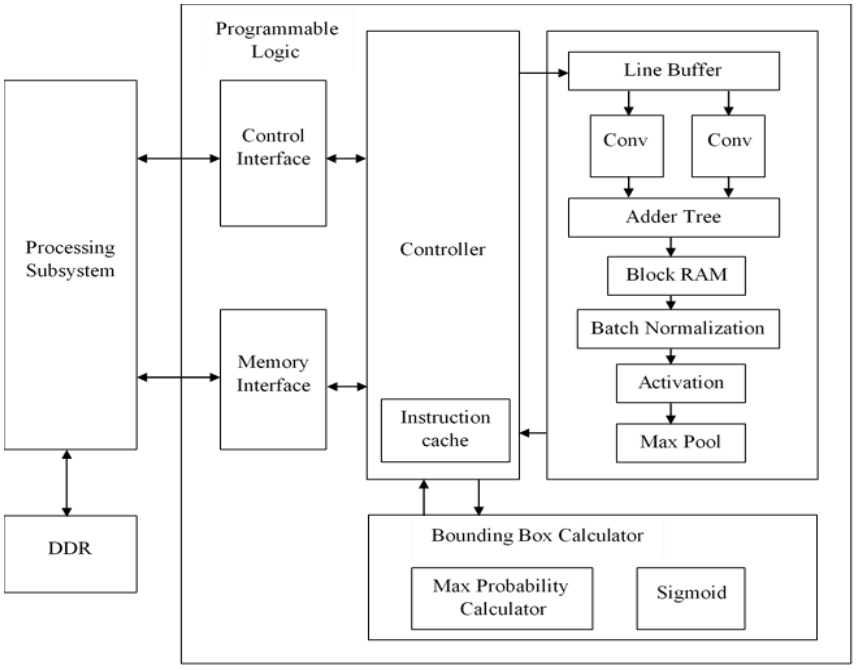

Fig. 5.3 Block diagram of Proposed work

As already discussed, the algorithms buffer the given input to the ConvNet. There are multiple convolution layers that process the input from the buffer and the output from this convolution layer are combined by adder tree which is followed by convolution layer. Then these are forwarded to the block RAM for Batch Normalization process where it provides the unit and zero variance. The shifted and scaled output from the preceding process is pre-transformed by activation function, then pooled by means of the Max Pooling operation in the pooling layer.

The bounding box calculator which mainly focuses only on bounding the detected object in the given image after processing through the CNN. Using the sigmoid function and the max

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probability calculator, the bounding of the recognized object in image is executed and thus object recognized in the given image.

6. RESULT

Initially Tiny YOLO v2 were implemented directly with the floating-point precision on Intel Altera Cyclone-IV. The utilization of hardware resource exceeded the hardware limitation as in utilize over 150% of RAM, 170% of logic and 70% of the DSP blocks in the hardware. Then to implement and outwork it, first the pre-processing batch normalization technique is approached which managed to reduce the exceeded hardware utilization by the algorithm. Instead of floating-point precision, half-precision floating point which is 16-bit is employed for further enhancement of algorithm to work efficiently.

Fig. 6.1 Predicted Image (Test Image) by Intel Altera Cyclone-IV using half-precision floating point Tiny YOLO v2

The image in Fig. 6.1 is the predicted test image of the half-precision floating point Tiny YOLO v2 on Intel Altera Cyclone IV. The hardware predicted the objects on the image with high accuracy.

7. CONCLUSION

The existing system that predicts whether the given image is a face or not were the input given of resolution 32x36 and of the format PGM (Portable Grey Map). The most frequently used image format like JPEG cannot be processed and also the real-time high-resolution images cannot be cast-off using the existing system. Our proposed system overcame both these limitations i.e. JPEG format and higher resolution images can be given as input to FPGA hardware for recognizing object with enhanced and optimized algorithm using half-precision floating point Tiny YOLO v2 in addition with batch normalization pre-processing. The proposed work is realized in the Intel Altera Cyclone-IV and obtained the result with high accuracy.

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