

Discrete Controlled Bi Frequency Boost Converter

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Abstract

A digital PID controller has been modeled for a Double frequency boost converter. The proposed converter is composed of two cells. One cell operates under high frequency and another cell operates under low frequency. Without the accumulation of extra control circuits, the converter can work at a very high switching frequency. The static and transient response of the proposed converter is enhanced and the switching loss of the converter is small. A discrete compensator incorporated with PID control algorithm enhances the dynamic response of the closed loop system. Double frequency boost converter with closed loop controller is simulated using MATLAB / Simulink and switching loss across the switches are found using pSpice software.

Keywords: Double frequency Boost converter (DF Boost converter), Switching loss, Efficiency, Discrete PID controller.

1. Introduction

Conventional Energy resources have sought a great deliberation in these times experiencing a fast development. The output voltage from renewable energy resources such as the fuel cells and photovoltaic systems are low. P.V systems appear to be the feasible solutions to the problems in the environment as they produce clean electricity [7]. D.C – D.C Boost converters are usually required in solar applications which produce a low voltage output. D.C – D.C Boost converter convert the D.C voltage from lower level to higher level, essential for automotive, Battery power system, D.C motor drive applications etc., [2] – [8]. In order to limit Boost Inductor's size and to limit the switching loss of the device, the switching frequency has been preferred arbitrarily. High switching frequency in Boost converter is required to improve the load transient response. However, increase in switching frequency results in higher switching loss as the switching loss is directly proportional to the switching frequency. Thus the efficiency is low. This lay a limit on raise in switching frequency and the enhancement of system performance is hindered. Obviously, when the switching frequency is low, the switching losses are low with improved efficiency. In order to decrease the switching loss, active and passive soft switching methods have been recommended.

The active method consists of an auxillary switch along with several resonant and diode components to provide zero voltage turn - on and turn - off of the main switch. Passive scheme provides zero current turn – on and zero voltage turn – off of the main switch with the accumulation of passive and diode elements only. Both active and passive soft switching techniques results in difficulty in control circuit and provokes unwanted E.M.I harmonics under variable load conditions. Thus, the reliability of the converters with soft switching techniques is reduced due to complications in the control circuit and added elements. Interleaved converter is the only alternative to depreciate the E.M.I harmonics [9]. Although interleaved converters improve the converter efficiency and reliability [5], circulating current arises due to interaction problem which is the major drawback [12]. The purpose of double frequency Boost converter is to overcome the circulating current problem and to attain good dynamic response and high efficiency in Boost converters [3]. The suggested configuration consists of high frequency and low frequency Boost converter cells supplied from a single dc voltage source. The flow of current in the high frequency Boost cell is redirected through the low frequency Boost cell. This current flow promptly falls down and the converter performance is

improved by high frequency Boost. Due to low current handling requirement of the high frequency cell in D.F Boost converter, the efficiency is intensified. The main challenge is to design a suitable control system of D.F Boost converter. Analog controller provides high output voltage at low operating duty cycles and lower voltage on the switch. The major disadvantage of this traditional controller is low reliability, complications over control, lack of tractability to system change. Digital controller provides more benefits than their analog counterpart. Some of them are: (i) Less influenced by din (ii) High response on changes in parameter (iii) Digital controller components are less prone to aging and atmospheric changes. (iv) No difficulty in operation. It offers high stability, quicker response and good dynamic response in terms of minimal overshoot [1]. Three most significant areas in digital control technique are 1) To sample the error voltage, Analog to Digital Converter is needed 2) To correct the error signal, and digital Compensator is postulated. 3) To attain high precision in the output voltage, Digital Pulse Width Modulation (DPWM) signals are created with high resolution.

The objective of this effort is to design a discrete compensator for double frequency Boost converter to subdue the above mentioned troubles. State space modeling method is used to model the double frequency boost converter and a digital PID controller [10] is used to model a discrete compensator for double frequency boost converter. Switching losses across various open loop boost converters are obtained using pSpice software [14] and simulations are carried out using MATLAB/Simulink.

2. General block diagram

Figure 1. outlines the entire block diagram of double frequency boost converter with closed loop control scheme. Using the first comparator, double frequency boost converter's output voltage is compared with the desired reference voltage to obtain the error signal. Digital compensation approach has been done to design a digital controller. The outcome of the controller is fed into the second comparator and third comparator. The obtained signal is compared with the distinct ramp signals of appropriate switching frequencies. Using the driver circuit, the out coming signals for gate are fed to the switches of the proposed double frequency Boost converter.

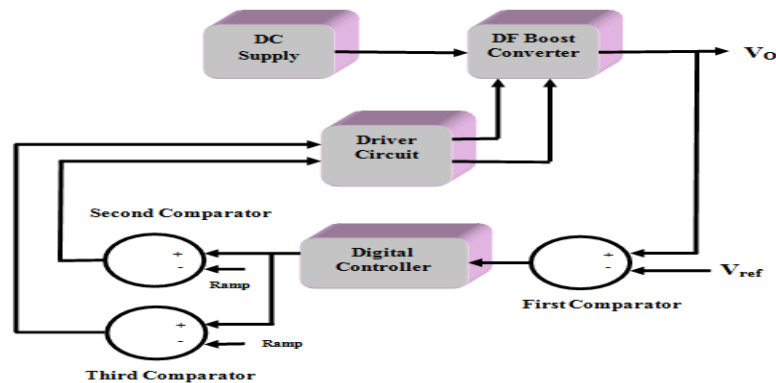


Figure 1. General Block Diagram

3. DF Boost converter design

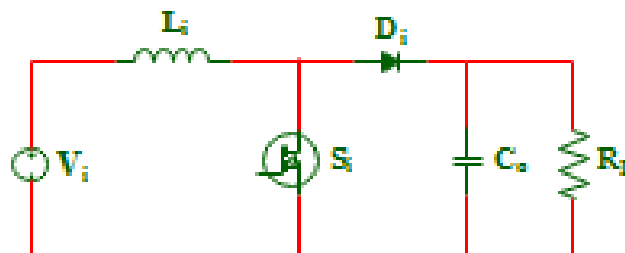


Figure 2. Conventional Boost Converter

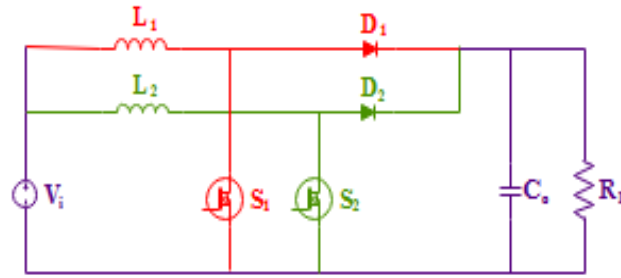


Figure 3. Double Frequency Boost Converter

The Duty cycle is

$$K = (V_o - V_{IN})/V_o \quad (1)$$

Where V_{IN} is the input voltage and V_o is the output voltage.

The value of Load Resistance R_L is

$$R_L = V_o^2/P_o \quad (2)$$

Where P_o is the output power.

The output current I_o is

$$I_o = P_o/V_o \quad (3)$$

The value of the inductor L is

$$L = (K * V_{IN})/(f_{sw} * \Delta I_L) \quad (4)$$

Where f_{sw} is the switching frequency and ΔI_L is the inductor ripple current.

The value of the capacitor C is

$$C = (K * I_o)/(f_{sw} * \Delta V_C) \quad (5)$$

Where ΔV_C is the capacitor ripple voltage.

The following design parameters are calculated from equations to 1 to 5, $V_{IN} = 12$ V, $V_o = 24$ V, $(P_o) = 15$ W, $f_H = 100$ KHZ, $f_L = 10$ KHZ, $L_1 = 63.15$ μ H $L_2 = 631$ μ H, $C = 44$ μ F, $R = 38.4$ Ω , $K = 50\%$.

4. Analysis of Efficiency

The expression for efficiency is confabulated to scrutinize the efficiency enhancement of double frequency boost converter. The scrutiny is also actionable to single low frequency and high frequency boost converters. At steady state, a clear loss model is acquired to depict the efficiency interconnection among the single high frequency boost, single low frequency boost and DF boost converters. The conduction loss and switching loss of active switch and diode are found using the on state voltage, V_{ON} and forward voltage, V_F of the switches respectively. Switching loss is taken into account since the switching loss usually dominates the total loss.

A. Losses in single frequency Boost converter

The total loss in single frequency boost converter falls under following categories - switching loss of the diode ($P_{D,S}$), switching loss of the switch ($P_{S,S}$), conduction loss of the diode ($P_{D,CON}$) and conduction loss ($P_{S,CON}$) of the switch [12]. The total losses can be anticipated from the following equations and Figure 4(a) and figure 4(b).

$$P_{S,CON} = KV_{ON}I_{La} \quad (6)$$

$$P_{D,CON} = (1 - K)V_F I_{La} \quad (7)$$

$$P_{S,S} = \frac{1}{2} f_{sw} V_I I_{La} (t_{on} + t_{off}) \quad (8)$$

$$P_{D,S} = \frac{1}{2} f_{sw} V_I I_{La} (t_{on} + t_{off}) \quad (9)$$

Where K is the duty cycle, V_I is the input voltage, f_{SW} is the switching frequency, I_{La} is the average current flowing through the inductor, t_{on} and t_{off} are the on time and off time of the switch or diode correspondingly.

B. Losses in double frequency Boost converter

The losses are classified into two parts: outer high frequency cell losses and inner low frequency cell losses. There is no variation on the conduction losses, the distinction is on the switching frequencies, f_H – high switching frequency and f_L – low switching frequency. I_{LH} is the current flowing through the outer high frequency cell inductor. I_{LL} is the current flowing through the inner low frequency cell inductor, t_{on} and t_{off} is the conduction time and non - conduction time of the switch or diode correspondingly. Figure 4(c) and figure 4(d) shows the losses across the high frequency and low frequency cell switch.

Outer High frequency cell losses are

$$P_{S,CONH} = 0.5KV_{ON}I_{LH} \tag{10}$$

$$P_{D,CONH} = 0.5(1 - K)V_F I_{LH} \tag{11}$$

$$P_{S,SH} = \frac{1}{4}f_H V_I I_{LH}(t_{on} + t_{off}) \tag{12}$$

$$P_{D,SH} = \frac{1}{4}f_H V_I I_{LH}(t_{on} + t_{off}) \tag{13}$$

Inner low frequency cell losses are

$$P_{S,CONL} = K(I_{La} - 0.5I_{LL}) \tag{14}$$

$$P_{D,CONL} = (1 - K)V_F(I_{La} - 0.5I_{LL}) \tag{15}$$

$$P_{S,SL} = \frac{1}{2}f_L V_I(I_{La} - 0.5I_{LL})(t_{on} + t_{off}) \tag{16}$$

$$P_{D,SL} = \frac{1}{2}f_L V_I(I_{La} - 0.5I_{LL})(t_{on} + t_{off}) \tag{17}$$

Total conduction loss in double frequency boost converter

$$P_{CON,DF} \approx P_{S,CON} + P_{D,CON} \tag{18}$$

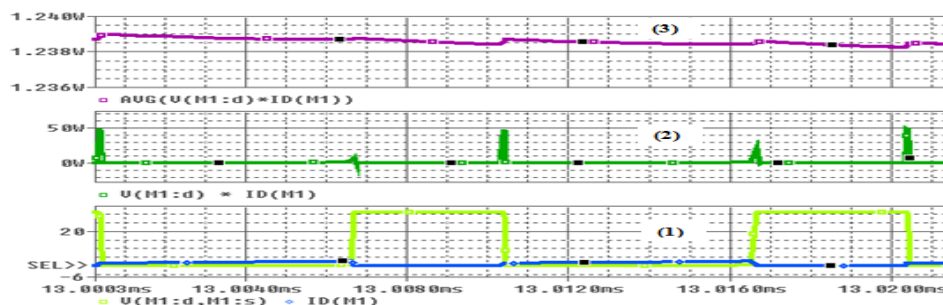
Total switching losses in double frequency boost converter

$$P_{S,DF} = f_L V_I I_L(t_{on} + t_{off}) \tag{19}$$

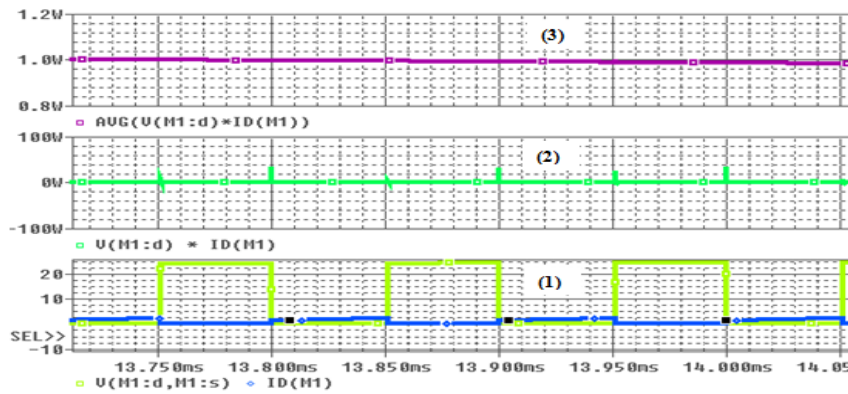
$$\text{Efficiency (\%)} = \frac{\text{Power Output}}{\text{Power Output} + \text{Losses}} \tag{20}$$

Table 1. Correlation of losses occurring in different types of Boost converter

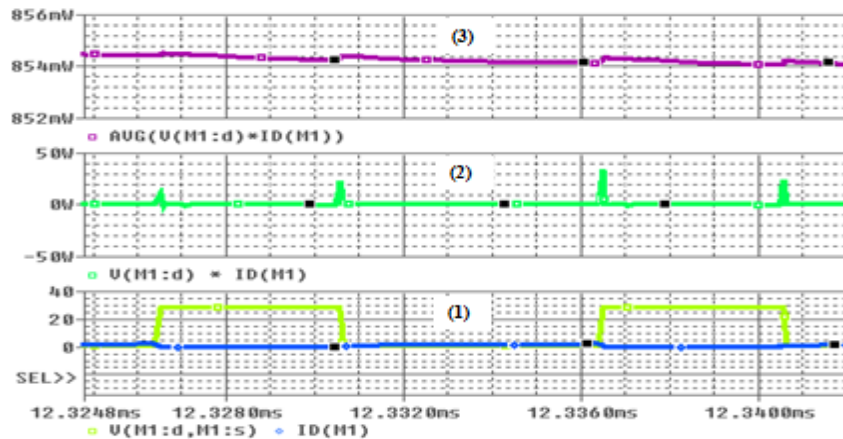
BOOST CONVERTERS	TOTAL LOSSES (Watt)	POWER OUTPUT (Watt)	EFFICIENCY (Percentage)
DF Boost	0.900	15.1744	94.40
LF Boost	1.000	15.10057	93.78
HF Boost	1.239	15.06492	92.40



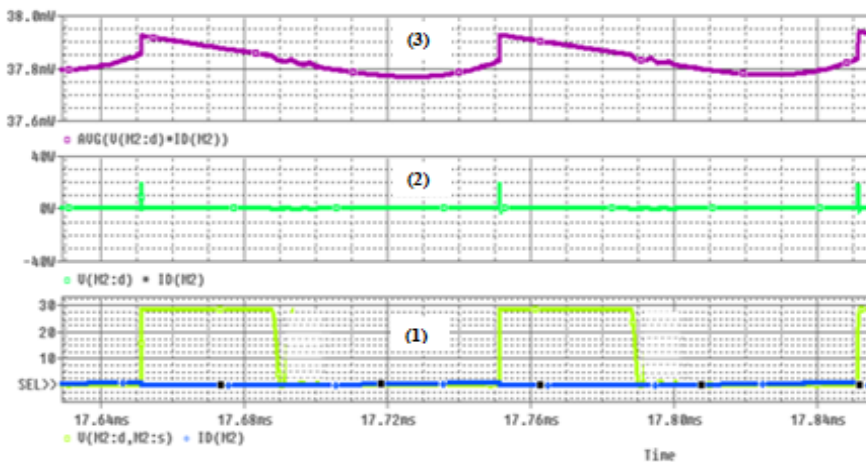
(a) Switching losses of High frequency boost converter



(b) Switching losses of Low frequency boost converter



(c) Switching losses at high frequency cell switch of double frequency boost converter (Outer cell)



(d) Switching losses at low frequency cell switch of double frequency boost converter (Inner cell)

Figure 4. Total Switching losses of various boost converters - (1) Switch Voltage and Current (2) Power Loss (3) Total Power Loss

The total losses and efficiency of single frequency boost converters and double frequency boost converter are detected from the figure 4 and equations 6 to 20. The total losses, output power and efficiency of various boost converters are shown in the table 1. The average current flowing through

the double frequency boost switches and diodes are similar to the average current flowing through the single frequency boost switches and diodes. It is evident from the above equations that the total conduction loss of double frequency boost converter and single frequency boost converter are identical. Also, the total switching loss of double frequency boost converter is nearly equal to the low frequency boost converter and smaller than the high frequency boost converter. Accordingly the efficiency of DF boost converter is superior than all other single frequency boost converter has been justified by the table 1.

5. State space analysis of double frequency boost converter

Double frequency boost converter has been simulated via state space modeling method following the design calculation [6]. The distinctive characteristics of this technique are that the design can be performed for different sets of input (ramp, step or impulse function) with the integrated initial conditions. By incorporating this technique for low frequency estimation of true dynamics, the irregular effect acquainted by the switching is neglected. Converter circuit's system equations are needed for the simulation. Below discussion is on the state space scrutiny. Pulse generator drives the switches S_1 and S_2 with an invariable switching frequency f_H and f_L correspondingly. The state

variables of DF boost converter are $x_1 = I_{LL}$, $x_2 = I_{LH}$, $x_3 = V_C$ and the state vector is $x(t) = \begin{bmatrix} I_{LL} \\ I_{LH} \\ V_C \end{bmatrix}$,

where I_{LL} , I_{LH} are the current flowing through the low frequency and high frequency cell inductor correspondingly and V_C is the capacitor voltage. The set of continuous time state space equations expressed below describes the system in which x and V_1 are state vector and input vector respectively and A , B , C , D are state coefficient matrices.

$$\dot{x}(t) = Ax(t) + BV_1(t) \quad (21)$$

$$y(t) = Cx(t) + DV_1(t) \quad (22)$$

Respective state equations for the four modes of operation are

Operating Mode 1:

Switches S_1 and S_2 - ON

$$\dot{x}(t) = A_1x(t) + B_1V_1(t) \quad (23)$$

Operating Mode 2:

Switch S_1 - ON and Switch S_2 - OFF

$$\dot{x}(t) = A_2x(t) + B_2V_1(t) \quad (24)$$

Operating Mode 3:

Switches S_1 and S_2 - ON

$$\dot{x}(t) = A_3x(t) + B_3V_1(t) \quad (25)$$

Operating Mode 4:

Switch S_1 - OFF and Switch S_2 - ON

$$\dot{x}(t) = A_4x(t) + B_4V_1(t) \quad (26)$$

Where

$$A_1 = A_3 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{RC} \end{bmatrix} \quad (27)$$

$$A_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{L_2} \\ 0 & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \quad (28)$$

$$A_4 = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & 0 \\ \frac{1}{C} & 0 & -\frac{1}{RC} \end{bmatrix} \quad (29)$$

$$B_1 = B_2 = B_3 = B_4 \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix} \quad (30)$$

For the continuous conduction mode of operation, we have

$$K_1 = K_3 \quad (31)$$

$$K_2 = K_4 \quad (32)$$

$$K_1 + K_2 = 0.5 \quad (33)$$

$$K_1 + K_2 + K_3 = D \quad (34)$$

$$K_4 = 1 - K \quad (35)$$

$$K_2 = K_4 = 0.5 \quad (36)$$

$$K_1 = K_3 = 0 \quad (37)$$

$$A = A_1K_1 + A_2K_2 + A_3K_3 + A_4K_4 \quad (38)$$

$$B = B_1K_1 + B_2K_2 + B_3K_3 + B_4K_4 \quad (39)$$

$$C = [0 \quad 0 \quad 1] \quad (40)$$

$$D = 0 \quad (41)$$

Then Matrix A is

$$A = \begin{bmatrix} 0 & 0 & -\frac{K_2}{L_1} \\ 0 & 0 & -\frac{K_2}{L_2} \\ \frac{K_2}{C} & \frac{K_2}{C} & \frac{-2K_1-2K_2}{RC} \end{bmatrix} \quad (42)$$

$$B = \begin{bmatrix} \frac{2K_1+2K_2}{L_1} \\ \frac{2K_1+2K_2}{L_2} \\ 0 \end{bmatrix} \quad (43)$$

Using the matrices A and B, the transfer function is found as

$$G(S) = \frac{3.95e^7s+3.371e^{-9}}{s^3+118.4s^2+9.898e^6-3.311e^{-9}} \quad (44)$$

For the design of discrete PID controller, the continuous state equations are discretized. With the exception that discrete system is sampled with a sampling time estimated as $1\mu S$, it is treated identical to the continuous system.

6. Double frequency boost converter's closed loop system

DF boost converter incorporated with discrete PID controller is revealed in the figure 5. The target of this system is to follow the reference input signal by minimizing the error V_{err} between V_{ref} and V_o [13]. The output voltage is fed to the Analog to Digital converter. The feedback system controls the output voltage. Its function is to make sure that the output is steady, not affected by load disturbances and has good transient behavior which enhances the dynamic performance of the system. The digital compensator with PID control algorithm samples the error signal V_{err} with a sampling time equal to $1\mu S$ and generates a control signal. The sampled output is processed through the Digital Pulse Width Modulation block which is a demodulator comprised of sample and hold slab generates a gate signals to control the switch. The sample and hold slab incorporates a time delay (t_d), Analog to Digital conversion time, switch conversion time, computational delay and modulator delay.

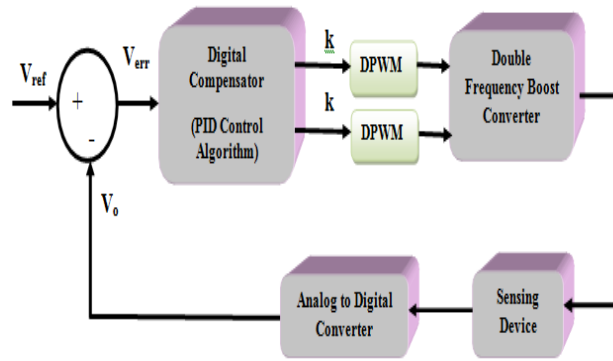


Figure 5. Closed loop control system using Digital controller

The block diagram of ADC is revealed in the figure 6. Continuous time signal to discrete time signal conversion takes place in this block using sampling and it comprises of delay block, Zero Order Hold (ZOH) block, quantizer block and saturation block. The function of the delay block is to estimate the total time between sampling the error voltage and upgrading the duty ratio at the start of next switching phase. The sampling effect is designed by ZOH. The purpose of the quantizer is to round off the values to smaller units of accuracy.

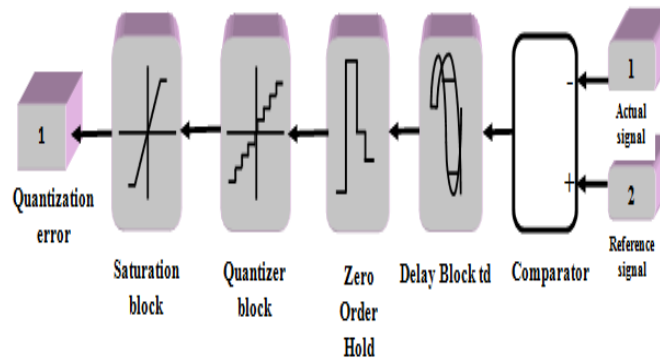


Figure 6. Analog to Digital Converter

The digital compensator block is shown in figure 7. The quantized error is fed to the discrete zero – pole which in turn is converted into gate pulses with the help of Digital Pulse Width Modulation (DPWM) blocks shown in figure 8. The digital compensator is modeled to reduce the error signal. It generates a PWM control pulses to the switches.

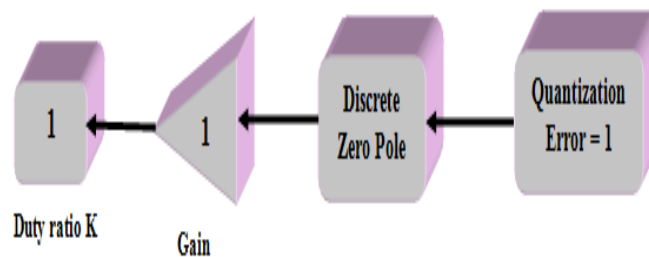


Figure 7. Digital Compensator

The compensator's output is correlated with one low frequency ramp signal to acquire the duty ratio for low frequency switch and also correlated with one high frequency ramp signal to acquire the duty ratio for the high frequency switch.

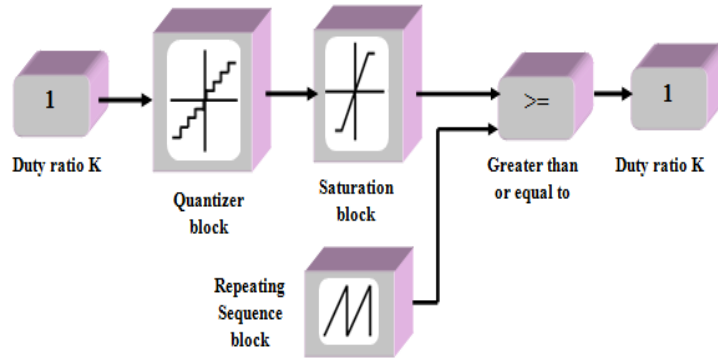


Figure 8. Digital pulse width modulation (DPWM)

7. Modeling of robust digital controller

A closed loop system of DF boost converter with a discrete PID controller is shown in figure 5. PID controller is superior to PI & PD controller. PI controller minimizes the steady state error (e_{ss}). PD controller enhances the stability of the system and enhances the bandwidth of the system.

$$u(t) = K_p e(t) + K_i \int_0^t e(t) dt + K_D \frac{d}{dt} e(t) \quad (45)$$

$$u(t) = K_p [e(t) + \frac{1}{T_I} \int_0^t e(t) dt + T_D \frac{d}{dt} e(t)] \quad (46)$$

Equations 45 and 46 denotes the expression for continuous time PID controller, where $u(t)$ is the output of the controller, K_p is a constant of proportional gain, T_D is a constant of derivative time or rate time, T_I is a constant of integral time or reset time and $e(t)$ is the error signal.

$$U(s) = K_p \left(1 + \frac{1+T_I T_D S^2}{T_I s} \right) E(s) \quad (47)$$

$$= K_p \left(1 + \frac{1}{T_I s} + T_D s \right) E(s) \quad (48)$$

Equations 47 and 48 give the expression for subsequent continuous time PID controller. The overall control action proportional to the error signal is provided by the proportional term. The steady state error is minimized by the integral part through low frequency compensation via integrator. The transient response of the system is improved by the derivative part through high frequency compensation via differentiator.

By choosing these tuning parameters aptly, a discrete PID controller can be designed for a definite converter. The range of K_p is found using Routh – array method and fix K_{cr} within K_p range. T_D and T_I values are calculated using Ziegler – Nichols tuning system [11]-[15] shown in the table 2, in which K_{CR} and P_{CR} is the critical gain and critical period respectively. Find the system's natural frequency (ω_o) after solving the characteristic equation and substituting $s = j\omega_o$ in equation and find T_D and T_I using the relation $P_{cr} = \frac{2\pi}{\omega_o}$ using the table 2.

$$1 + G(S)H(S) = 0 \quad (49)$$

Therefore,
 $S^3 + 118.4S^2 + 3.95E^1S + 9898000 + X = 0 \quad (50)$

Where X is the Stability range.

Table 2. Ziegler – Nicholas tuning method

CONTROLLER	K_p	T_I	T_D
P	0.5 k_{cr}	-	-
PI	0.45 k_{cr}	0.833 P_{cr}	-
PID	0.6 k_{cr}	0.5 P_{cr}	0.125 P_{cr}

The transfer function of the PID controller is

$$U(s) = \frac{G(s)}{K(s)} \quad (51)$$

$$U(S) = K_p + \frac{K_I}{S} + K_D S = \frac{K_D S^2 + K_P S + K_I}{S} \quad (52)$$

The uneven poles in the transfer function are eliminated by pole - zero deletion method is used. In this technique, the discrete PID controller equation is altered as

$$G(S) = \frac{K_D \left(S^2 + \frac{K_P}{K_D} S + \frac{K_I}{K_D} \right)}{S} \quad (53)$$

The closed loop transfer function is determined by

$$H(S) = \frac{1}{S^2 + 2\xi\omega_0 S + \omega_0^2} \quad (54)$$

$$\frac{K_I}{K_D} = \omega_0^2 \quad (55)$$

$$\frac{K_P}{K_D} = 2\xi\omega_0 \quad (56)$$

After that

$$G(S)H(S) = \frac{K_D}{S} \quad (57)$$

The settling time is given by

$$t_s \leq 1ms \quad (58)$$

The maximum peak overshoot is given by

$$M_p \leq 1\% \quad (59)$$

The closed – loop poles must rest within the unit circle for a stable system. The above condition has been satisfied by the values K_p , K_I , K_D and so the system is stable. The values of K_p , K_I , K_D , ω and ξ are 1, 0.18844812, $0.1326625 \cdot 10^{-3}$, 59.2 rad/sec and 0.9 correspondingly.

$$U(S) = \frac{V_o(S)}{K(S)} \quad (60)$$

$$= \frac{0.1326625 \cdot 10^{-3} (S^2 + 7537.925S + 1420.50783)}{S} \quad (61)$$

Equations 60 and 61 express the analog PID equation of the controller. Trapezoidal method (also called Bilinear – Transformation method) is used to transfer analog PID controller equation into discrete PID controller equation. This method is also named as Tustin method. Consider the Tustin method now. Let us assume $\int e(t) = s(t)$ and so the integral value of $t = (X+1) T$ is equal to the value at XT in addition with the area supplemented from XT to $(X+1) T$.

$$S [(X+1) T] = u (XT) + \int_{XT}^{(X+1)T} e(t) dt \quad (62)$$

Considering Tustin method, the area from $t = XT$ to $t = (X+1) T$ is $e(t)$ and is estimated as $\frac{e[(X+1)T] + e(XT)}{2} * T$ (63)

Hence

$$S \{(X+1)T = s(XT) + \frac{T}{2} \{e[(X+1)T] + e(XT)\} \} \quad (64)$$

z- Transform of (64) is given by (65)

$$Z S(z) = S(z) + \frac{T}{2} [zE(z) + E(z)]. \quad (65)$$

$$\frac{S(z)}{E(z)} = \frac{T}{2} \left[\frac{z+1}{z-1} \right] \quad (66)$$

Thus the transfer function of a discrete Integrator is given by equation 66. Let us assume $\frac{de(t)}{dt}$ at $t = XT = s(XT)$.

$$s(XT) = \frac{e(XT) - e[(X-1)T]}{T} \quad (67)$$

$$\frac{S(z)}{E(z)} = \frac{(z-1)}{Tz} \quad (68)$$

The z – Transform of equation 67 is taken to get the transfer function of a discrete differentiator equation 68. The block diagram of robust digital PID controller is shown in figure 9.

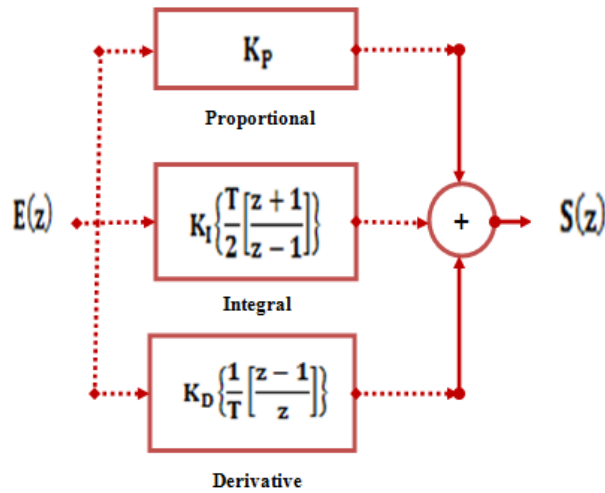


Figure 9. Robust digital pid controller

The transfer function of robust digital PID controller is given by equations 69 and 70.

$$G(z) = \frac{U(z)}{E(z)} \quad (69)$$

$$G(z) = \left[K_P + K_I \left\{ \frac{T}{2} \left(\frac{z+1}{z-1} \right) \right\} + K_D \left\{ \frac{z-1}{Tz} \right\} \right] \quad (70)$$

$$U(z) = \left[K_P + K_I \left\{ \frac{T}{2} \left(\frac{z+1}{z-1} \right) \right\} + K_D \left\{ \frac{z-1}{Tz} \right\} \right] E(z) \quad (71)$$

The robust discrete PID controller equation of double frequency boost converter is given by equation 72

$$U(z) = \frac{(z-0.9492)(z-0.9174)}{(z+1)(z-1)} \quad (72)$$

Table 3. Performance parameter comparison of various Boost converters

BOOST CONVERTER TYPES	RISE TIME (ms)	PEAK TIME (ms)	PEAK OVER-SHOOT (%)	SETTLING TIME (ms)	STEADY STATE ERROR (V)
DF Boost	0.5	1.11	62.5	21.4	0.04
HF Boost	0.6	1.15	61.58	27	0.05
LF Boost	1.8	3.4	78.7	97.4	0.08
Analog PID DF Boost	0.5	0.8	4	2	0.03
Discrete PID DF Boost	0.4	0.8	0	2	0.02

5. Simulation outcome

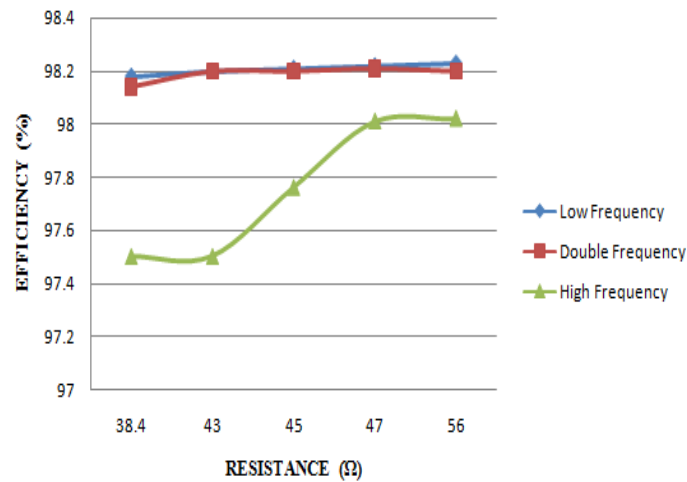


Figure 10. Efficiency Comparison Graph of High Frequency, Low Frequency & Double Frequency Boost Converter with Load Variation

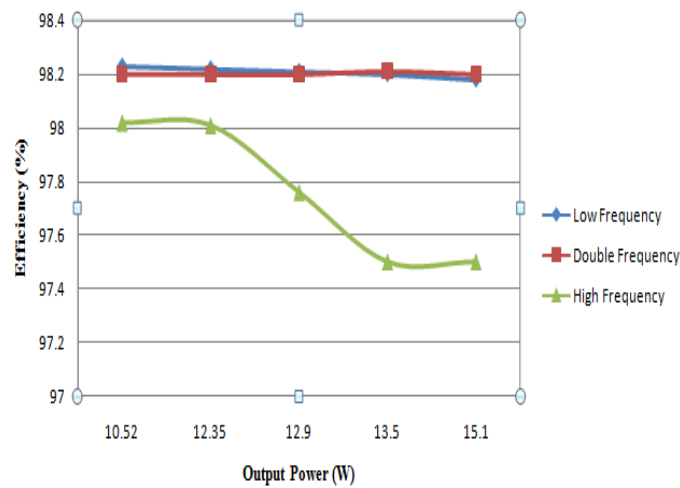


Figure 11. Efficiency Comparison Graph of High Frequency, Low Frequency, & Double Frequency Boost Converter with Output Power variation

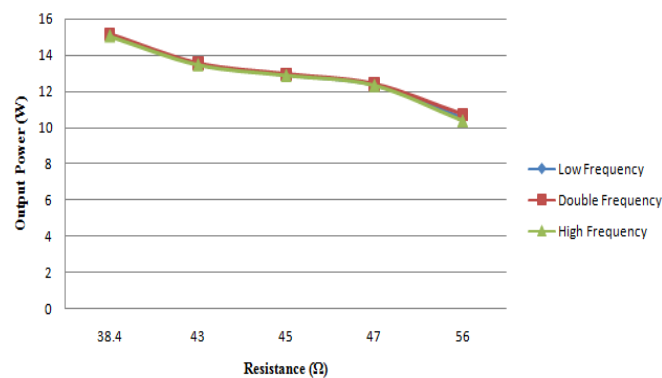


Figure 12. Output Power Comparison Graph of High Frequency, Low Frequency & Double Frequency Boost Converter with Load variation

It is evident from the efficiency comparison graphs of figure 10 and figure 11, that the high frequency Boost converter has efficiency lesser than the efficiency of other two Boost converters. The low frequency Boost converter and double frequency Boost converter have almost the same efficiency and from the output Power comparison graph of figure 12, the output Power of double frequency

Boost converter is higher than the output power low frequency and high frequency Boost converters. From the table 1 and table 3, it is clear that both the converter performance and efficiency is improved by the discrete PID controlled Double Frequency Boost Converter. Figure 13 shows the Simulation diagram for discrete PID controlled double frequency Boost converter.

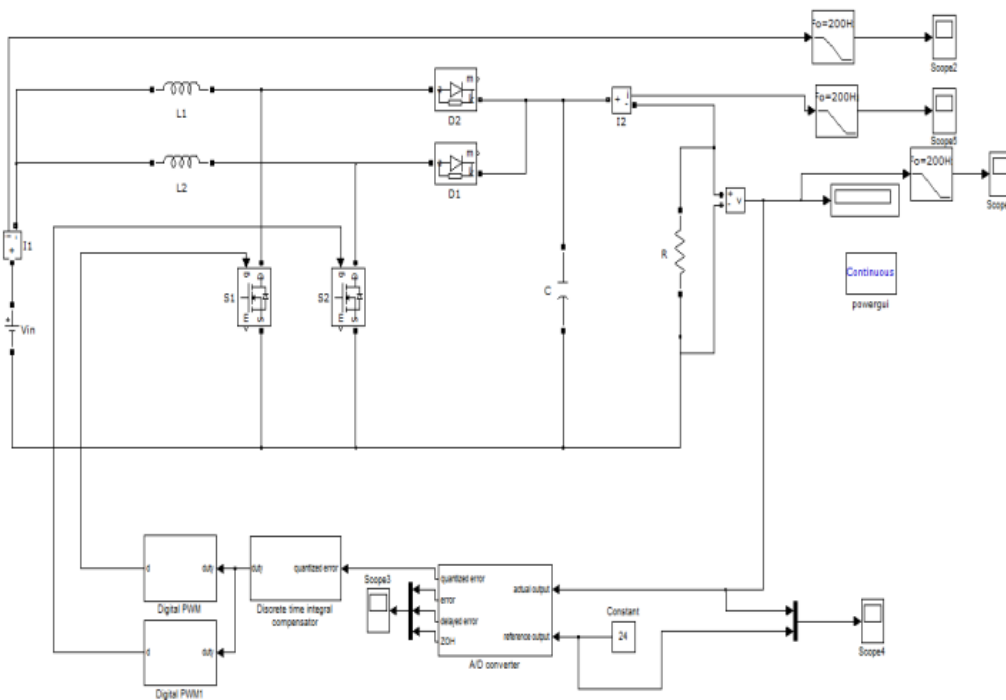


Figure 13. Simulation diagram for digital PID controlled double frequency Boost converter

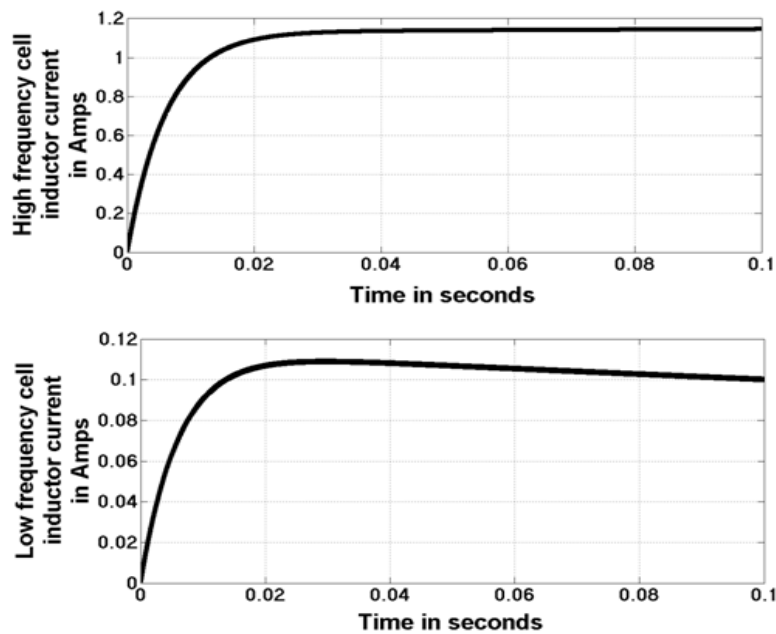


Figure 14. Waveforms of high frequency and low frequency cell inductor current for DF Boost converter

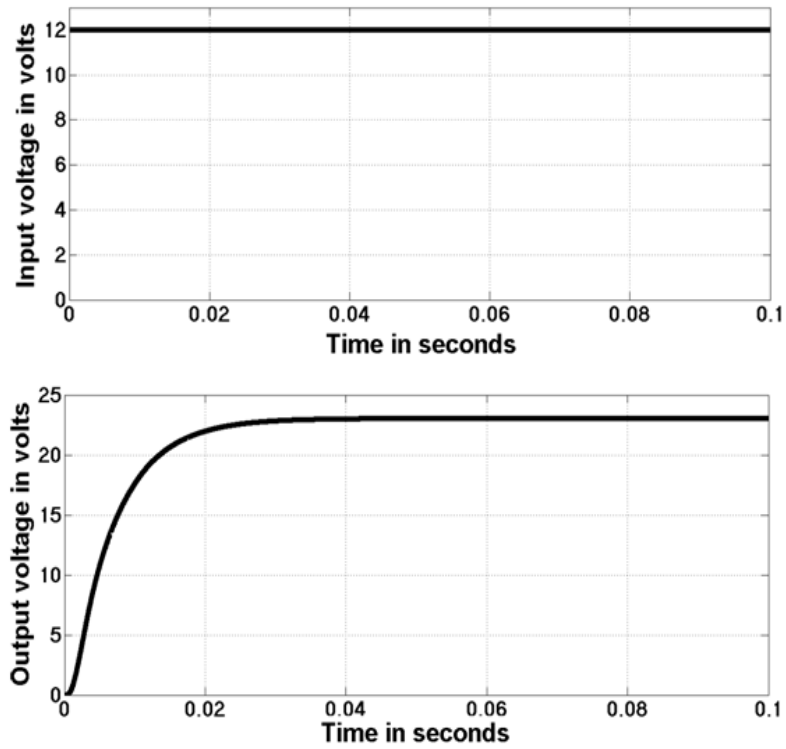


Figure 15 Waveforms of input voltage and output voltage of DF Boost converter

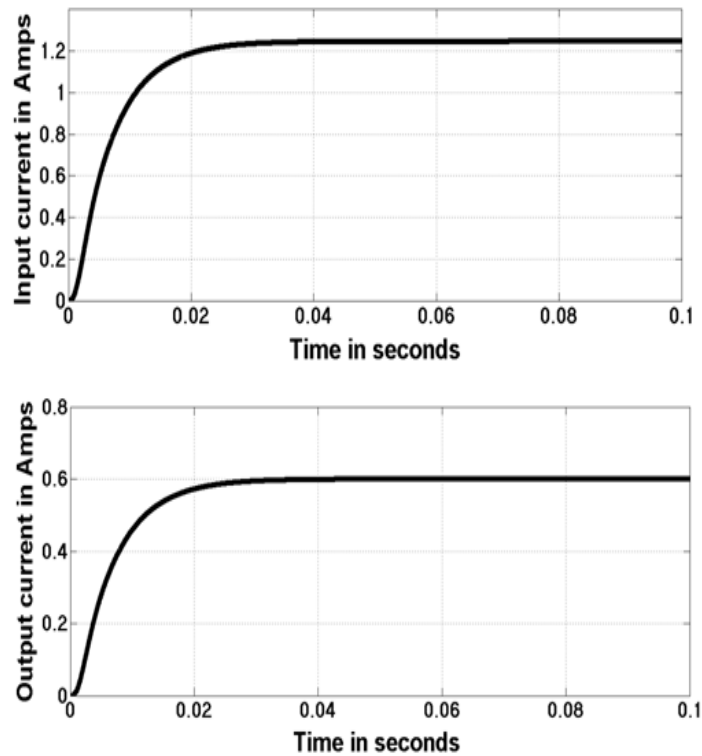


Figure 16. Waveforms of input current and output current of DF Boost converter

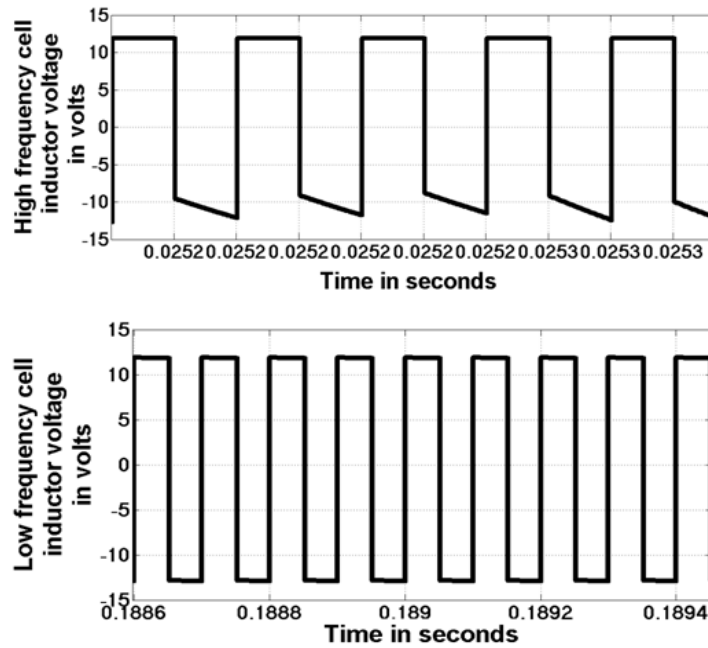


Figure 17. Waveforms of voltage across high frequency and low frequency cell inductor for DF Boost converter

The waveforms of high frequency and low frequency cell inductor current and waveforms of voltage across high frequency cell inductor and low frequency cell inductor for digital PID controlled DF boost converter are illustrated in Figure 14 and Figure 17 respectively. The waveforms of input current and output current for digital PID controlled DF boost converter is depicted in Figure 16. For an input voltage of 12V, the output voltage is 24V and corresponding waveforms are depicted in Figure 15. There is peak overshoot in the output voltage response.

9. Conclusion

A discrete PID controlled double frequency Boost converter has been designed and implemented in this paper. The performance parameter and efficiency comparison tables of various boost converters illustrate that DF Boost converter is the best choice. Also discrete PID controlled DF Boost converter has better dynamic performance with no maximum peak overshoot and less steady state error. In single frequency Boost converter, the switch carries the entire input current. Therefore a high rate switch is required and the current stress on the switch will be high. However, in DF Boost converter, the main input current is diverted in another path. Unlike the single frequency Boost converter, two low rate switches are enough to operate the converter. Correspondingly, the current stress on the switches is low. The digital PID controlled Double Frequency Boost converter produces a controlled output voltage, better dynamic response and superior efficiency. Future work will be on changing the resistive load to inductive load or motor load of the proposed discrete controlled converter and to enquire whether it is applicable for industrial applications.

10. Reference

- [1] Vijayalakshmi, Subramanian, and Thangasamy Sree Renga Raja. "Development of robust discrete controller for double frequency buck converter." *automatika* 56, no. 3 (2015): 303-317.
- [2] Hasaneen, B. M., and Adel A. Elbaset Mohammed. "Design and simulation of DC/DC boost converter." In *2008 12th International Middle-East Power System Conference*, pp. 335-340. IEEE, 2008.

- [3] Zhou, Luowei, Xiong Du, and Quanming Luo. "A novel buck converter topology with double frequency." In *2005 IEEE International Conference on Industrial Technology*, pp. 1069-1074. IEEE, 2005.
- [4] Newlin, D. Jeba Sundari, R. Ramalakshmi, and S. Rajasekaran. "A performance comparison of interleaved boost converter and conventional boost converter for renewable energy application." In *2013 International Conference on Green High Performance Computing (ICGHPC)*, pp. 1-6. IEEE, 2013.
- [5] Vijayalakshmi, S., E. Arthika, and G. Shanmuga Priya. "Modeling and simulation of interleaved Buck-boost converter with PID controller." In *2015 IEEE 9th International Conference on Intelligent Systems and Control (ISCO)*, pp. 1-6. IEEE, 2015.
- [6] Sarwar, Adil, Abdulla Shahid, Abdul Hudaif, Utkarsh Gupta, and Mohd Wahab. "Generalized state-space model for an n-phase interleaved buck-boost converter." In *2017 4th IEEE Uttar Pradesh section international conference on electrical, computer and electronics (UPCON)*, pp. 62-67. IEEE, 2017.
- [7] Vijayalakshmi, S., and Sree Renga T Raja. "Time domain based digital controller for buck-boost converter." *Journal of Electrical Engineering & Technology* 9, no. 5 (2014): 1551-1561.
- [8] Rahavi, JS Anu, T. Kanagapriya, and R. Seyezhai. "Design and analysis of interleaved boost converter for renewable energy source." In *2012 International Conference on Computing, Electronics and Electrical Technologies (ICCEET)*, pp. 447-451. IEEE, 2012.
- [9] Shanthi, N., P. Nivethitha, S. Sindhuja, M. Hilasini, and K. Divyabharathi. "High Efficient Interleaved Boost Converter for Photovoltaic Applications." In *2018 International Conference on Computation of Power, Energy, Information and Communication (ICCPEIC)*, pp. 305-309. IEEE, 2018.
- [10] Vijayalakshmi, Subramanian, Renga Raja, and Thangasamy Sree. "Time domain based Digital PWM controller for DC-DC converter." *Automatika: časopis za automatiku, mjerenje, elektroniku, računarstvo i komunikacije* 55, no. 4 (2014): 434-445.
- [11] Chander, Subhash, Pramod Agarwal, and Indra Gupta. "Auto-tuned, discrete PID controller for DC-DC converter for fast transient response." In *India International Conference on Power Electronics 2010 (IICPE2010)*, pp. 1-7. IEEE, 2011.
- [12] Du, Xiong, Luowei Zhou, and Heng-Ming Tai. "Double-frequency buck converter." *IEEE Transactions on industrial Electronics* 56, no. 5 (2009): 1690-1698.
- [13] Gayathiridevi, P., S. Vijayalakshmi, and K. R. Vairamani. "Discrete controller for high frequency buck converter." In *2013 International Conference on Circuits, Power and Computing Technologies (ICCPCT)*, pp. 605-610. IEEE, 2013.
- [14] Sivakumar, R., S. Ramprasath, and P. Ramesh Babu. "Efficiency and power packing density improvement for DC-DC boost converter by soft switching techniques." In *2015 International Conference on Circuits, Power and Computing Technologies [ICCPCT-2015]*, pp. 1-7. IEEE, 2015.
- [15] Malik, Prashant S., Sujay S. Gawas, Imran AltafPatel, Ninad P. Parsekar, Akshay A. Parab, and Shubham S. Parkar. "Transient Response Improvement of DC to DC Converter by Using Auto-tuned PID Controller." In *2018 Second International Conference on Inventive Communication and Computational Technologies (ICICCT)*, pp. 546-549. IEEE, 2018.