

FULL DUPLEX DOCSIS 4.0 DOWN STREAM SPECTRUM USAGE DESIGN

¹ S.Arun Prathap, ² S.R.Karthikeya, ²J.Mohamed Yunus, ² V.Yogeshwaran

¹ Assistant Professor, ² UG Students

Department of Electronics and Communication Engineering,
M.Kumarasamy College of Engineering, Karur, Tamilnadu

Abstract

A significantly versatile DOCSIS 4.0 building which is an improved advancement of DOCSIS 3.0 structure with flexible one of a kind extents of data. A Full Duplex DOCSIS innovation which applies developing procedures from remote systems to accomplish an achievement increment in the downstream speeds for DOCSIS conveyed broadband assistance. In current game plan the upper some part of the range is committed for downstream traffic. LMH2832 carefully controlled variable addition enhancer and ADS54J40 simple to-advanced converter is explicitly utilized in this structure procedure. A DOCSIS 4.0 Full Duplex system gives the pinnacle paces and adaptability of TDD arrangements, however one-ups both TDD and FDD with twofold the limit. These advancements are required to yield DOCSIS 4.0 system execution of up to 10 Gbps balanced on 1 GHz HFC systems, with the potential for significantly better by using range that is at present accessible for future extension over 1 GHz. In view of our system, the circuit is executed on the PCB board utilizing Mentor Graphics Expedition Tool.

I. INTRODUCTION

Ultra-quick download speeds, when a dream, are presently a reality from your link supplier, because of the new leap DOCSIS 4.0 innovation

DOCSIS is an innovation created for move of information over coaxial link that are conveyed and utilized for satellite TV association. Link administrators over the world have embraced DOCSIS norms for giving web information, voice and video administrations utilizing existing digital TV frameworks.

One of the key focal points of DOCSIS 4.0 over Fiber is that it utilizes the equivalent 'last mile' innovation to help the higher Gigabit speeds. Fiber requires a totally new foundation and new link formats to the home. DOCSIS 4.0 innovation is a substantially more savvy innovation for satellite internet services to actualize.

DOCSIS 4.0 offers an immense bounce in download and transfer web speeds, supporting up to 10 Gbps download and 1 Gbps transfer speeds. Utilizing DOCSIS 4.0, Comcast is offering Gigabit and Gigabit Pro Internet administration with 1 and 2 Gigabit download speeds. As DOCSIS 4.0 is in reverse perfect with DOCSIS 3.1, administrators are as yet utilizing DOCSIS 3.0 for upstream association.

DOCSIS 4.0 characterizes new testament based security includes that reinforce security of link modem verification and secure programming download to the modem. Improved security includes further decrease the danger of malevolent firmware being stacked on the link modem.

DOCSIS 4.0 backings improved bundle queueing systems

over the link arrange. Decreased inertness improves voice quality for VoIP calls and improves web based gaming experience by limiting the likelihood of web based game play.

That will enable link administrators to take advantage of 600MHz of extra usable range and dig greater limit with regards to different DOCSIS-based private and business administrations, including rapid Internet, IP video and remote backhaul.

Individuals acquainted with the 4.0 exertion accept that the greater part of the new specs could be wrapped before the finish of 2019 (given that a significant part of the specs for FDX and Low Latency DOCSIS are well downstream), and that the plant-related work for Extended Spectrum DOCSIS (to 1.8GHz) should be possible before mid-2020. That could make way for items that help the full 4.0 specs to rise in 2021.

DOCSIS 4.0 is as yet advancing, yet as per Light Reading, the following update will completely bolster Full Duplex DOCSIS, enabling clients to get the equivalent transfer speed as their download speed, and will completely actualize Low Latency DOCSIS which could lessen traffic deferrals to under 1 milli second.

II. PCB OVERVIEW

A Printed Circuit Board (Pcb) Mechanically Supports And Electrically Interfaces Electronic Parts Utilizing Conductive Tracks, Cushions And Different Highlights Scratched From Copper Sheets Overlaid Onto A Non-Conductive Substrate. Parts – Capacitors, Resistors Or Dynamic Gadgets – Are For The Most Part Fastened On The Pcb. Progressed Pcb's May Contain Segments Implanted In The Substrate.

Pcb's Can Be Single Sided (One Copper Layer), Two Sided (Two Copper Layers) Or Multi-Layer (External And Inward Layers). Conductors On Various Layers Are Associated With Vias. Multi-Layer Pcb's Tak Into Account A Lot Higher Segment Thickness.

Fr-4 Glass Epoxy Is The Essential Protecting Substrate. A Fundamental Structure Square Of The Pcb Is A Fr-4 Board With A Slim Layer Of Copper Foil Overlaid To One Or The Two Sides. In Multi-Layer Sheets Different Layers Of Material Are Overlaid Together.

Printed Circuit Sheets Are Utilized In Everything Except The Most Straightforward Electronic Items. Pcb's Require The Extra Plan Exertion To Spread Out The Circuit, However Assembling And Get Together Can Be Mechanized. Assembling Circuits With Pcb's Is Less Expensive And

Quicker Than With Other Wiring Techniques As Segments Are Mounted And Set Up With One Single Part.

III. PCB Characteristics

Circuit Properties Of PCB

The resistance, determined by width and thickness, of the traces must be sufficiently low for the current where the conductor will carry. For microwave circuits, transmission lines can be laid out in the form of strip line and microstrip with carefully controlled dimensions to assure a consistent impedance.

- Copper Traces Of PCB
- Different types of Vias are used in designing in PCB. They are Through hole Via, Blind Via, Buried Via.
 - Through hole Via
 - Blind Via
 - Buried Via
- Steps Involved In Designing Process
- BILL OF MATERIALS
- REFERENCE DESIGNATOR

- PART NUMBER
- DATASHEET
- FOOT PRINT CREATION
- PAD CREATION
- There are two types to create the pad
- SMD
- THROUGH HOLE
- CELL CREATION
- PART MAPPING
- PIN MAPPING
- SCHEMATIC CREATION
- BOARD OUTLINE
- LAYER STACK-UP
- PACKAGING
- CONSTRAINT SET UP
- PLACEMENT
- ROUTING
- ROUTING CLEAN UP
- PLANE CREATION
- Post Process
- SOLDER MASK
- SILKSCREEN
- ASSEMBLY
- SOLDER PASTE
- Arrange all reference designator legibly in silkscreen layer
- Bottom silkscreen text need to be mirrored.
- Silkscreen ref des should not fall on via and fiducial
- Save the board file with with proper name.
- ASPR-Assembly Primary
- ASSR-Assembly Secondary
- FAB-FABRICATION Layer
- L1-Top Layer
- L2-Power Layer
- L3-Ground Layer
- L4-Bottom Layer
- SLPR-Silkscreen Primary
- SLSE- Silkscreen Secondary
- SPPR-Solder Paste Primary
- SPSE- Solder Paste Secondary
- SMPR-Solder Mask Primary
- SMSE- Solder Mask Secondary
- NC DRILL

- GERBER GENERATION
- GERBER OUTPUT
- GERBER VALIDATION

PCB Design Tool

Many tools are available for PCB design. Such as

- Altium Designer.
- Autodesk EAGLE.
- KiCad EDA.
- SolidWorks PCB.
- Express PCB Plus.
- OrCAD Capture.
- Mentor graphics Xpedition tool.

Xpedition Tool

Xpedition Designer gives a total schematic plan answer for structure creation, definition, and reuse. It gives everything expected to circuit structure and reenactment, part choice, library the board and sign honesty arranging in a simultaneous group based plan condition. The incorporated work area empowers building groups to play out each key structure creation task in a solitary, adaptable, simultaneous and constant cooperation condition.

Advantage

- It is more powerful and high speed to design a complex boards.
- This tools are used to make product design

Disadvantage

- This tool is very difficult to learn.
- This tool's cost is high.
- Equations
- Design Process

Create System Specification

The starting advance of any PCB produce is, obviously, the structure. PCB assembling and configuration consistently start with an arrangement the architect spreads out a plan for the PCB that satisfies every one of the prerequisites as laid out. After every one of the checks are finished, the PCB configuration can be printed. Dissimilar to other plans, as engineering drawings, PCB plans don't print out on an ordinary 8.5 x 11 sheet of paper. Rather, a unique sort of printer, known as a plotter printer, is utilized. A plotter printer makes a "film" of the PCB. The last result of this "film" looks a lot of like the transparencies that used to be utilized in schools — it's basically a photograph negative of the board itself.

Within layers of the PCB are spoken to in two ink hues:

- Black Ink: Used for the copper follows and circuits of the PCB
- Clear Ink: Denotes the non-conductive territories of the PCB, similar to the fiberglass base

On the external layers of the PCB structure, this pattern is turned around — clear ink alludes to the line of copper pathways, however dark ink additionally alludes to territories where copper will be evacuated.

A. Select PCB Board Type

Each PCB layer and the going with patch cover gets its own film, so a straightforward two-layer PCB needs four sheets - one for each layer and one each for the going with weld veil.

After the film is printed, they're arranged and an opening, known as an enlistment gap, is punched through them. The enrollment opening is utilized as manual for adjust the movies later on all the while.

B. Data Management

PCB Artist is provided with a lot of libraries. These libraries can be utilized, altered and added to as required. You can blend and match new and existing library things together to make your very own arrangement of one of a kind libraries. The following barely any sections focus on kicking you off with making your very own libraries. After the keep going part on planning Components, there is more insight regarding how to utilize the Library Manager.

C. Design Entry

A schematic is a circuit chart. It utilizes concurred images to speak to parts and shows how they are electrically associated. A PCB configuration shows the copper track and opening format of a printed circuit board and ordinarily demonstrates the area of parts and their qualities/codes with a silk screen printed layer.

D. Layout Design

The PCB format and configuration is a pro aptitude requiring information on not just of the PCB structure programming and PCB CAD framework, yet additionally an assortment of models and methods used to guarantee that the essential circuit configuration is effectively moved to a general printed circuit board.

E. Gerber File Generation

The Gerber position is an open ASCII vector group for printed circuit board (PCB) structures. It is the accepted standard utilized by PCB industry programming to depict the printed circuit board pictures: copper layers, patch veil, legend, drill information, and so forth.

F. Silk Screen

Silkscreen is a layer of ink follows used to recognize segments, test focuses, portions of the PCB, notice images, logos and imprints and so forth. This silkscreen is normally applied on the part side; anyway utilizing silkscreen on the bind side is likewise normal. Be that as it may, this may expand the expense. Basically a nitty gritty PCB silkscreen can help both the maker and the architect to find and recognize every one of the segments.

Red Colour

Red patch veil shading will in general be striking and expert. The difference present between planes, spaces and follows are very acceptable. On the as opposed to the green printed circuit board, the difference is lower. Any amplification is utilized for assessing the board follows in the event of imperfections. In spite of the fact that red looks alluring, eye-getting and striking, green is as yet thought about the best.

Blue Colour

If there should arise an occurrence of blue bind cover shading, amplification is viewed as essential and is required for investigating the deformities of manufacturing. However, it is to be noticed that the differentiation between the patch veil and silkscreen is very high that is the in addition to point for utilizing blue shading.

Black Colour

Powerful amplification is required for the review of this board. Investigating it is simply a bad dream as it needs a tilted plot for throwing shadow to discover follows. Another issue with dark PCB shading is its warmth ingestion during the procedure of reflow.

Green Colour

A 'green' printed circuit board isn't really green completely through. The main green part is the external covering of tar called the weld veil or patch oppose/oil. This is a solidified tar with hued shades that is applied to the sheets in a silkscreen design. The reason for bind cover is to shield the electronic follows underneath from dampness and dust and to control the progression of liquid patch.

Design Tools

Computer based tools have evolved to automate or improve the speed and accuracy of every step in the process these tools are divided into three major groupings based on where they are used:

- CAE(Computer-Aided Engineering)
- CAD(Computer-Aided Design)
- CAM(Computer-Aided Manufacturing)

CAE-CAD is used to refer the computer-based tools and systems that are employed in the stages of design before the physical layout step or to analyse and evaluate the electrical performance of the final physical layout.

CAD-CAD tools are used to turn the electrical circuit described by the schematic into a physical package or PCB.

CAM-CAM tools are CAD Systems tailored to the needs of the fabrication process. The output of the PCB design process is a set of CAD files that describes each artwork layer of a PCB, the silkscreen, drilling requirements and netlist information. Gerber file is created with the extension of .gbr.

IV. Proposed System

Block Diagram

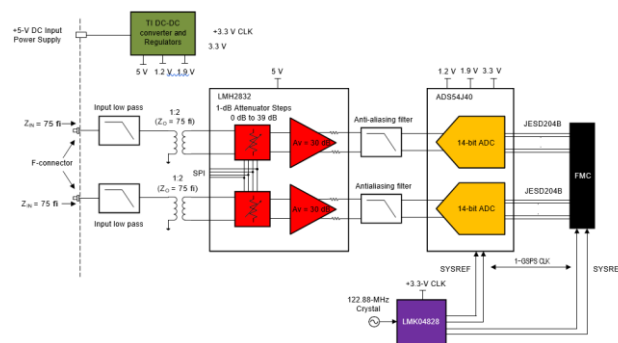


Fig-1: System-Level Block Diagram

Description

This reference design consists of an analog front-end (AFE) signal chain for wideband receiver applications using the LMH2832 digitally-controlled variable gain amplifier and ADS54J40 analog-to-digital converter. The design is primarily targeted for upstream DOCSIS 4.0 receiver applications specified for cable modem termination systems (CMTS) and supports up to 196 MHz of upstream signal bandwidth. The circuit solves the filtering and analog signal processing requirements for the DOCSIS 4.0 standard, which makes easier.

System Description

The TIDA-01378 reference configuration principally comprises of a simple front-end (AFE) signal chain utilizing a carefully controlled variable increase enhancer (LMH2832) and a simple to-computerized converter (ADS54J40) for upstream DOCSIS 4.0 CMTS beneficiary applications. This guide tends to significant parameters, for example, the framework signal proportion (SNR) and misleading free powerful range (SFDR) execution to help in the framework plan.

LMH2832

The LMH2832 is a high-linearity, double channel, computerized variable-gain intensifier (DVGA) for rapid sign chain and information obtaining frameworks. The LMH2832 is improved to give high data transfer capacity, low bending, and low commotion, along these lines making the gadget undeniably fit as a double, 14-piece, simple to-computerized converter (ADC) driver.

Key highlights of the gadget include:

- –3-dB transmission capacity of 1.1 GHz at greatest addition
- Individual channel, sequential fringe interface (SPI)- controlled increase programmable from 30 dB to – 9 dB in 1-dB attenuator steps
- Output third-request block point (OIP3) of 51 dBm at 200 MHz
- Noise figure of 6.5 dB (most extreme increase) at 300 MHz for $Z_{IN} = 150 \Omega$
- Single 5-V supply activity with customizable force utilization of 90 mA to 108 mA for every channel

ADS54J40

The ADS54J40 is a low-power, wide-data transfer capacity, 14-piece, 1.0-GSPS, double channel, simple to-computerized converter (ADC). Key highlights of the gadget include:

- 14-bit goals, double channel, 1-GSPS ADC
- Noise floor: – 158 dBFS/Hz
- spectral execution ($f_{IN} = 170$ MHz at – 1 dBFS):
 - SNR: 69.0 dBFS
 - NSD: – 155.9 dBFS/Hz
 - SFDR: 86 dBc
 - SFDR: 89 dBc (with the exception of HD2, HD3, and interleaving tones)
- Input 3-dB data transmission of 1.2GHz
- JESD204B interface with subclass-1 help for two or four paths for each ADC at 10.0 Gbps or 5.0 Gbps, separately

LMK04828

The LMK04828 is a ultra-low-clamor JESD204B-consistent clock-jitter cleaner with double circle stage bolted circles (PLLs) that produces the 1-GHz input clock sign to the ADC utilizing a 122.88-MHz precious stone oscillator. This gadget likewise produces the SYSREF signal, which alongside the clock signal, is utilized to appropriately synchronize the JESD204B computerized yields originating from the ADC to the Virtex field-programmable entryway cluster (FPGA).

System Design Theory

The information channel is trailed by a 1:2 ($ZO = 75 \Omega$) impedance transformer that matches the single-finished $75-\Omega$ contribution with the $150-\Omega$ differential info impedance of the DVGA (LMH2832). This application utilizes a transformer with a base level band reaction of up to 270 MHz and furthermore gives DC segregation between the RF coaxial info and the DVGA basic mode input voltages. The 1:2 impedance proportion of the transformer makes a voltage addition of roughly 3 dB.

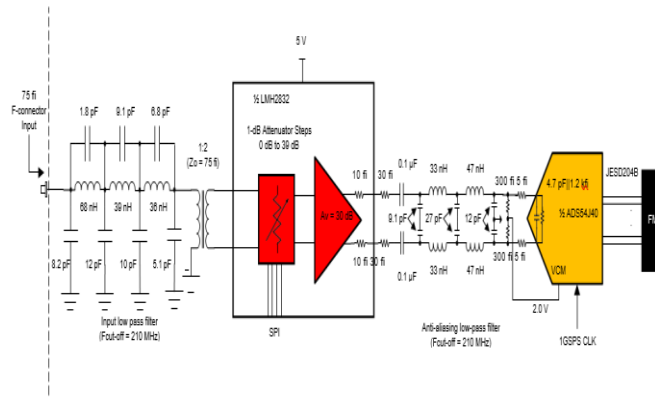


Fig-2: Front End Block Diagram

The DVGA (LMH2832) works in a programmed increase control (AGC) circle in order to keep up consistent sign force going into the ADC. The DVGA design comprises of 39 stages of a 1-dB stepping stool attenuator followed by a 30-dB voltage-increase fixed-gain intensifier. The gadget displays a generally steady commotion figure (NF) for the initial 4-dB attenuator ventures with the NF corrupting relative to the fifth attenuator step, in this way giving a powerful range upgrades. Low twisting and with more noteworthy than 300 MHz of working recurrence make the LMH2832 a perfect contender for DOCSIS 4.0 applications.

Following the DVGA, an antialiasing channel smothers the out-of-band commotion and music created by the sign intensification of the DVGA. The antialiasing channel has a fifth-request low-pass trademark with a cut off recurrence of 210 MHz.

The interface between the DVGA and the ADC is AC-coupled, which separates the DVGA yield normal mode (CM) voltage and the ADC input CM voltage.

Input Filter Characteristics

The thin division (of ~54 MHz) between the upstream band and the downstream band requires the stop-band lessening to be sharp after the upstream band cut off recurrence ($f_0 = 204$ MHz). This limited division likewise requires accomplishing more noteworthy than 40 dB of stop-band lessening to maintain a strategic distance from any downstream prods from associating with the upstream groups. Thus, the info channel chose is a 75- Ω , single-finished, seventh-request, Cauer-Chebyshev low-pass channel. Likewise, to keep away from any sign reflections because of long coaxial links, the arrival misfortune necessity for a 75- Ω input must be more noteworthy than 12 dB. Figure 4 shows the recreated return misfortune (S11) and forward-move work (S21) of the info channel.

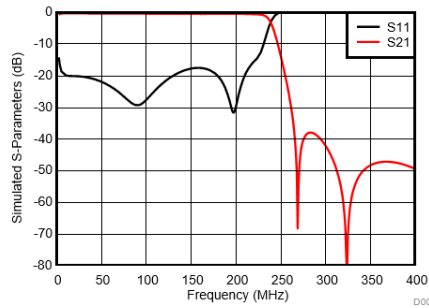


Fig -3: Simulated Input Filter Transfer Function

Hardware

A low-clamor signal generator is utilized to produce the necessary single-tone signal. A band-pass channel is utilized to smother the sign generator sounds from the info sign and drives the BMP5075 gadget, which is a 50- Ω to 75- Ω impedance-transformation cushion. The 75- Ω side of the BMP5075 gadget is associated with the F-connector contribution of the TSW54J40 assessment module (EVM).

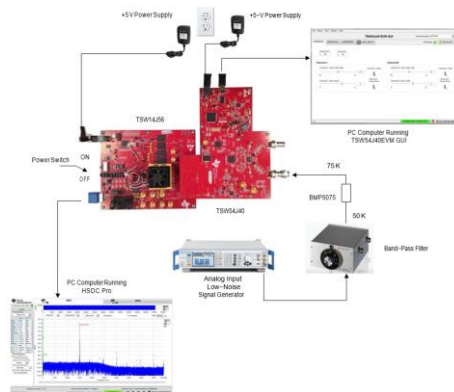


Fig -4: Hardware Setup Diagram

Software

The TSW54Jxx graphical UI (GUI) is utilized to design the installed DVGA (LMH2832) and the ADC (ADS54J40). The TSW54Jxx GUI programming is like the ADS54J40 EVM GUI programming with the exception

of an additional tab to program the LMH2832 gadget gain. Follow the means for programming the ADC and check in the ADS54J40EVM client's guide [1].

The HSDC Pro programming is utilized to investigate the computerized information caught by the TSW14J56 EVM. Allude to the

Fast Data Converter Pro Software device organizer for a definite depiction on the most proficient method to utilize the GUI.

V. Conclusion

Testing and Results

The accompanying diagrams and HSDC Pro screen captures show the deliberate outcomes utilizing the TSW54J40 EVM. The equipment test arrangement for these outcomes is appeared in the previous Figure 4. The run of the mill conditions for the test are: a 5-V ostensible divider mount power supply, input clock inspecting pace of 983.04 MSPS, ostensible room temperature (25°C).

The two-tone tests are at -7-dB full-scale for each tone at the ADC focused at ± 1 MHz from the central tone (f_0).

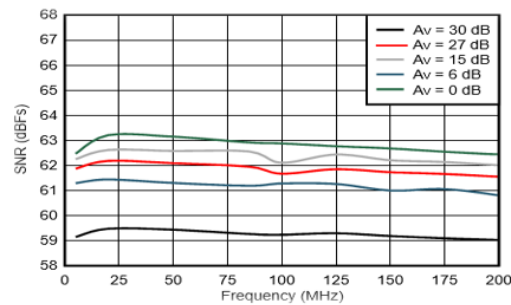


Fig -5: SNR versus Frequency

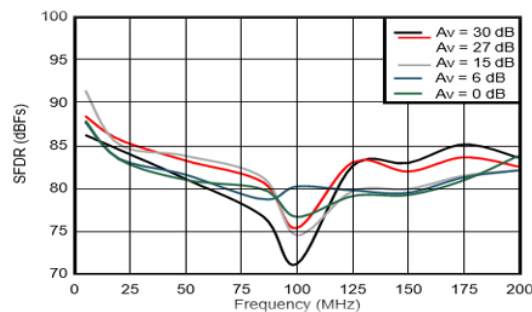


Fig-6: SFDR versus Frequency

Output Layers:

In patch mount, the layer which are at the highest point of PCB where are mounted called top layer.

In through opening where the segments are bound, this layer is called base layer

The size or state of any part is characterized on the highest point of PCB, through layer called gathering top.

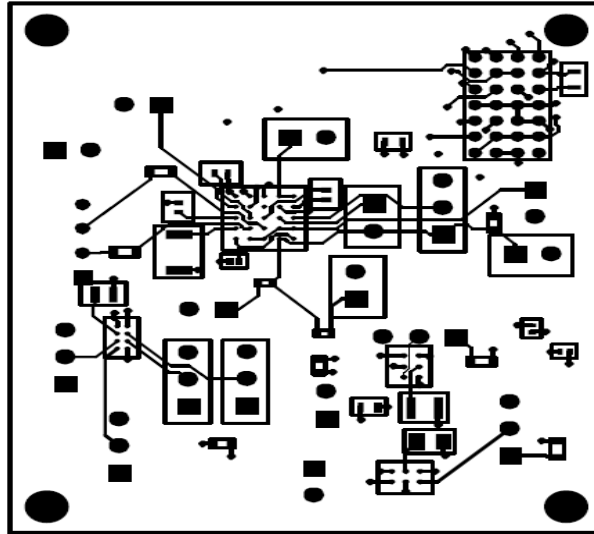


Fig -7: Bottom Layer

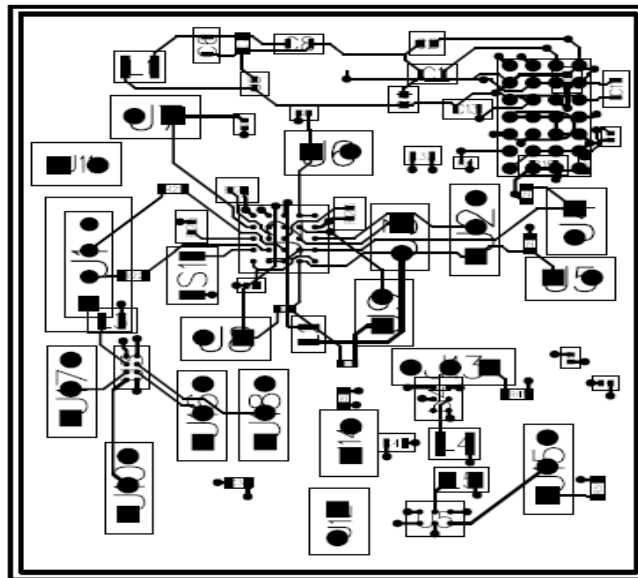


Fig -8: Placement Layer

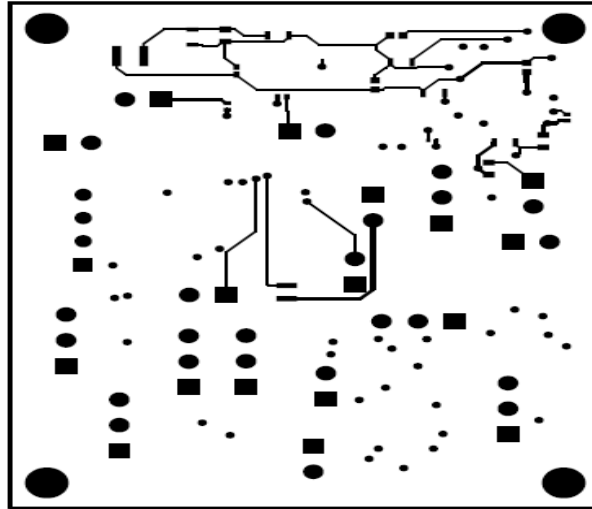


Fig -9: Top Layer

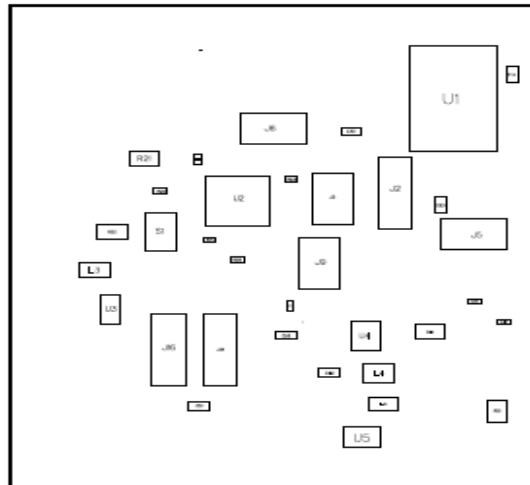


Fig -10: ASSEMBLY TOP

REFERENCES

1. T.Abirami, Dr.S.Palanivel Rajan, "Detection of poly cystic ovarian syndrome (PCOS) using follicle recognition techniques", Bioscience Biotechnology Research Communications, ISSN: 0974-6455, Vol. 12, Issue : 01, pp. 1-4, DOI: 10.21786/bbrc/12.1/19, 2019.
2. Dr.S.Palanivel Rajan, "Enrichment of ECG Quality using Independent Component Analysis for Dynamic Scenario by Eliminating EMG Artifacts", Advances and Applications in Mathematical Sciences, ISSN No.: 0974-6803, Vol. No.: 18, Issue : 2, pp. 219-237, 2018.

3. Dr.S.Palanivel Rajan, S.Suganya, “Design of Loop Antenna for the Human Brain Signal Analysis”, Indian Journal of Science and Technology, Online ISSN No.: 0974-5645, Print ISSN No.: 0974-6846, Vol. No.: 11, Issue: 10, pp. 1-6, DOI: 10.17485/ijst/2018/v11i10/120829, 2018.
4. M.Paranthaman, Dr.S.Palanivel Rajan, “Design of E and U Shaped Slot for ISM Band Application”, Indian Journal of Science and Technology, Online ISSN No.: 0974-5645, Print ISSN No.: 0974-6846, Vol.: 11, Issue: 18, pp. 1-3, DOI: 10.17485/ijst/2018/v11i18/123042 2018.
5. C.Vivek, S.Palanivel Rajan, “Z-TCAM : An Efficient Memory Architecture Based TCAM”, Asian Journal of Information Technology, ISSN No.: 1682-3915, Vol. No.: 15, Issue : 3, pp. 448-454, DOI: 10.3923/ajit.2016.448.454, 2016.
6. S.Vijayprasath, R.Sukanesh, S.Palanivel Rajan, “Assessment of relationship between heart rate variability and drowsiness of post operative patients in driving conditions”, JoKULL Journal, ISSN No.: 0449-0576, Vol. 63, Issue 11, pp. 107 – 121, 2013.
7. Paranthaman, M., and S. Palanivel Rajan. "Design of Triple C shaped Slot Antenna for Implantable Gadgets." Current Trends In Biomedical Communication And Tele–Medicine (2018): 40. DOI: 10.21786/bbrc/11.2/6
8. S.Palanivel Rajan, R.Sukanesh, S.Vijayprasath, “[Design and Development of](#) Mobile Based Smart Tele-Health Care System for Remote Patients”, European Journal of Scientific Research, ISSN No.: 1450-216X/1450-202X, Vol. No. 70, Issue 1, pp. 148-158, 2012.
9. M. Paranthaman, "T-shape polarization reconfigurable patch antenna for cognitive radio," 2017 Third International Conference on Science Technology Engineering & Management (ICONSTEM), Chennai, 2017, pp. 927-929. doi: 10.1109/ICONSTEM.2017.8261338
10. S.Palanivel Rajan, R.Sukanesh, S.Vijayprasath, “Analysis and Effective Implementation of Mobile Based Tele-Alert System for Enhancing Remote Health-Care Scenario”, HealthMED Journal, ISSN No. : 1840-2291, Vol. No. 6, Issue No. 7, pp. 2370–2377, 2012
11. M.Annakamatchi, V.Keralshalini," Design of Spiral Shaped Patch Antenna for Bio-Medical Applications", International Journal of Pure and Applied Mathematics , Online ISSN No.: 1314-3395,Print ISSN No.:1311-8080 ,Vol. No.:118, Issue No.:11,pp.131-135,2018.
12. S.Palanivel Rajan, “A Significant and Vital Glance on “Stress and Fitness Monitoring Embedded on a Modern Telematics Platform”, Telemedicine and e-Health Journal, Vol.20, Issue 8, pp.757-758, 2014.

13. S.Palanivel Rajan, T.Dinesh, "Systematic Review on Wearable Driver Vigilance System with Future Research Directions", International Journal of Applied Engineering Research, Vol. 2, Issue 2, pp.627-632, 2015.
14. S.Palanivel Rajan, S.Vijayprasath, "Performance Investigation of an Implicit Instrumentation Tool for Deadened Patients Using Common Eye Developments as a Paradigm", International Journal of Applied Engineering Research, Vol.10, Issue 1, pp.925-929, 2015.
15. M.Manikandan,N.V.Andrews, V.Kavitha, "Investigation On Micro Calification Of Breast Cancer From Mammogram Image Sequence" International Journal of Pure and Applied Mathematics, Online ISSN No.: 1314-3395, Print ISSN No.: 1311-8080, Vol. No.: 118, Issue No.: 20, pp. 645-649,2018.
16. S.Palanivel Rajan, T.Dinesh, "Statistical Investigation of EEG Based Abnormal Fatigue Detection using LabVIEW", ", International Journal of Applied Engineering Research, Vol. 10, Issue 43, pp. 30426-30431, 2015.
17. L. RAMESH, T.ABIRAMI, "Segmentation of Liver Images Based on Optimization Method", International Journal of Pure and Applied Mathematics, Online ISSN No.: 1314-3395, Print ISSN No.: 1311-8080, Vol. No.: 118, Issue No.: 8, pp. 401-405, 2018.
18. S.Palanivel Rajan, V.Kavitha, "Diagnosis of Cardiovascular Diseases using Retinal Images through Vessel Segmentation Graph", Online ISSN No.: 1875-6603, Print ISSN No.: 1573-4056, Vol. No.: 13, Issue : 4, pp. 454-459, DOI : 10.2174/1573405613666170111153207, 2017.
19. S Mohanapriya, M Vadivel, "Automatic retrieval of MRI brain image using multiqueries system", 2013 International Conference on Information Communication and Embedded Systems, INSPEC Accession Number: 13485254, Electronic ISBN: 978-1-4673-5788-3, DOI: 10.1109/ICICES.2013.6508214, pp. 1099-1103, 2013.
20. S.Palanivel Rajan, "Review and Investigations on Future Research Directions of Mobile Based Tele care System for Cardiac Surveillance", Journal of Applied Research and Technology, Vol.13, Issue 4, pp.454-460, 2015.
21. S.Palanivel Rajan, R.Sukanesh, "Experimental Studies on Intelligent, Wearable and Automated Wireless Mobile Tele-Alert System for Continuous Cardiac Surveillance", Journal of Applied Research and Technology, ISSN No.: 1665-6423, Vol. No. 11, Issue No.: 1, pp.133-143, 2013
22. S.Palanivel Rajan, R.Sukanesh, "Viable Investigations and Real Time Recitation of Enhanced ECG Based Cardiac Tele-Monitoring System for Home-Care Applications: A Systematic Evaluation", Telemedicine and e-Health Journal, ISSN: 1530-5627, Online ISSN: 1556-3669, Vol. No.: 19, Issue No.: 4, pp. 278-286, 2013.

23. M.Paranthaman, S.Palanivel Rajan, “Design of H Shaped Patch Antenna for Biomedical Devices”, International Journal of Recent Technology and Engineering, ISSN : 2277-3878, Vol. No. 7, Issue:6S4, pp. 540-542, Retrieval No.: F11120476S4/19©BEIESP, 2019.
24. S.Palanivel Rajan, et.al., “Intelligent Wireless Mobile Patient Monitoring System”, IEEE Digital Library Xplore, ISBN No. 978-1-4244-7769-2, INSPEC Accession Number: 11745297, IEEE Catalog Number: CFP1044K-ART, pp. 540-543, 2010.
25. S.Palanivel Rajan, et.al., “Cellular Phone based Biomedical System for Health Care”, IEEE Digital Library Xplore, ISBN No. 978-1-4244-7769-2, INSPEC Accession Number: 11745436, IEEE Catalog Number: CFP1044K-ART, pp.550-553, 2010.
26. S.Palanivel Rajan, et.al., “Performance Evaluation of Mobile Phone Radiation Minimization through Characteristic Impedance Measurement for Health-Care Applications”, IEEE Digital Library Xplore, ISBN : 978-1-4673-2047-4, IEEE Catalog Number: CFP1221T-CDR, 2012.
27. M.Paranthaman, S.Palanivel Rajan, “Design of Implantable Antenna for Biomedical Applications”, International Journal of Advanced Science and Technology, P-ISSN: 2005-4238, E-ISSN: 2207-6360, Vol. No.: 28, Issue No. 17, pp. 85-90, 2019.
28. S.Palanivel Rajan, et.al., “Experimental Explorations on EOG Signal Processing for Real Time Applications in LabVIEW”, IEEE Digital Library Xplore, ISBN : 978-1-4673-2047-4, IEEE Catalog Number: CFP1221T-CDR, 2012.
29. Dr.S.Palanivel Rajan, Dr.C.Vivek, “Performance Analysis of Human Brain Stroke Detection System Using Ultra Wide Band Pentagon Antenna”, Sylwan Journal, ISSN No.: 0039-7660, Vol. No.: 164, Issue : 1, pp. 333–339, 2020.
30. Dr.S.Palanivel Rajan, Dr.C.Vivek, “Analysis and Design of Microstrip Patch Antenna for Radar Communication”, Journal of Electrical Engineering & Technology, Online ISSN No.: 2093-7423, Print ISSN No.: 1975-0102, Vol. No.: 14, Issue : 2, DOI: 10.1007/s42835-018-00072-y, pp. 923–929, 2019.