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Analysis for VLSI Based Multipliers for High Speed Low Power Design Strategies

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Abstract

One of the key problems discussed in nanometer design is the low power creation of complex CMOS circuits. The transistor density increases significantly with the introduction of millions and billions of transistors on a single chip, resulting in more and more complex applications implemented on a single chip. Design time is another major challenge which forces designers to address the need to optimize chip performance over a very short period of time. Designers rely upon new methodologies and ready-mix solutions to optimize the field, time and resources to ensure the design is accomplished in the initial iteration. Signal processing and communication block sets are important issues, given that technological breakthroughs lead to new generation technologies which promote higher bandwidth and better signal quality. For an increasingly rising operating frequency, efficient, faster, and low-performance circuits need data processing. Throughout all levels of the design process, power management must be carried out. New methods must be implemented on the basis of hierarchical stages of design architecture. Energy saving in complex CMOS circuits is accomplished through the detection and compensation of major sources of power dissipation by correct design techniques. The techniques provided for the design of complex signal processing and communication blocks needed for 4 G, WiMax and wireless LAN applications may be common and adopted in this work.

1. INTRODUCTION

Size of transistor geometry resulted in millions of devices being combined into a very limited room, thereby allowing the realization of complex hardware applications and promoting high-speed applications. Design methods changed tremendously, while the basic concepts remained essentially the same, due to the increases in budgets and transistor and clock speeds, growing energy usage challenges and changes to efficiency and design instruments. App Scaling improved various applications' operating frequency which resulted in a high energy consumption. In designing complex VLSI circuits, low power technology has been successfully adopted and deployed. With the need for quicker, cheaper and reliable products operating on a remote power supply that delivers high end applications, new low-power design techniques for VLSI circuits are always required. The challenge of the VLSI designer is to develop a system which meets speed requirements, consumes small power or area, works reliably and takes little time to design. Low power technical systems are discussed in this work at circuit level, sub-system level and architectural level. The development and implementation of modern low-power techniques is carried out in 4 G communication network blocks such as root raised cosine filter, digital down converters, digital up and wireless locked-in loops.

1.1 MOTIVATION

Since new product demand and short design times and costs have been brought about by technology development, many of the designs used for complex VLSI circuits have failed to implement simple and creative power-reducing techniques. As the time to market was shorter, many engineers did not seek or did not deal with any of the intelligent techniques to minimize power at circuit, sub-system levelor design level. To reduce power it is important for the selection of suitable deceleration techniques to understand the architectural and functional requirements. There are also fewer literatures which analyze the results of different building blocks implemented using a semi-custom and complete flow. The signal processing blocks needed for building a Communication System, such as Root Raised Cosine Filter, Digital Up Converter (DUC), Digital Down Converter (DDC), and

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Digital Phased Lock Loop (DPLL), require power and speed optimization. The IPs of these blocks are very challenging, which inspired the design of secure, semi-customized architectures.

1.2 PROBLEM STATEMENT

Different power reduction strategies are suggested, and implemented to reduce the power on the VLSI circuit with the design of low-power generation technologies. The key power consuming blocks that conduct high speed data processing activities are signal processing and communication blocks; it is important to minimize power by using new approaches in these blocks. This condition is fulfilled by the problem statement in this study. Within this analysis new technologies are evaluated for reducing the power dissipation, for reducing power at all levels of abstraction (circuit level, sub-system level, and design level). The techniques developed are used for the production of complex construction blocks, such as the RRC, DUC / DDC and DPLL. FPGA, the full implementation of the work is carried out on a customized and semi-custom basis.

1.3 4G COMMUNICATION SYSTEM

4 G is the next big mobile network device upgrade to be introduced in the near future. High data rates in the mobile network need a huge interest for consumers in multimedia applications. Most wired network devices such as video conferencing, network SCADA and HDTV will be assisted by the introduction of 4 G mobile communication systems. The key criteria that modern transceptors have to meet to deliver a variety of innovative and high quality services to customers are the high capacity and variable bit rate information transmission with good bandwidth performance. In contrast to 3 G networks, the 4 G networking system has the following advantages:

- Higher bit rates than 3G (20 Mbps < peak < 200 Mbps)
- Higher spectral efficiency and lower cost per bit than 3G
- Higher frequency band than 3G (below 5 GHz preferred)
- RF channel bandwidths of 20-100 MHz

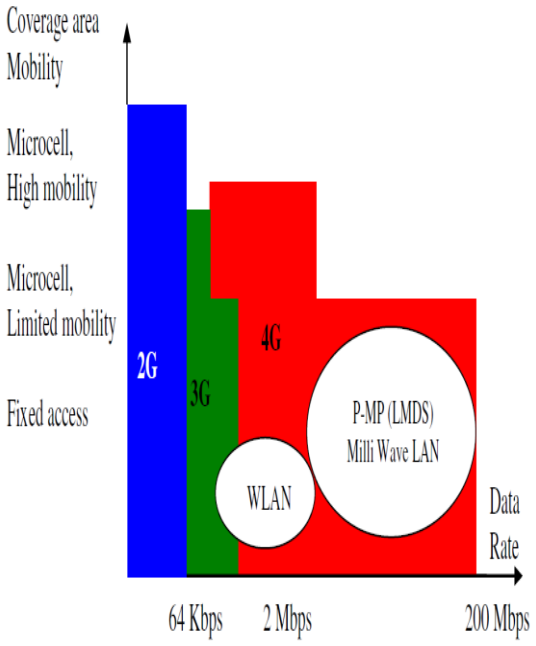

Figure 1.1 Advances in Communication Technologies

The 2 G, 3 G and 4 G networking network and their communications infrastructure advancements are outlined in Figure 1.1. Orthogonal Multiplexing Frequency Division (OFDM) is commonly used in wireless communications networks because of its high transmission power for data rates with a high bandwidth efficiency and its intensity to fade and delay in multipathes. The fourth generation mobile communications (4 G) technology has also been introduced as key technology.

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2. LITERATURE REVIEW

The new hybrid model for analog and digital circuit architecture proposed by NimaTaherinejadwas designed to propagate the transport, thus achieving a full 78ps lateness and 7,26μw adder for power consumption. The average improvement of 159%, 184% and 516%, in terms of Delay, Power Consumption and PDP, was shown by SPICE Simulations on the 0,18μm TSMC system.

S. R. Talebiyan has proposed a rapid low power 1-bit CMOS-free complete adder system, three modules have replaced one with a new design in a traditional full-adder system and optimized another to reduce the static power consumption. The concept was simulated and measured using the PTM 65 nm models.

The latency of Ali Malik is taking advantage of recent changes in FPGA architecture and the area's density. The use of the standard LOPs and Floating Points (2-Path) algorithms for FPGAs is difficult to achieve and contributes significantly to the overall latency of design. The FPGAs are designed to produce the LOPs. It is performed on a Xilinx Virtex-II Pro FPGA platform and synthesized.

Shoarinejad.A addresses and offers a performance overview for such CMOS cells in terms of the efficiency of single-bit full-adders. Quatorze full-bit add-ons are tested, with the use of 0.35, 0.25 and 0.18 μm TSMC CMOS technology, and three add-ons, a total of different adder cells. Therefore, a single-bit complete adder performance analysis is designed to delay, power and load capabilities of the logic components.

In order to reduce switching activities, Robin Sheen is proposing to build dynamic data based on the efficient dynamic range of data input, the functional blocks of the adder are involved in the dynamic data range and the unused functional blocks have a limited switching energy consumption. There is an attempts to reduce the number of busses transitions and hold two complementary arithmetic operations straightforward.

AmauryNève discusses possible methodologies to minimize the power delaying product for high-performance and low-power applications of 64-bit carrier-select additionals. A first realization using complex branch-based logic (BBL) cells in 0,18-m (PD) partially depleted silicon-on-insulators (SOI) induces a delay of 720 ps and a power dissipation of 96 mWat 1.5 V.

3. DESIGN AND ANALYSIS OF DUC AND DDC FOR LOW POWER APPLICATIONS

DUCs and DDCs are key components of all current designs of wireless base stations. Within the optical transmitters, DUCs are typically used to filter; sample signals and modulate from the baseband to the transmitter frequency. In order for the signal to be further processed at lower frequencies, the DDC must be demodulated, filtered and downsampled to a baseball. The IF-tobaseband and the IF-tobaseband functions including up / down frequency, band-selective filtering and tape-limiting filtering are implemented digitally within the software-defined radio architecture. In this implementation, interpolation and decimal operations are typically needed.

In general, one or more modulated DBS signals need to be sent to Radio Frequency (Rf) carriers for transmission on the side of a wireless communication network. The traditional transmission chain for the modulation of modulated data produces a specific modulated signal by a digital signal processor.A Digital to Analog Converter (DAC) and a Smoothing Filter transform this digital signal to an analog format. The analog simple band signal then is transferred to the target RF through a variety of analog IF processing strips. In case of transmission of multiple channels, they often require individual amplification and power control and are combined with an analog IF combiner. Digital IF upgrade requires a digital conversion converter to replace the first analog IF strip. Owing to its digitality, the initial IF processing has all associated advantages. This includes design versatility and manufacturing efficiency.

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3.1 DIGITAL UP CONVERTOR

Spread spectrum communication systems and CDM2000 and 3G basic stations are extensively used for wide-block and wireline systems, such as the digital broadcasting system, radio defined softwares (SDRs), cable modems, BPSK, QPSK, QAM modulators. The PFIR filter uses the Nyquist transmit filter operation to spectrally form the complex input signal at a rate of change of 2. For every stage of processing, bias free convergent rounding or truncating is used to restrict bit growth through the DUC.

The CIC filter's complex data stream is mixed with a local DDS oscillator. The mixer outputs are combined and are the final DUC output and they are used for the generation of the intermediate frequency signal as input to a digital to analog converter (DAC). The output from the DUC when D_{OUT} is nonvalid and the last valid output data is stored on a port of $D_{OUT}$when the programmable CIC rate change option is chosen, and the current rate change reaches the maximum rate change. The DUC consists of following blocks as shown in Figure 3.1; it has FIR filter, FIR filter compensation, cascaded comb integrator filter, optical direct synthesizer, multiplier, FIR filter P(z) pulse shaping pulse forming and FIR filter compensation C[z].

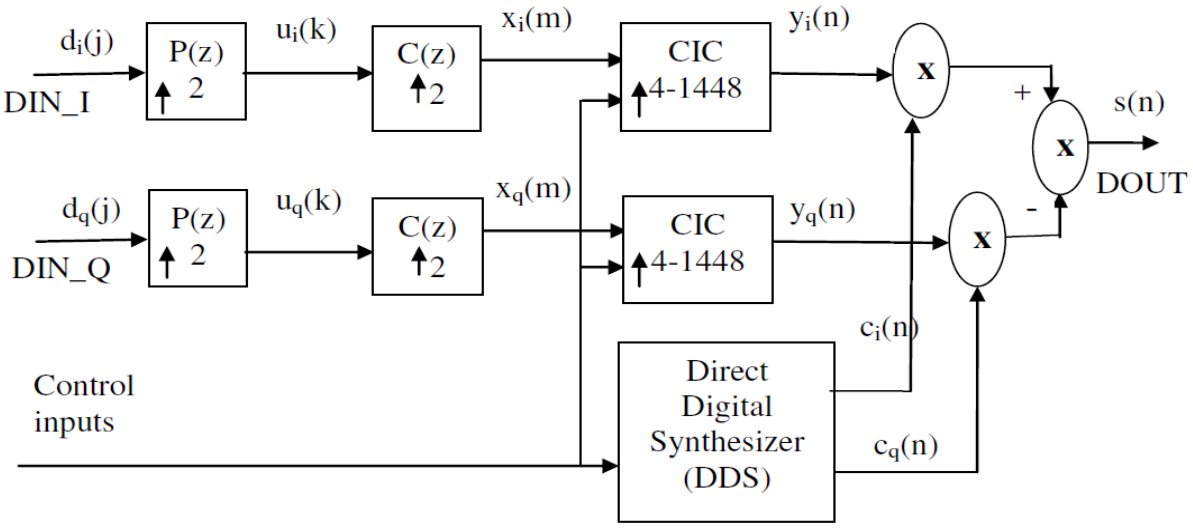

Figure 3.1 Block diagram of Digital Up Converter (DUC)

For any communication device, DUC and DDC form a transmitter and recipient pair.The diagrams shown in blocks include a series of filters such as the PFIR, CFIR, CIC, multipliers and suppliers [64, 79] to change signal from a baseband to HF or down to a basic-band signal conversion. Multipliers and adders are necessary in order for PFIR, CFIR and CIC to be implemented. DUC / DDC couples have very high power consumption, because they have more multipliers and additives.

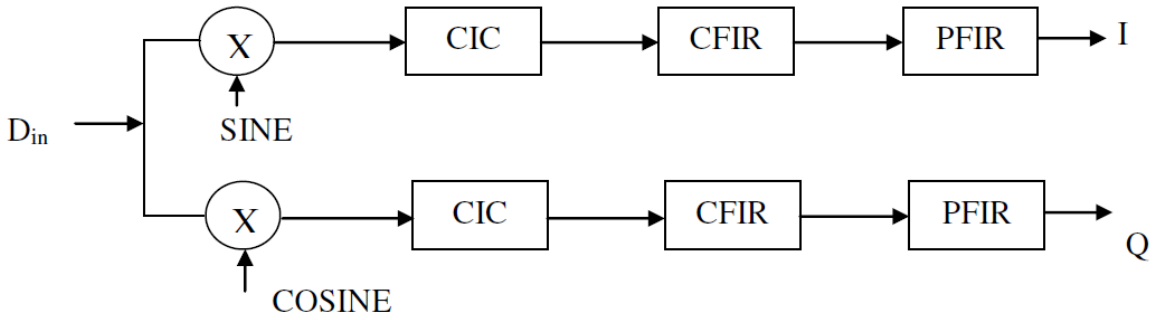

Figure 3.2 Block diagram of Digital Down Converter (DDC)

Specifies such things as data movement between blocks, number representation of input / output data and FPGA / ASIC implementation domains and low-power techniques that can save energy at the device level, as well as the reduction techniques that can be used to realize DUC / DDC. Within this portion, the design and VLSI implementation of DUC / DDC low power performance on ASIC and FPGA is carried out.

4. FPGA IMPLEMENTATION OF DUC AND DDC

The transmitter and receiver pair DUC and DDC combination has been designed in a top HDL package. The functionality of the HDL model is verified and the results achieved by using MATLAB are compared. In order to maximize area and power, both DUC and DDC on single FPGA will be implemented. The Verilog code is optimized for the architecture provided as Appendix D and simulated in ModelSim and synthetized in Xilinx ISE.

The input signal of 4 KHz is converted to 48 KHz to verify the design and to test the design functionality and re-fueled to the DDC block to transform the signal back to 4 KHz. The input and output signal are of the same frequency with some delay for properly built DUC and DDC parts. Specific test cases were considered to test the concept functionality. Direct digital synthesizer (DDS) or digital PLL block is required for DUC and DDC blocks at transmission and receiver. Digitale PLL block design and analysis (discussed above) is used in DUC and DDC implementation as a DDS block.

The block diagram of the architecture proposed for FPGA is shown in Figure 4.1.The input signal 300-4000Hz and the upstream intermediate signal are fed into the DUC and the DUC output is fed as an input to DDC and downstream to baseband signal for the input signal in the system.

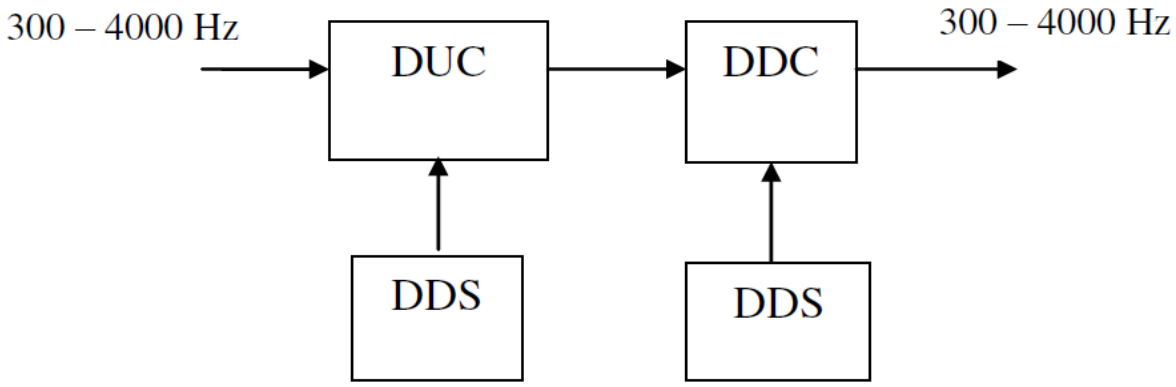

Figure 4.1 Block diagram implemented on FPGA.

5. RESULTS AND DISCUSSION OF DUC/DDC

This work uses a MATLAB (Simulink) to establish reference patterns for decimation and filter-interpolation. Hardware FIR is HDL modeled and ModelSim XE III 6.3c simulated. Xilinx ISE 10.1 is used for practical testing. For the verification of DUC and DDC on FPGA, a test environment is created. The design of the Spartan-3 FPGA Starter Kit is implemented.

MATLAB Simulation results of DUC/ DDC

Computer reference models are built as reference models to validate the hardware implementation of DUC / DDC. Discussions are provided in this section on the findings of the Computer reference model.

DUC (real-time domain) simulation results are modeled on MATLAB real figure 5.1 and a 4 KHz input signal is transformed by PFIR, CFIR and CIC at a samples rate of 2.4576 MHZ to a higher sampling rate. The findings are graphically presented. The input signal has several steps

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corresponding to any sample; this step is also the improved signal, but is not easy to distinguish as the sample rate increases.

A carrier signal always has the same sampling rate multiplies the up-converted signal. Figure 5.1 displays the up-converted signal. The up converted signal is the two-sided signal band, which filters the signal side band output. Figure 5.2 displays the effects of the DDC simulation (in time domain).

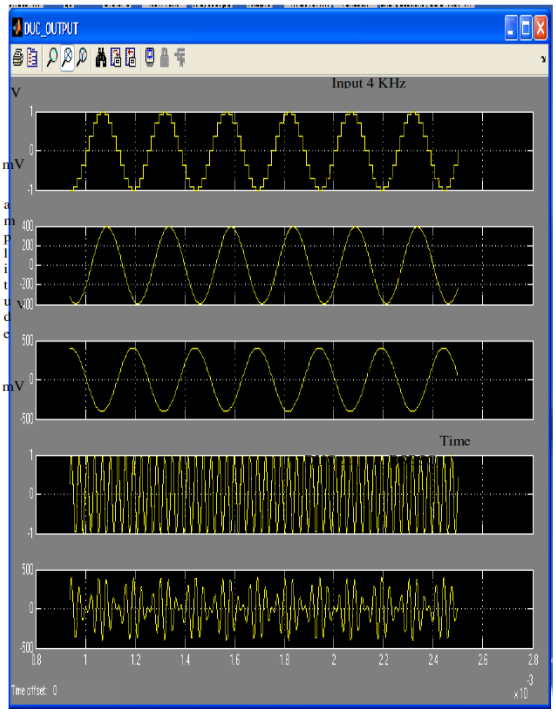

Figure 5.1 Simulation result of DUC in time-domain.

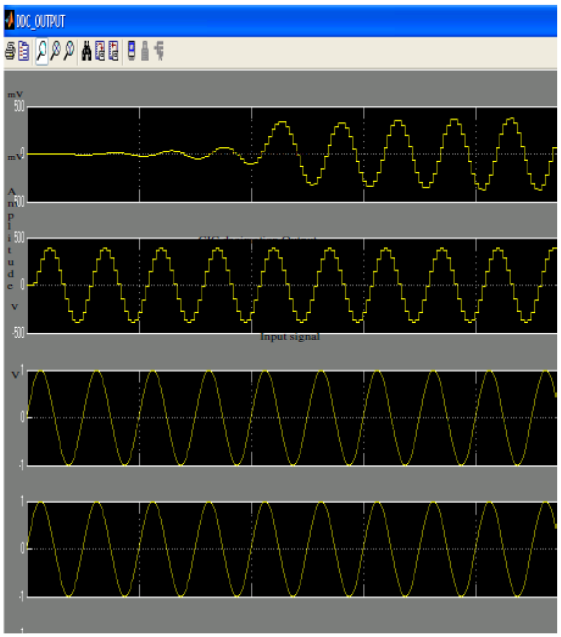

Figure 5.2 MATLAB simulation result of DDC in time-domain.

ModelSim Simulation results of DUC/DDC

ModelSim simulates HDL models for the planned DUC and DDC, with results estimated. The results show that the results of the Matlab simulation and HDL ModelSim are the same, thus confirming the functionality of the HDL model established.

Figure 5.3 displays the product of the ModelSim simulation of DUC. The 300-4000 Hz input signal is fed into the 4 & 5 interpolation filter series and the upsampled signal is multiplied with the DSBSC signal output.

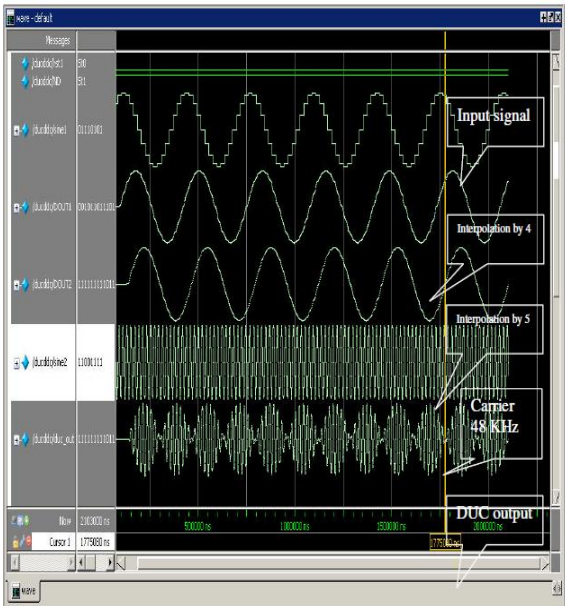

Figure 5.3 ModelSim Simulation result of DUC.

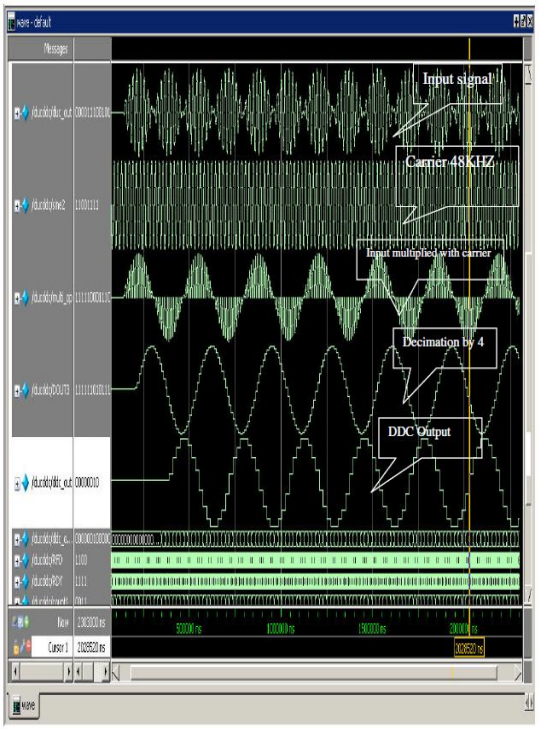

Figure 5.4 ModelSim Simulation result of DDC.

FPGA Implementation

Built HDL models are compatible with Xilinx ISE 10.1. The design is initially synthesized without restrictions based on the results obtained, so that it recognizes the resources of DUC / DDC to satisfy the specification needed. UCF file is modified based on the initial results. Pin restrictions are applied appropriately; area and timing limits have been set to maximize the area and power configuration. Figure 5.5 demonstrates the integration of the template and the optimized netlist.

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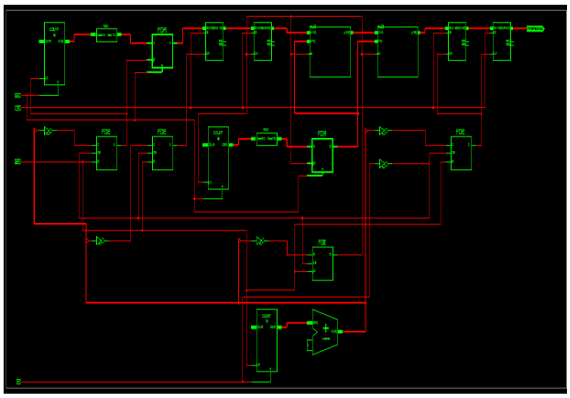

Figure 5.5 RTL Schematic for DUC and DDC.

CONCLUSION

This work includes the design, modelization and implementation of ASIC and FPGA of the most important block sets of communication units such as RRC, DUC, DDC and DPLL. For its output, various building blocks, such as adders and multipliers, required for signal processing and communication block sets, are analyzed. Various techniques for reduction in energy have been implemented to minimize heat, including variable Vt, multi-Vt, clock gating, heat gating and design of equipment. The results obtained show that the option of suitable multipliers and adders is an significant feature in complex signal processing applications. DUC and DDC are the primary coordination unit blocks, translating the baseline band signal to HF and vice versa. They use more resources as they have several filter stages and several data flow paths. It ensures that the DUC / DDC blocks must be kept to a minimum. In the implementation of RRC, low power techniques are implemented and applied to DUC / DDC. The result obtained optimizes and implements a single FPGA DUC / DDC block that forms a receiver pair.

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