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VLSI IMPLEMENTATION OF OFDM TRANSCEIVER USING CUSTOMIZED IFFT/FFT ALGORITHM

C.Valli[1], Smilee Mathuram[2], K.Abinaya[3], R.Arunkumar[4]

[1]*Asso Professor, EEE,Sri Venkateswaraa College of Technology, sriperumbudur,India . Vallime2013@gmail.com*
[2]*Asso Professor,EEE,AMET Deemed to be an University, Chennai, India. smileemp@hotmail.com*
[3]*Asst.Professor,EEE,Sri Venkateswaraa College of Technology, sriperumbudur,India*
[4]*abinayakumar.tvm@gmail.comAsst.Professor, EEE,Sri Venkateswaraa College of Technology, sriperumbudur,India arunk.sky@gmail.com*

Abstract

The orthogonal frequency division multiplexing system is a form of multicarrier modulation technology.FFT/IFFT processor is one of the key components in the implementation of wideband OFDM systems.It performs multi carrier modulation & demodulation.High performance &High speed algorithms are necessary for modulation&demodulation in OFDM transmitter &receiver respectively.

In this paper,principles of OFDM are described & we can implement high throughput OFDM tranceiver using efficient FFT algorithm.The processor is based on DITradix-2 FFT algorithm.Area,power dissipation &speed are most important factors when it comes to implementation of such system in VLSI domain.OFDM is used today in wireless local area network as specified by IEEE802.11a &also used for wireless digital radio &television signal transmissions.

Keywords-*OFDM,DIT,FastFourierTransform,VLSI implementation,wireless applications.*

1. INTRODUCTION

Mobile communication faces a particularly hostile environment, simultaneously containing multi-path, interfererice and impulsive parasitic noise. The problem is further complicated by the scarcity of available spectrum resources and power supply for the mobile devices[1,2]. Robust, bandwidth efficient systems with good performance in such an environment are therefore desirable for digital transmission. Orthogonal Frequency Division Multiplexing (OFDM), the most spectrum efficient multi-carrier modulation technique, has been recently proposed to overcome the adverse effects of communication channels .The OFDM technique transforms a highly-selective wide-band channel into a large number of non-selective narrow-band slices which are frequency multiplexed[3-5].

Orthogonal Frequency Division Multiplexing (OFDM) has successfully been applied to a wide variety of applications in recent years. It has been deployed in Digital Audio Broadcasting (DAB) and terrestrial Digital Video Broadcasting (DVB-T) applications in Europe. It has been adopted in the wireless LAN standards (IEEE 802.11a and Hiperlan2) and DSL wire line applications. It is quickly emerging as a potential candidate for the next generation wireless (fixed and mobile) voice and multimedia data communication due to its better bandwidth efficiency, immunity to multi-path degradation of the signal, and higher data rate[6-8]. Fast Fourier Transform (FFT) and Inverse Fast Fourier Transform (IFFT) are the key building blocks for OFDM transceiver systems. Thus, fast computation of FFT

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with an efficient VLSI structure is desired. Good VLSI implementation of FFT is constrained by factors such as smaller footprint, low power dissipation, modularity and simplicity[10-12].

Section 2 presents the principles of OFDM with its FFT requirements for wireless Applications, FFToptimization **as** well **as** their VLSI implementation issues and trade-offs are presented in Sections **3** and **4.**Simulation results of ofdm transmitter and receiver &discussions are given in Section ***6.***

2 .OFDM

OFDM**]** is a bandwidth efficient multiple access scheme for digital communication systems. Unlike conventional frequency division multiplexing, in OFDM the individual carriers are orthogonal to each other and overlap**.** Thus, the spectrum efficiency **is** achieved. Carriers **are** spaced in frequency at exactly the reciprocal of the symbol interval. Information content of a symbol is spread over multiple narrowband carriers instead of a single carrier. Again, each carrier carries information of multiple symbols. This fundamental property makes OFDM more robust during transmission. The advantage of OFDM based multiple access technique is its immunity against multipath, Doppler shifts, impulse noise, and narrowband interference. It has low co-channel interference and little or no inter symbol interference**.**

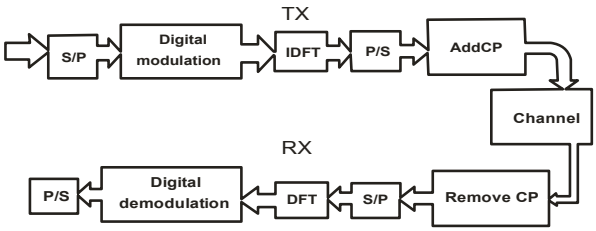

Figure 1. Block Diagram of OFDM Transceiver

In OFDM, a block of data is converted into a parallel form and mapped into each subcarrier in time domain. By transmitting the symbols in parallel, the interval between the signals becomes much larger and this effectively eliminates inter symbol Interference in time dispersive channels. IFFT (Inverse fast Fourier transformation) is in turn used to transfer the signal from time domain to frequency domain. It takes in N symbols at one time where N is the number of subcarriers in the system. Each of these N input symbols has a period of T seconds. As we know, the basis functions for an IFFT are N orthogonal sinusoids. Each input symbol acts like a complex weight for the corresponding sinusoidal basis function. Since the input symbols are complex, the value of the symbol determines both the amplitude and phase of the sinusoid for that subcarrier. The IFFT output is the summation of all the N sinusoids. Thus, the IFFT block provides a simple way to modulate data onto N orthogonal subcarriers. The block of N output samples from the IFFT make up a single OFDM symbol

3.FFT OPTIMIZATION

(A) Basic of FFT Algorithm

Fast Fourier Transformation (FFT) module is an Indispensable part for wireless and mobile communication, especially when broadband wireless systems require a high speed and low power hardware module for its packet-based high-speed data transfer, such as video transmissions and internet applications. This has made the design of FFT processor a critical requirement for the next generation wireless systems. The FFT hardware implementation will

have a dramatically lower power consumption and much higher computation efficiency than a software solution on general DSPs

The N-Point discrete Fourier Transform (DFT) of an input sequence x(0), x(1)…..x(N-1) and its inverse (IDFT) are defined by the following equations.

The DFT is given as,

$$X(k) = DFT(x(n)) = \sum_{n=0}^{N-1} x(n) W_N^{kn} \quad (1)$$

And IDFT is given as,

$$x(n) IDFT(X(k)) = 1/N \sum_{k=0}^{N-1} X(k) W_N^{-kn} \quad .(2)$$

Where, $W_N = e^{-j2\Pi/N}$

Cooley and Turkey first proposed the famous F'FTAlgorithm for computing the DFT, which breaks the Computation into smaller DlT computations. Later, Numerous FFT algorithms have been proposed. These
Algorithms are based on reorganizing the DIT computations. Direct implementation of DFT algorithm needs O(N2) multiplications and additions whereas F'FT Algorithms need O(N1ogN).

(B) 8 point radix2 FFT

To construct the 8-point FFT unit, we have chosen
the radix-2 DIT(Decimation-in-Time) 8-point FFTalgorithm. As shown in Fig,2 in this case, the butterfly Computations are predominantly addition and subtraction Operations. We exploited this fact and implemented a fully parallel 8-point FFT architecture by exactly following the buttert1y graph(Fig2) using only addition/subtraction and shift-and-add operations with Signed digital control. The internal wordlength of these units is 16-bit. The computation of an 8-point FFT is Carried out in a single clock cycle .

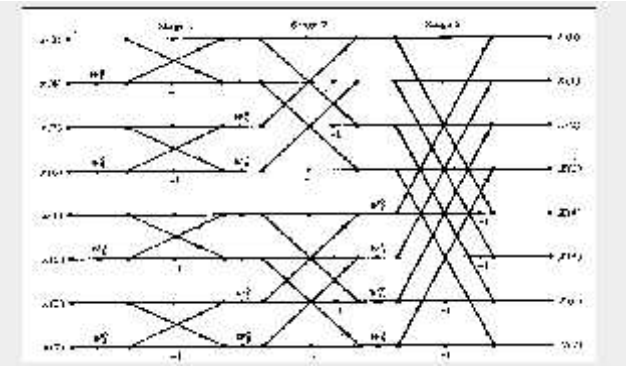

Figure. 2 Signal Flow graph of Radix-2 DIT – FFT Algorithm for N=8

DIT and DIF are two basic types of radix-2 FFT Algorithms. DIT of 2-point butterfly module can be expressedas

$$X_{m+1}(i) = X_m(i) + W_N^K X_m(i) \quad (3)$$

$$X_{m+1}(j) = X_m(j) - W_N^K X_m(j) \quad (4)$$

And the DIF algorithm can be expressed as

$X_{m+1}(i) = X_m(i) + X_m(j)$ (5)

$X_{m+1}(i) = [X_m(i) - X_m(j)]W_N^K$ (6)

DIT derives its name from the fact that the time sequence x(n) is decomposed into smaller successive subsequence's. While in one common derivation of DIF algorithm, the frequency values X (k), are decimated during each stage. In addition, DIT starts with bit-reversed order input and Generates normal order output, while DIF has normal order input and bit-reversed order output. There is no difference in computational complexity between DIT and DIF algorithms, and both of them need only $O(\log_2 N)$ arithmetic operations.

(3) Reduction of FFT Processor Hardware

According to definition of discrete Fourier transform(DFT) of an N-point input xn the twiddle factor can be separated as real and imaginary part W_N^{nk}=Xp+jYp,where Xp is real part and Yp is the imaginary part. For a 64 point FFT,the Twiddle factor range from W_{64}^{0} to W_{64}^{49}(p=0 to 49).According to symmetry of TW, ($W^{nk} = -W^{nk+N/2}$) and($W^{nk+N/4} = -W^{nk+N/4} = -jW^{nk}$),all the TWs can be obtained from the TWs p=0 to 8 by simple phase mapping..The proposed OFDM transceiver uses a TW multiplier which is implemented as magnitude and phase part respectively, to realize complex multiplications by TWs((A+jB)(Xp+jYp)=(AXp-BYp)+j(AYp+BXp)=Re+Img).For the magnitude part, the multiplication of constant values(Xp &Yp) can be performed more efficiently by using shift & add operations.W_{64}^{7} is decomposed with a power of 2:

$W_{64}^{7} \sim 1 - 2^{-2} + 2^{-6} - 2^{-7}$

By using the signed digit technique to minimize the non –zero bits the number of adders can be reduced further.That means the real and imaginary parts of all TWsets share only 3 adders and two adders to perform shift and add operations ,respectively.

For the characteristic IEEE 802.11,the IFFT/FFT processor operates at the up sampling frequency of 40Mhz,which is twice the data rate. Therefore, the real part and imaginary part of the magnitude can share only one hardware. Consequently the modified complex multiplier needs only seven adders and some MUXs, and no ROM is required to store TW coefficients.

4. VLSI DESIGN TRADE OFFS

4.1Choice of radix

Time to compute an N point FFT with single butterfly hardware can he defined as

$T_{FFT} = N/r.\log_r N.T_{r.PE}$ (7)

Where,
N/r = No. of butterfly per stage
log,N = No. of stage
Tr.PE= Time to calculate one butterfly.

This time requirement maybe reduced by factor of L, where L = number of butterfly hardware elements. From **(7),** it is evident that time required to compute an N point sequence decreases with higher radix. Furthermore, the number of computations is significantly less for higher radix especially with large N. But hardware complexity increases exponentially with higher radix.

4.2 Parallel operation

Parallel processing by hardware replication is an imponant design option. More processing elements clearly lead to larger hardware footprint. High density VLSI integration enables designers to use more parallelism. Using parallel processing, a trade off between speed of computation and power dissipation can be achieved, at the cost of more hardware.

4.3: Pipelining

Pipelining is an effective way to speed up a circuit or achieve the low power goal. In pipelining, a set **of** registers is placed in the forward cut-set of a circuit to reduce the critical path. This leads to increased clock speed or reduced supply voltage design. Advantages of pipelining are achieved at the cost of system latency.

4.4: Low power

Both parallel processing and pipelining can be utilized to reduce the supply voltage, which leads to low power dissipation according to the following equation.

$$P=kC_LfV_{dd}^2 \qquad (8)$$

Where, k= Switching activity
$\mathbf{C_L}$= Total capacitance of the circuit
f = Frequency of operation
V_{DD}= Supply voltage.

In general, reducing the supply voltage is an attractive design option. However, circuit delay increase's drastically when the supply voltage approaches the sum of the threshold voltages of the PMOS and NMOS transistors for the **CMOS** process. Reducing the threshold voltage leads to increased static power dissipation.

5. SYSTEM SIMULATION WITH FIXED-POINT FFT PROCESSOR

The WLs of the processor should satisfy the required system SNR and SQNR both. According to 802.11 specifications, the SNR requirement for 64-QAM is 26 dB, and the SQNR requirement needs and additional margin of 12 dB as compared to the SNR to make the SNR degradation due to quantization noise less then 0.25dB.Moreover,the signal WLs of the IFFT/FFT processor,<x,y,,z>(x is sign bit,y is integer bit,z is fractional bit),determined by the fixed-point analysis are <1,0,9> for FFT inputs and <1,6,12> for FFT outputs. When the signal passes through every PE,the integer bit is added one to avoid SQNR loss.

(A) Chip Design

After the appropriate WL of the OFDM Transceiver with FFT processor is chosen by the fixed point analysis, the whole chip was designed using hardware description language and the chip output is functionally verified using FPGA. The proposed system uses processor

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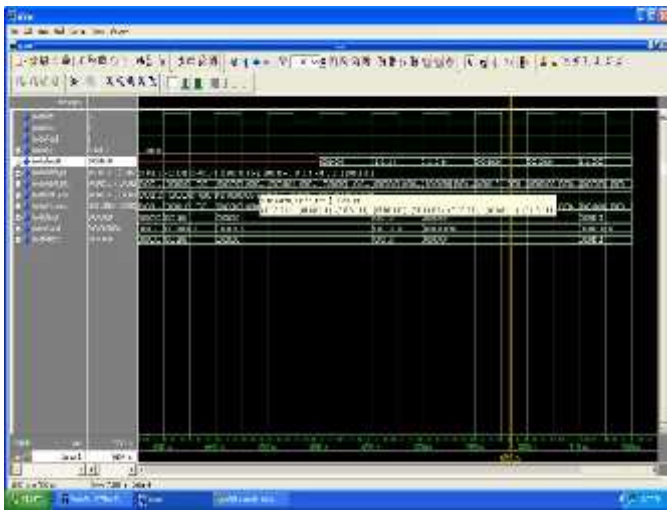
which is fabricated by .18 µmeter CMOS process. Obviously the result of the post simulation and chip measurement are on speed of 40. MHz and match very well for 200 symbols. At the operating frequency of 40 MHz, the power consumption of FFT processor is only 7.74 mW at the supply voltage of 1.8 volt.The core size is .57mmx.565mm

(6) RESULT AND DISCUSSIONS

A .SIMULATION RESULTS

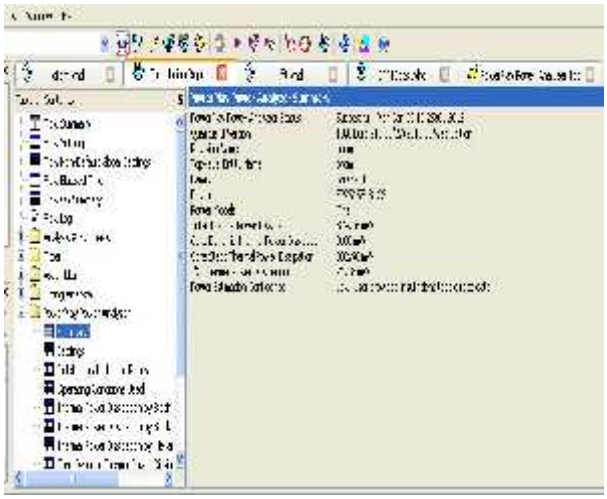
i) Serial to parallel convertor output

i) OFDM transmitter output



iii) OFDM receiver output

IV).Power Analysis



B .CONCLUSION

We focussed on OFDM transceiver with a cost efficient processor with its fixed point analysis. The IFFT/FFT processor is a multiplier less architecture since the complex multiplication of the TW is realised by hardwired shift-and- add operation without any memory storage such as ROM. Furthermore the non-zero bits of TW s are minimised to reduce the structure of the shift and add by proposed classification of TWs and Hardware sharing. The quantisation noise power of the processor can be calculated by analysis. Measurement result show that the processor chip area operates up to 40MHz under 1.8 V supply voltage and power consumption is 7.74mw.

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