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Efficiency Analysis of a Synchronous Buck Converter

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Abstract
DC-DC converters occupies very significant role in the field of industries or daily life applications. To charge batteries of low voltage associated with continuous power supply (UPS), DC-DC converters are required. Batteries requires low voltage and the accessible voltage at the source is to be advance down to the required level of voltage at the purpose of utility (PoU). While planning DC-DC converters, productivity and effortlessness of the circuit is particularly essential. Basically for the UPS applications, Buck converter can convey the voltage at required level which is exceptionally basic in activity yet the expanded misfortunes in diode can be addresses by utilizing a synchronous Buck converter. By utilizing synchronous Buck converter, the diode conduction misfortunes in Buck converter can be limited, subsequently enhancing the proficiency of the converter. In this paper, Synchronous Buck converter is utilized to charge the batteries of UPS. In this paper Design, displaying of synchronous Buck converter for UPS application was done and its outcomes were gotten by utilizing Matlab/Simulink. An equipment model was additionally created and the equipment comes about were likewise appeared.

Keywords— *Uninterrupted power supply (UPS), DC-DC Converter, Point of Utility (PoU), Buck, interleaved Buck, Conduction losses.*

1. INTRODUCTION

Efficiency versus cost is always a trade-off when designing a switch mode power supply, with synchronous buck converters being no exception.The large variety of discrete components that are on the market today offer the designer a nearly infinite
number of solutions. This, combined with tight schedules and budgets, increases the need for a fast and accurate way to predict the performance of a system. Ideally, these predictions begin before a circuit is built, to reduce the number of design iterations that are needed to provide an optimized solution. As part of an optimized solution, the designer must verify that design meets efficiency and cost requirements, without exceeding temperature constraints of lossy components.The goal of this application note is to provide designers of synchronous buck converters with a fast and accurate way to calculate system power losses, as well as overall system efficiency. The majority of power losses in a typical synchronous buck converter occur in the following components:

- High-Side MOSFET
- Low-Side MOSFET
- Inductor
- MOSFET driver

HIGH-SIDE MOSFET LOSSES

The total power loss in any MOSFET can be summed up as the losses due to conduction, and the losses due to switching. In a low-duty cycle, converter switching losses will tend to dominate for a MOSFET in the highside position. The duty cycle for a buck

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converter is described as: Dc= Vout /Vin where Vout= system output voltage, Vin = system input voltage. When the duty cycle is low, the high-side switch will be on for a small percentage of the period. The drain of the high-side MOSFET is tied to VIN, while the source is tied to the phase node, as shown in Figure 1. When the high-side turn on begins, the phase node is clamped below ground by the body diode of the low-side MOSFET. This large voltage differential from drain-tosource, in addition to the fact that the high-side MOSFET is also switching the full load current of the converter, leads to a lossy switching event.

High-Side Conduction Losses

Conduction losses in a high-side MOSFET are described as:

EQUATION 1:

PHS□COND□□= RDS□ON□□□□IDS□RMS□2 **,**Where RDS(ON) = Drain-to-Source On Resistance, IDS(RMS) = RMS Drain-to-Source Current.

Note that the IDS(RMS) term is squared in this calculation. Therefore, as load current increases and as the duty cycle gets higher, the conduction losses may exceed the switching losses.The calculation for RMS drain-to-source current, aswell as inductor ripple current, can be found. Since RDS(ON) is dependant on the junction temperature of the device, and losses will increase the junction temperature, an iterative calculation is necessary. These iterations must be performed until the junction temperature of the device stabilizes (generally to <1%).

High-Side Switching Losses

Figure 2 is a graphical representation of the switching losses in the high-side MOSFET. Note that these are ideal waveforms, and assume a constant gate current.

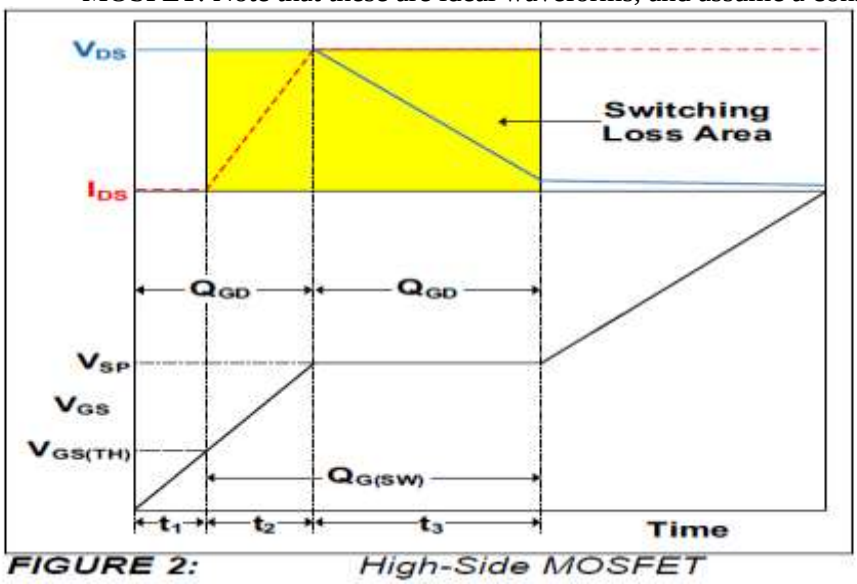

FIGURE 2: High-Side MOSFET

FIGURE 2: shows the *High-Side MOSFET Switching Waveforms.*

The initial rise period t1 of VGS (the MOSFET's gate-to source voltage) occurs when the MOSFET driver begins to supply current to the MOSFET's gate. During this time, the input capacitance CISS (CGS + CGD) is being charged, while VDS, the MOSFET's drain-tosource voltage, remains constant. A diagram of a MOSFET's parasitic capacitances is shown in Figure 3. There is no drain-to-source current flow at this time. Therefore, there are no switching losses during this period. At the beginning of period t2, the VGS voltage exceeds the gate-to-source threshold voltage (VGS(TH)). Current will begin to flow from drain-to-source, while CISS continues to charge. This current will rise linearly until IDS equals the inductor current IL. Since there is a voltage drop across the MOSFET equal to

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VIN, and current IDS is flowing through the device, there are significant switching losses during this period.During period t3, the IDS current remains constant,while the VDS voltage begins to drop. While the drain to source voltage is dropping, nearly all of the gate current is delivered to charge CGD. Since almost no
gate current is used to charge CGS, the gate-to-source voltage remains relatively flat at a voltage called the "switch-point" voltage (VSP). This region is commonly known as the Miller Plateau. During this period, similar to t2, there is a voltage drop from drain-to-source, as well as significant current flowing through the device.Therefore, t3 is a lossy period of the switching cycle.Upon exiting period t3, the MOSFET channel is enhancing, up to the point where VGS reaches its maximum value. Switching losses have ceased, and conduction losses occur until the high-side MOSFET is turned off. The turn-off event is very similar, happening in reverse of the turn-on event.

The power loss during the switching cycles of the highside MOSFET can be described as:

EQUATION 2:

PHS□SWITCH□□□□□VIN □□IOUT)/2 FSW*(tS□LH□□+ tS□HL□□□*

Where:
VIN = Input Voltage
FSW = Switching Frequency
tS(LH) = Switching Time, Low-to-High
tS(HL) = Switching Time, High-to-Low

The switching times from low-to-high and high-to-low can be calculated using Equations 3 and 4:

EQUATION 3:

tS□LH□□□□QG□SW□□□□IDRVR□LH□

Where:
QG(SW) = Gate Charge, Switching
I DRVR(LH) = Driver Current, Low-to-High

EQUATION 4:

tS□HL□□□□QG□SW□□□□IDRVR□HL□

The QG(SW) parameter can be found using the VGS versus QG characterization graph that can be found in

the MOSFET's data sheet (see Figure 2). It is the charge required to bring the VGS from VGS(TH) to the

end of the Miller Plateau. QG(SW) can also be found if QG(TH) is listed as a data sheet parameter, using Equation 5:

EQUATION 5:

QG□SW□□= □QGS + QGD□□– QG□TH□ Driver currents for each transition are described in Equations 6 and 7:

EQUATION 6:

IDRVR□LH□□□□□VDD – VSP)(RDR(PU)+ RG+ RDAMP)

Where:
VDD = Driver Voltage
VSP = Switch Point Voltage
RDR(PU) = Driver Pull-Up Resistance
RG = MOSFET Gate Resistance
RDAMP = External Damping Resistance

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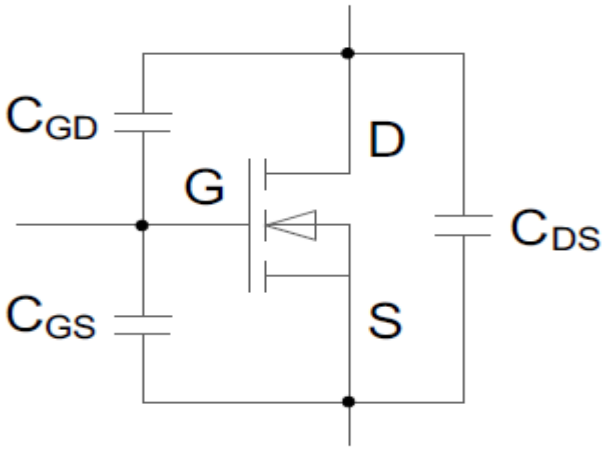
EQUATION 7:

*IDRVR□HL□□□□VSP / (*RDR(PD)+ RG+ RDAMP)

RDR(PD) = Driver Pull-Down Resistance
RG = MOSFET Gate Resistance
RDAMP = External Damping Resistance



$C_{ISS} = C_{GD} + C_{GS}$
$C_{OSS} = C_{GD} + C_{DS}$
$C_{RSS} = C_{GD}$

FIGURE 3: *MOSFET ParasiticCapacitances.*

Other High-Side MOSFET Switching Losses

Although conduction and switching loss account for a majority of power losses in the high-side MOSFET,

there are other minor lossy areas in the switching cycles. One of these areas of loss is the power lost due

to charging the gate of the MOSFET, expressed as:

EQUATION 8:

PGATE = QG□TOTAL□□□□VDD □□FSW

Where:
QG(TOTAL) = Total Gate Charge

Note that QG(TOTAL) will change with respect to VGS, so be sure to pick the value from the data sheet that

corresponds with the MOSFET driver's gate drive voltage (VDD). These losses will be distributed among

all resistances in the gate drive path, including the MOSFET driver pull-up or pull-down resistance

(depending on which edge is being evaluated), the series damping resistor (RDAMP) and the gate

resistance of the MOSFET (RG).

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Another area of loss in a synchronous buck converter is the reverse recovery loss of the low-side MOSFET's

body diode. Note that this power loss will occur in the high-side MOSFET, as it is the turn on of this device

that has to recover the low-side's body diode. The charge required to recover the body diode can be found

in the MOSFET's data sheet, under diode characteristics, labeled QRR. These losses can be described as:

EQUATION 9:

$$PDIODE\_RR = QRR \cdot VIN \cdot FSW$$

Where:

QRR = Body Diode Reverse Recovery

EQUATION 10:

$$PCOSS = \{ COSSLS + COSSHS \cdot VIN^2 \cdot FSW\}/2$$

Where:

COSSLS = LS MOSFET Output Capacitance

COSSHS = HS MOSFET Output Capacitance

LOW-SIDE MOSFET LOSSES

Looking back at Figure 1, it can be seen that the lowside MOSFET's drain is tied to the phase node, while

the source is connected to ground. When the high-side device turns off, and before the low-side MOSFET is

turned on, the body diode in the low-side MOSFET will begin to conduct, as current through the inductor must

continue to flow. Since the source of the low-side device is tied to ground, the phase node must go below

ground by a voltage equal to the forward drop of the body diode, in order to conduct. Therefore, when the

low-side switch is turned on, there is only a voltage equal to the forward drop of the body diode across it.

This leads to a "soft" switching event, with losses that are considered negligible in this application note.

As with the high-side MOSFET, the losses in the lowside MOSFET are largely dependant on duty cycle and

RMS current. Conduction losses, both from drain-tosource while the device is on, and from source-to-drain

through the body diode when both MOSFETs are off,completely dominate in a low-side application.

Low-Side Conduction Losses

Similar to conduction losses in the high-side device, the conduction losses in the low-side MOSFET can be

calculated with the following equation:

$$PLS\_COND = RDS\_ON \cdot IDS\_RMS^2$$

Since the duty cycle in synchronous buck converters tends to be low, the drain-to-source RMS current in the

low-side MOSFET can become quite high. At high-load currents, the conduction losses in the low-side device

can become the largest area of loss in a buck converter. As with the high-side MOSFET calculations,

the conduction losses in the low-side device require an iterative calculation, in order to provide accurate

results.

As explained earlier, the body diode of the low-side MOSFET will turn on when both switches are off in a

synchronous buck converter. During this time, known as Dead Time (DT), conduction losses will occur in the

body diode. These losses can be described as:

$$PDIODE = DT \square\square FSW \square\square VSD \square\square IOUT$$

Where:DT = Dead Time, Rising and Falling

VSD = Diode Forward Voltage

Note that the DT in this equation accounts for both the rising and falling edges combined. At low-load currents,

it is common to see the diode conduction losses equal to, or greater than, on-time conduction losses in the

low-side MOSFET.

Low-Side MOSFET Gate Charge Losses

Another component of power loss in the low-side MOSFET, although small, is the power lost charging

the gate. This loss is calculated using the same formula used for the high-side device (see Equation 8).

INDUCTOR LOSSES

In a synchronous buck converter operating at high-load currents, the equivalent series resistance of the

winding of an inductor will have a significant impact on system efficiency. This impact can be described as:

$$P_{INDUCTOR} = ESR_L * I^2 OUT$$

Where:

ESRL = Inductor Equivalent Series Resistance Note that this power loss is not dependant on the duty

cycle, since the inductor is always conducting. Inductor selection is critical when optimizing a synchronous

buck converter, as power loss in the inductor can rival losses in the MOSFETs, when the load current is high.

Core losses will not be discussed in this application note, as the calculations can become complex. These

losses can usually be considered negligible, when compared to the inductor's conduction loss.

5.CONCLUSION

DC-DC converters assume an exceptionally indispensable part in a significant number of the applications particularly in the field of energy supply to low power necessities. In this paper we have thought about the use of charging batteries to drive UPS. This diminishment in misfortunes can enhance the converter effectiveness by at least 5%. In this paper, the model of interleaved Buck converter was given its outline. Ordinary buck converter was additionally talked about with its yield comes about. Simulink model of interleaved buck converter with both open circle and shut circle task was displayed alongside its outcomes. Additionally model of ordinary buck converter with both open

circle and shut circle task was displayed alongside its outcomes. The capacitor voltage swell and inductor current swell substance is additionally kept up underneath 2% and 5% individually. The contribution of 320V is diminished to 150V and the outcomes relating to this discourse were likewise appeared. Shut circle task conveys the yield of the converter to its last an incentive in substantially less time when contrasted with open circle activity in both buck and synchronous buck converter which can be seen from the yield comes about. Equipment model of the above said converter was composed and the outcomes relating to the equipment were additionally appeared in detail.

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