International Journal of Advanced Science and Technology
Vol. 29, No. 7s, (2020), pp. 5779-5791

Design and Analysis of Noise Tolerant, Low Power Wide-OR Domino Logic by using Interconnects in DSM Technologies

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Abstract

In Present scenarioDynamic logic approach is used in high performance circuit design because of its fast speed and less transistors count when compared to MOS logic style. The main drawback of the dynamic circuit is the power consumption which is mitigated in domino logic design, another problem lick UNG which is reciprocal to the leakage power and charge sharing problem is also reduces in novel domino circuit design. Here in this manuscript we have introduce RLC interconnects with wide fan-in domino logic there is also leakage reduction technique is incorporated in domino logic design to save the maximum power and increase the speed of the circuit. In proposed design a chain of evaluation network with stacking effect and RLC interconnects in the dynamic node help in reduction of the leakage current and achieve maximum UNG, so overall performance of the circuit improves. With the help of stacking effect and insertion of the current mirror circuits in proposed design achieves more noise immune and improves overall performance parameters when compared with other existing domino logic. Here simulation is performed at 32nm with MOS technology at 100MHz frequency with supply voltage of 0.9V. The proposed domino circuit saves 96.4% power consumption, delay upto 52.4% and UNG 5.6x when compared with other existing circuits.

Keywords :RLC*; Dynamic Logic; UNG; MOS;; Robustness; Wide fan-in gate.*

1. INTRODUCTION

As with the rapid integration of VLSI system the demand of more functionality is increasing day by day, to meet this requirement we are making a portable devices with low power budget and enhance higher speed of the circuit as it is seen in today's microprocessor devices. To achieve high speed and lower power consumption transistor technology and power supply must be scaled down simultaneously. As the technology scales down the threshold voltage (V_{th}) of the transistor also lowers in the same proportionate [1]. Scaling of threshold voltage results in exponential increase of sub threshold leakage current in the evaluation transistor and makes the domino logic less noise immune. The main source of noise in deep-submicron circuit is mainly due to the higher leakage current, crosstalk, supply noise and charge sharing, while noise at the input of the evaluation transistor may increases due to increased crosstalk. In domino logic scaling the supply voltage and capacitance of dynamic (pre-charge) node reduces the amount of charge stored at the dynamic node. While considering all this factor we are going to improve overall performance of the digital circuit, the noise immunity of domino circuit has to increase but it degrades as technology scales down below 90nm.

Leakage immunity is increasing in wide fan-in domino OR circuits because current will flow more in OR gate (parallel network). As we have seen that as we increase the OR network with wide fan in is directly proportional to leakage current, for measuring UNG which is going to decreases as fan-in of

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the circuit is increases[2]. UNG is the important parameter in wide fan-in domino OR logic for improving the performance of the circuit, because the evaluation transistor are all in parallel, leaking the charge from precharge node [3].

For increasing the robustness of the circuit we are upsizing the Keeper transistor but there is degration of performance will take place, it is not applicable in conventional method, so we are using week keeper transistor. A full keeper is added in precharge node to improve the robustness of the dynamic node. The keeper ratio (K) is measuresed as mobility of keeper and evaltion transistor and the aspect ratio of the keeper and evaluation network,

$$K = \frac{\mu p \left(\frac{W}{L}\right) keeper\ transistor}{\mu n \left(\frac{W}{L}\right) evaluation\ transisitor}$$

Here, W represent the width of the transistor and L denote the channel length of the transistor , μ_n and $\mu_p$is the mobility of transistors.

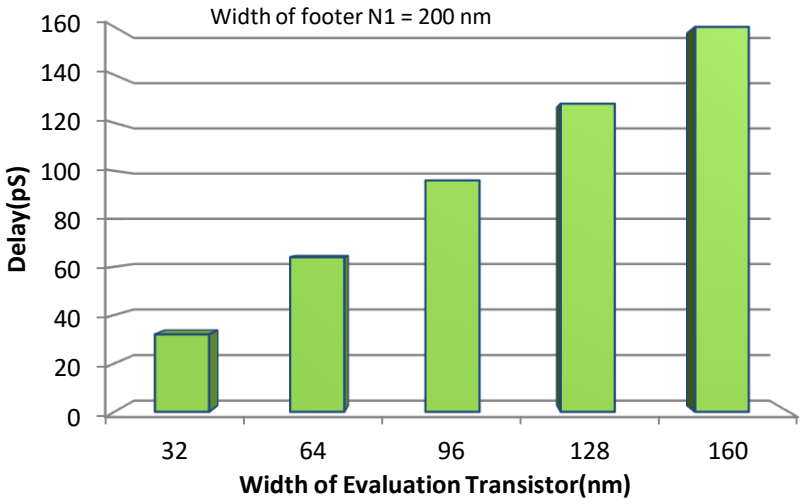

Fig.1: As delay and width Effect on Evaluation network

With the upsizing of the keeper transistor there is a flow of contention current between the NMOS evaluation network and keeper transistor, one network is discharging the dynamic node and another network is charging the dynamic node this leads to increase the evaluation delay of the circuit which results in the penalty of power consumption of the circuit and overall the performance of the circuit is degrades[4]. For improvement of UNG of the network and we are introducing a novel network at evaluation phase which controls the leakage, without upsizing the keeper transistor and reduces the tread off in between delay and power [5].

Here in over proposed design for wide fan-in domino OR logic with RLC interconnects, we have inserted a leakage reduction network which help in improving the UNG of the circuit, makes over circuit more robust and scalable over circuit at a nanometer regime without degradation of performance of the circuit. The arrangement of the transistor is in such a way that the UNG is

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improved, reduction of power consumption with the unity delay, we can cascade the circuit at a higher level while using RLC interconnects.

The paper is organized as follows. Literature review about existing domino circuit discussed in section 2. Noise immunity metrics used for Unity Noise Gain (UNG) in section 3. The proposed circuit description is in Section 4. Simulation result is presented and compared in section 5 with the brief conclusion of the paper in section 6.

II. LITERATURE REVIEW

Many existing domino circuits is study in this literature survey such as conventional higher fan-in domino OR logic with footerless and footer transistor, high speed domino, conditional keeper domino, wide OR gate diode footer domino. The main goal of these circuit design technique is to improved noise immunity and circuit performance, especially for wide fan-in circuit.
The main aim of designing a domino circuit is to achieve high-speed in digital logic design; however, there are many challenges occur with the sensitivity of the domino circuit with the noise perameters as technology scales down at nanometre regime. There are several alternate design come into the existence for reduction of power and improve the UNG of the circuit. In conventional, footed logic a keeper transistor is inserted below evaluation network which increases the resistance of the circuitwhich results in improving the overall UNG of the circuit hence overall performance is improved. However, while insertion of the PMOS keeper transistor results in the performance degradation and overall power consumption of the circuit is increase. If we increases the robustness of the RLC interconnect based domino circuit, there is Upsizing method of the keeper transistor is best possible way but the contention current of the evaluation network increases which increase in power dissipation of the domino circuit and there is enhancement in evaluation delay of the network. For achieving the high speed in RLC interconnects based domino circuit small size keeper is desirable. Interconnect modelling is critical in both the circuit design and verification processes. An efficient and accurate interconnect model paired with smart MOS Metal oxide field effect transistor buffers can meliorate these processes. In Fig.2 RLC based interconnect is cascaded in series which is followed by the buffer, all RLC interconnect is made with copper element and to achieve higher driving capability copper is used.

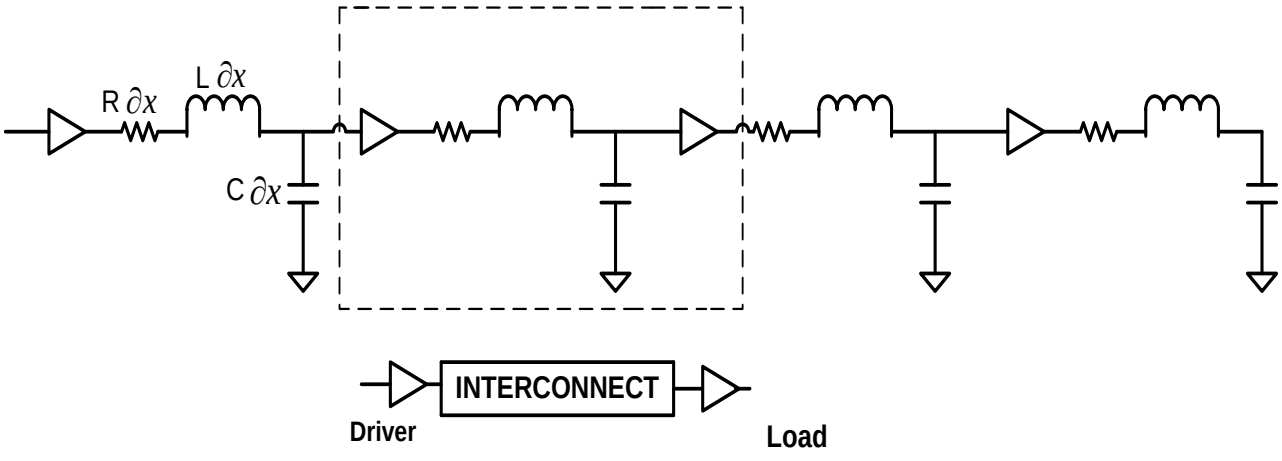

Fig.2. Equivalent Circuit Diagram of RLC Interconnects

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The working of FooterLess Domino Logic (FLDL) is shown in Fig.3. is similar to Footed Domino Logic (FDL) shown in Fig.3.The advantage of FDL over FLDL is more noise immune. The noise immunity is higher because of using stacking effect due to the added footer transistor at the bottom of the evaluation network. The convention FDL is used to achieve higher noise immune for reduction of leakage current and enhance the speed of the circuit [6].

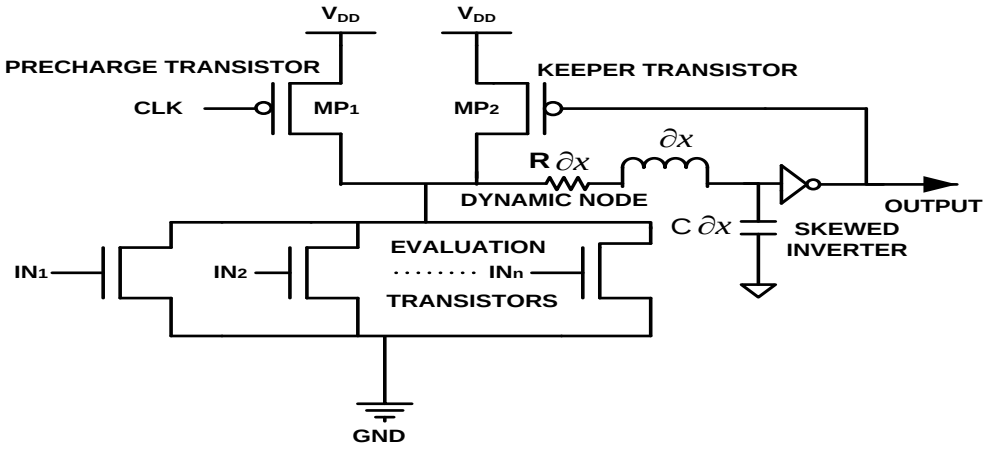

Fig. 3: Conventional High Fan in Domino OR Gate with FooterLess Domino Logic [FLDL]

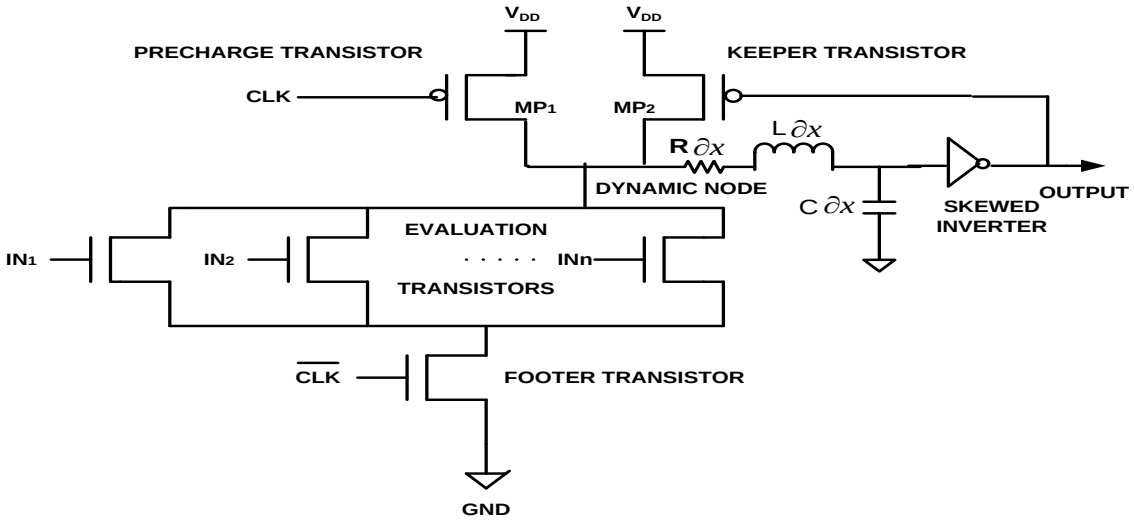

Fig.4: Conventional High Fan in Domino OR Gate with Footed Domino Logic [FDL]

2.1. High-speed domino

One of the existing leakage tolerant domino circuits is High Speed Domino (HSD) logic as shown in Fig 5. At the beginning of the evaluation phase, the input delay element is low and the clock is high. PMOS transistor MP_3 is ON and therefore it turns OFF the keeper transistor MP_2. After a delay equal to the delay of the inverters, when clock delayed is high, if the output node is high, MN_1 remains in the OFF state and keeper transistor MP_2 also remains OFF [7]. However, in the other case when output remains low after that delay (delay of inverters) in the evaluation phase, dynamic node is

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connected to the output node through the inverter. This causes PMOS transistor MP_2 (keeper transistor) to be turned ON to keep the dynamic node strongly connected to V_{DD} for the rest of the evaluation phase. The turned OFF keeper transistor at the beginning of the evaluation phase helps to remove the contention between the keeper and NMOS evaluation network, thus achieving less power consumption and higher performance. However, the dynamic node is floating at the beginning of the evaluation phase since the keeper is turned OFF. Therefore, if there is noise at the inputs at the onset of evaluation, the dynamic node can be discharged resulting in wrong evaluation [8].

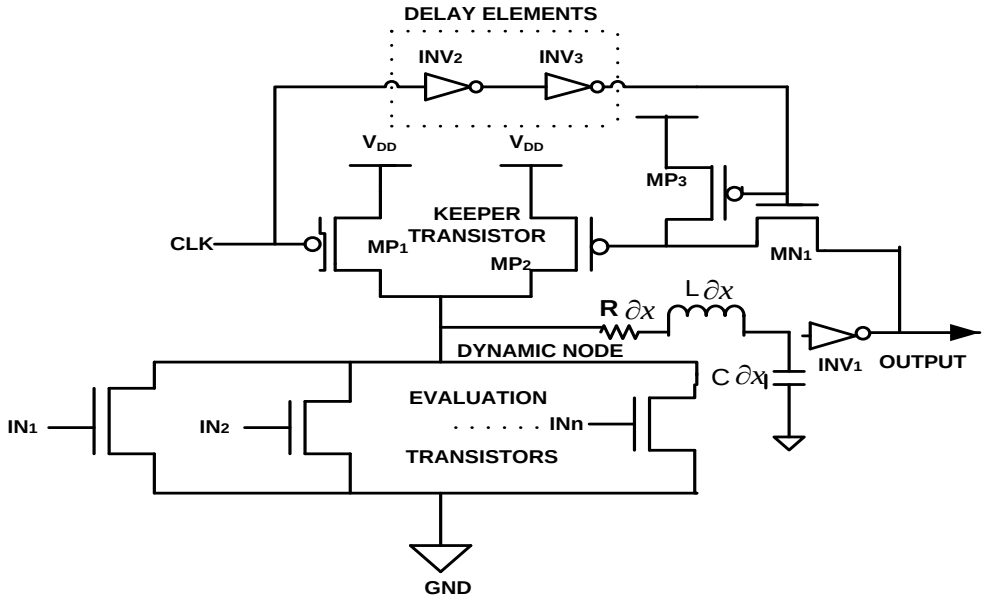

Fig.5: High Speed Domino [HSD] Logic Circuit

2.2. Conditional keeper domino logic

Another existing leakage tolerant domino circuit is the Conditional Keeper Domino (CKD) logic. The circuit schematic of the conditional keeper is shown in Fig 6. The circuit works as follows: at the beginning of the evaluation phase, the smaller keeper (K_1) is ON for keeping the state of the dynamic node. After delay of the inverters if the dynamic node is still high, the output of the NAND gate goes low to turn ON K_2 [9]. This keeper transistor is sized larger than K_1 to maintain the state of the dynamic node for the rest of the evaluation period. However, the conditional keeper remains OFF if the dynamic node is discharged to the ground. CKD logic has some problems like limitations on decreasing delays of the inverters and the NAND gate for improving noise immunity. Noise immunity can be improved by upsizing delay inverters, but this significantly increases power dissipation [10-12].

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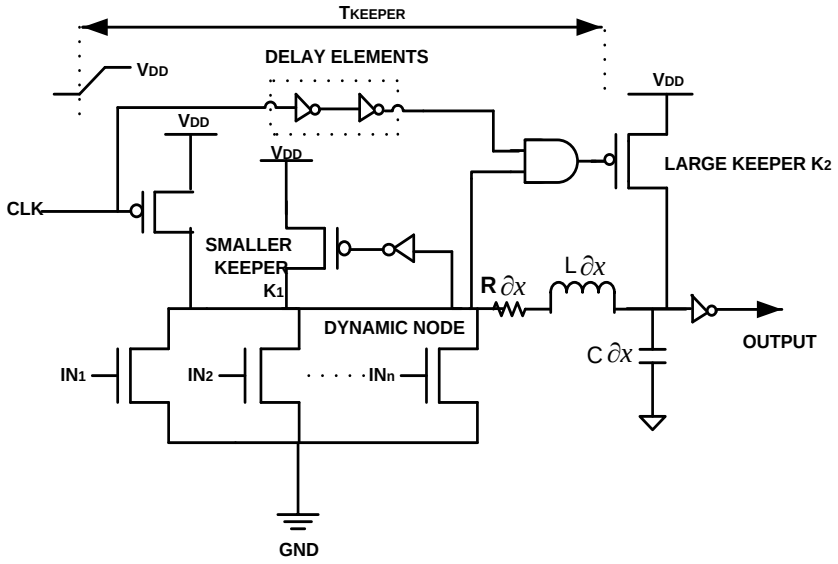

Fig.6: A Wide Fan-in Conditional-Keeper Domino [CKD]

2.3. Diode-footed domino

Another approach presented for reduced leakage current, enhancing the performance and better robustness is Diode-Footed Domino as shown in Fig 7. In the circuit, M_1 is diode footer, which is in series with the evaluation network. Leakage current is reduced by M_1 due to the stacking effect. Also M_1 increases the switching threshold voltage of the gate and therefore it increases the noise immunity. The mirror transistor and current feedback enhancing the robustness of the circuit against sub-threshold leakage and input noise in deep submicron range [13-15].

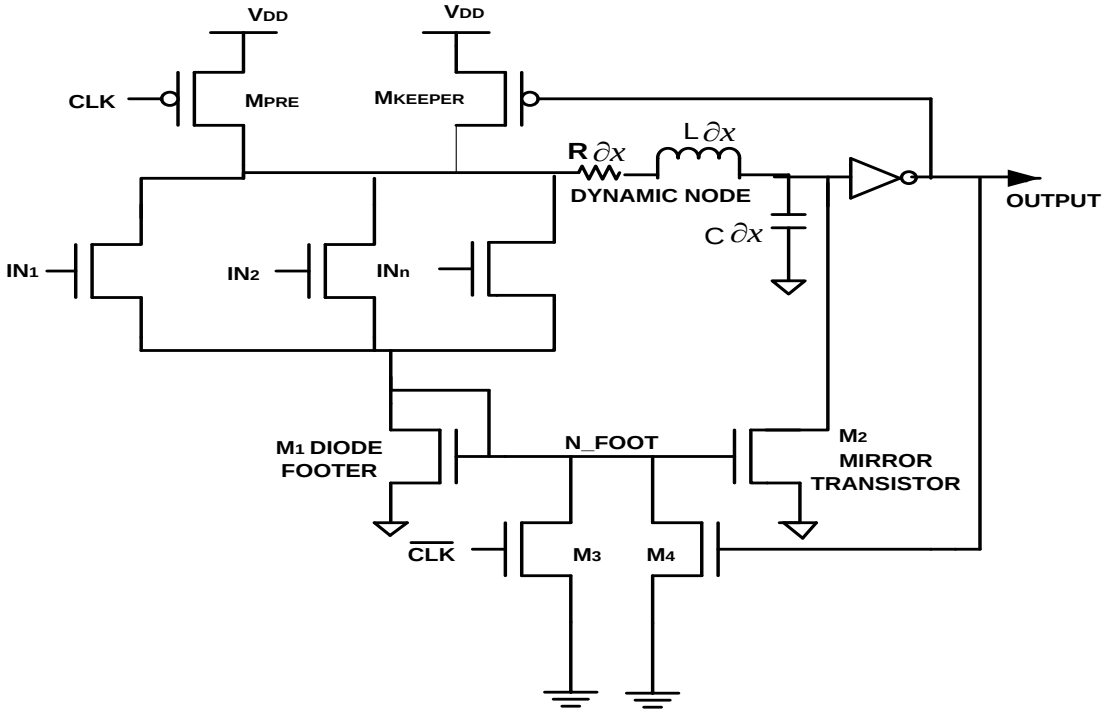

Fig.7: Wide OR Gate Using Diode-Footed Domino

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III. NOISE (LEAKAGE) IMMUNITY METRIC

For measurement of the robustness of the RLC domino circuit, we have applied an identical pulsesto all the inputs of wide fan in OR gate in the evaluation phase, and we measure amplitude of the output of the inverter to measure the UNG of the circuit. In this measurement, the duration of the pulse is kept constant at 40ps andthe same amplitude at the output is measured with applying different input till it achieve same output logic noise. The metric we use for leakage and noise robustness comparison is the unity noise gain (UNG), defined as the amplitude of the input noise that causes the same amplitude of noise at the output.

$$UNG = \{ V_{noise}; V_{noise} = V_{out} \}$$

We use a pulse noise to simulate cross-talk type of noise at the input. The effective noise depends on both the amplitude and duration of the noise pulse. The input noise level can be increased by increasing either the noise pulse duration or amplitude. In our experiments, we change the input noise level by changing its amplitude [16-19].

IV. PROPOSED CIRCUIT

The proposed circuit with RLC interconnect is designed for low power consumption and faster operation in which the delay of circuit is reduced exponentially. The exponential reduction of the delay reduces the power-delay-product (PDP) of the circuit. It takes the advantage of the semi dynamic logic, in which the source of the NMOS buffer transistor is connected to the drain of NMOS clock transistor instead of ground; it operates in semi dynamic state. Also the diode footer decreases the leakage and certain drawbacks of the circuit are further compensated by the presence of the current mirror circuit.

4.1. Circuit Analysis

The proposed RLC interconnect based new domino circuit scheme is shown in Fig.8, the transistor M_4 (complementary clock NMOS) is used as stacking transistor. Due to voltage drop across M_4 gate to source voltage of NMOS transistor in the Pull Down Network (PDN) decreases (stacking effect). The proposed circuit in which the evaluation transistor M_3 with gate connected to the clock; the purpose of M_3 in proposed scheme causes the stacking effect and make gate to source voltage of M_2 smaller (M_2 less conducting).

The mirror transistor M_1 is used as a diode. To make the diode footer, the drain and gate terminal of three transistors are shorted. Due to voltage drop across M_1, gate to source voltage of NMOS transistor in PDN decreases. M_1 has voltage drop due to presence of noise signal, M_2 start leaking that causes the circuit to dissipate power and also make it less noise robust. The purpose of transistor M_3 in proposed scheme causes the stacking effect and make gate to source voltage of M_2 smaller. Due to stacking effect of diode footer, the sub-threshold leakage current decreases and there is a voltage drop across the diode footer in evaluation phase. Due to this voltage drop V_{gs} becomes negative, this cause exponential reduction in threshold voltage.

The disadvantage of the diode footer is that, it increases the switching threshold voltage of gate by threshold of NMOS and new threshold voltage is about $2V_{tn}$ of the original, so there will be a

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performance degradation of the circuit the performance degradation is then optimized by putting a current mirror in the circuit [18-19].

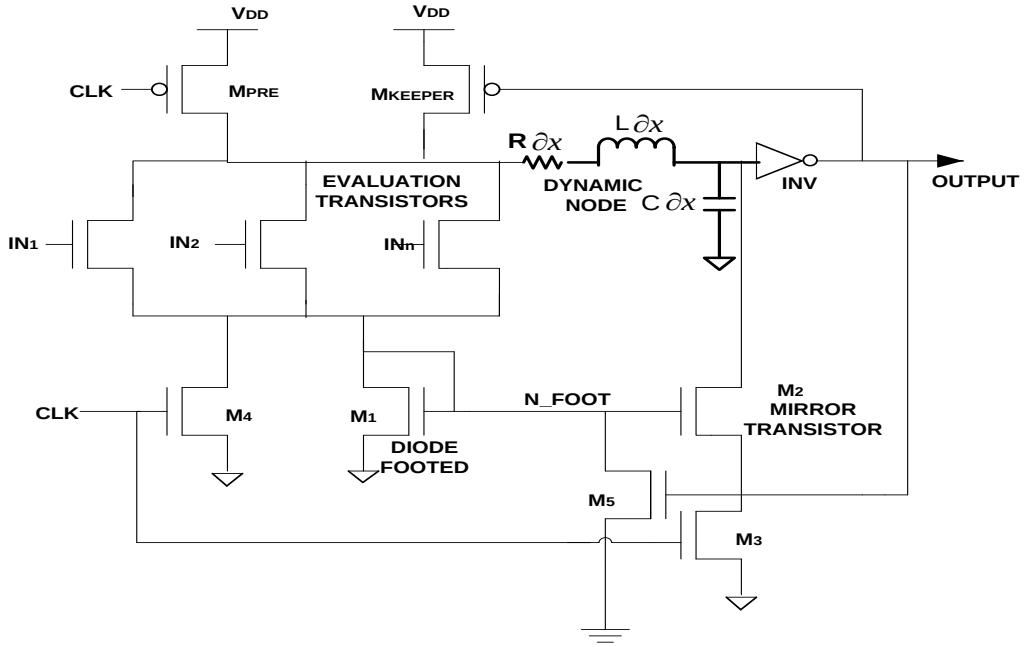

Fig.8: Proposed Domino Logic

The total evaluation current is the summation of current flow in pull down network and mirror current is summarized as:

$$I_{Total\ eval} = I_{PDN} + I_{Mirror}$$

I_{Total_eval}= Total evaluation current.
I_{PDN} = Current trough the evaluation network.
I_{Mirror} = Current through the mirror transistor.

The two phase of the proposed circuit is explained below:

4.1.1 Precharge phase

In the pre-charge phase clock voltage is low (clock=0 in Fig.6). Pre-charge transistor M_{pre}will conduct and turns ON, the keeper $M_{keeper}$is initially OFF. Therefore, the voltage of the dynamic node is raised to the high level by the pre-charge transistor (M_{pre}). When dynamic node voltage is at high level which is connected with RLC interconnects, the output of the inverter switch at low level and the keeper transistor turns ON. If the evaluation network is not ON the discharging of RLC interconnect dynamic node through evaluation network will not take place. In this phase the leakage current is decreased due to stacking effect since the minimum voltage of a MOS transistor in diode configuration is equal to $V_{GS}=V_{ds}=V_{tn}$, where V_{tn} is the NMOS threshold voltage.

4.1.2 Evaluation phase

In the evaluation phase clock is high (clock=1 in Fig.6) transistor M_{pre} turns OFF and transistor M_4 turns ON, whose gate is connected with the complementary clock and transistor is footed in the

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evaluation network. Firstly, if all the inputs of the evaluation transistor are low no discharging of the dynamic node takes place. The input of the inverter will be low and the output will be high verifying the OR operation of the circuit. In the second case, if at least one input in the pull down network is high the dynamic node gets discharged through the evaluation network and the input of the inverter will be set low and output node will be high again verifying the operation of OR gate. The current of PDN is higher than the mirror current M_1 is in the series with the evaluation network so the leakage current is reduced by M_1 due to stacking effect. M_1 transistor increases the switching threshold voltage of the gate and thereby improving noise immunity. The transistor M_2 and M_3 are connected in series to further reduce the leakage current, M_3 is driven by the clock of the NMOS transistor to increase the robustness and enhancing the speed of the circuit. The M_2 and M_3 transistors are connected in series, which reduces the leakage current when the dynamic node is not discharged and increases the robustness, enhancing the speed and the proper logic level is achieved as shown in Fig.9.

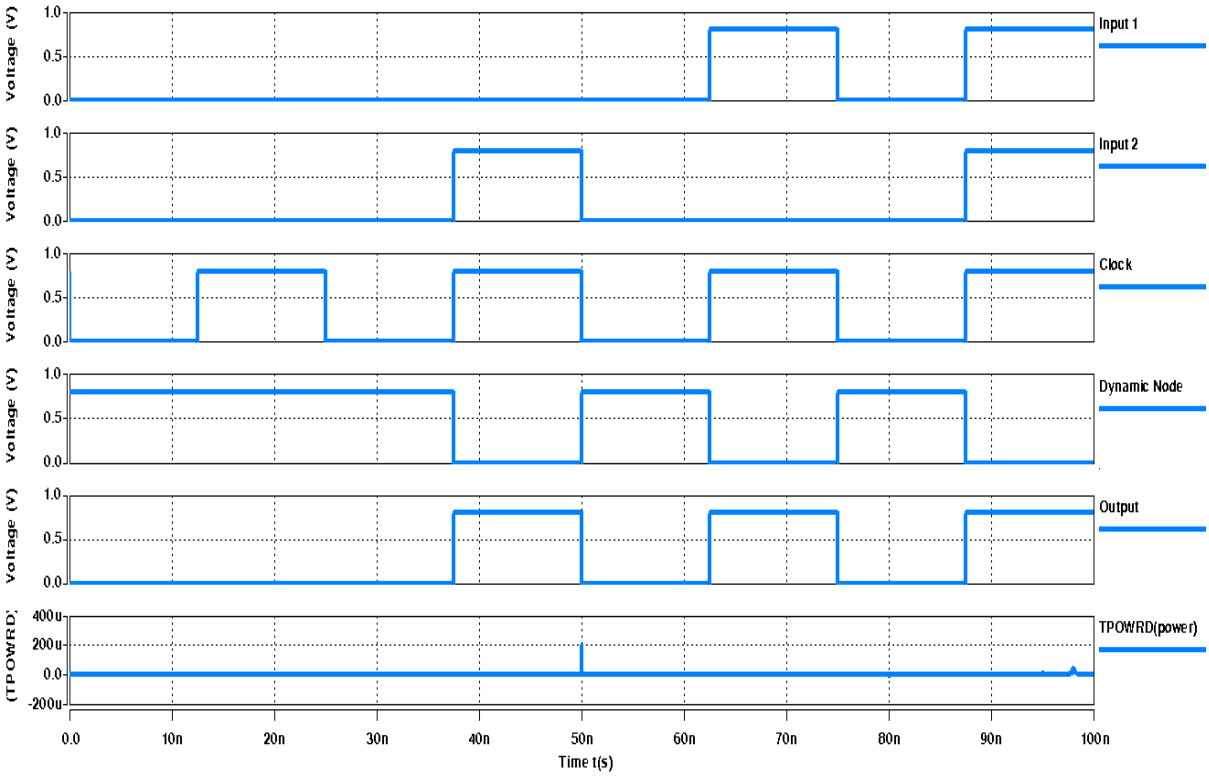

Fig.9: Transient characteristics of 2-input ULPS-DPC domino OR gate using HSPICE (the X-axis shows the simulation time in nanosecond and Y-axis shows the voltage in watts) at 10 MHz

Suppose if any or all the inputs are high the dynamic node is discharged through the active transistors. The output of the inverter is change from low to high transistor MP_2 turns OFF, transistor MN_3 is ON and the gates of M_k is directly connected to source of MP_2 through the channel of MN_3 turning M_k OFF, hence the supply rail V_{dd} is disconnected to dynamic node and high logic is achieved at the output verifying the OR operation.

V. SIMULATION RESULTS AND COMPARISON

Circuits are simulated using HSPICE simulator at temperature of 27^0C in 32 nm technology for bulk CMOS. Channel length is 32nm and width taken for simulations for keeper is 0.25 µm, PMOS 5 µm, NMOS 2.5 µm and load capacitance of 1f F, supply voltage V_{dd} used is 1V. For the noise-tolerance

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measurement, Unity Noise Gain (UNG) noise pulse width 50 ps (higher than gate delays) are taken and noise-voltages are applied to all inputs. TABLE I and II shows the UNG normalized to V_{dd}=1V and Power-Delay Product (PDP) for different schemes of OR gate with fan-in gate 8 and16 inputs. The comparison of UNG for 8 and 16 inputs OR gate are shown in Fig.10.Transistor M_2 plays a crucial role in terms of leakage and performance of gate in the proposed scheme. It provides the best UNG and power delay product.

TABLE 1: Comparison of power, propagation delay, power delay product, UNG, standby power, evaluation delay, short circuit current and no. of transistors for 8 input fan-in gate with inteconnects

Parameters	Footer less diode	Footed diode	High speed domino	Conditional keeper domino	Wide OR gate domino	Proposed circuit
Power (µW)	2.5714	3.023	501.19	287.91	3.4117	2.9863
Normalized power	1	1.175	194.90	111.96	1.3267	1.1613
Propagation delay (ps)	12.125	21.43	11.797	14.313	19.96	20.173
Normalized propagation delay	1.0278	1.816	1	1.2132	1.6929	1.7100
Power delay product (aJ)	31.160	64.79	5910	4120	68.105	60.244
UNG	0.298	0.327	0.2962	0.3079	0.329	0.3441
Normalized UNG	1	1.109	0.993	1.033	1.104	1.154
Standby power (µW)	1.314	0.798	505.33	286.49	1.149	0.924
Normalized Standby power	1.6451	1	632.690	358.695	1.4385	1.1568
Evaluation delay (ps)	8.94	14.40	8.288	11.397	13.903	13.820
Short circuit current (nA)	7.652	7.654	58.267	4.558	4.558	7.6533
No. of transistors	12	13	18	23	16	17

TABLE 2: Comparison of power, propagation delay, power delay product, UNG, standby power, evaluation delay, short circuit current and no. of transistors for 16 input fan-in gate with inteconnects

Parameters	Footer less diode	Footed diode	High speed domino	Conditional keeper domino	Wide OR gate domino	Proposed circuit
Power (µW)	3.688	5.333	502.1	288.9	4.834	4.112
Normalized power	1	1.445	136.144	78.335	1.310	1.114
Propagation delay (ps)	14.72	28.94	14.55	16.77	23.66	17.69
Normalized propagation delay	1.011	1.989	1	1.1525	1.6261	1.2158
Power delay product (aJ)	54.30	154.33	7308.0	4845.00	144.43	72.760
UNG	0.271	0.315	0.277	0.2795	0.317	0.322
Normalized UNG	1	1.162	1.022	1.031	1.169	1.188
Standby power (µW)	2.059	2.602	5.014	2.874	1.761	1.852
Normalized Standby power	1.1692	1.477	2.847	1.632	1	1.051
Evaluation delay (ps)	12.09	17.54	11.96	14.54	17.98	19.00
Short circuit power (nA)	7.628	7.652	7.654	58.28	7.6533	7.6533
No. of transistors	20	21	26	31	24	25

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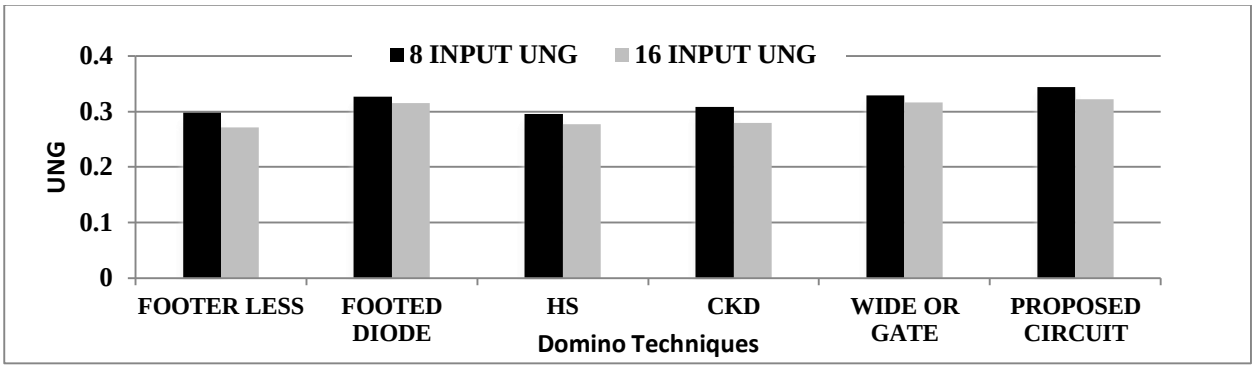

Fig. 10: Comparison of UNG for 8 and 16 inputs OR gate

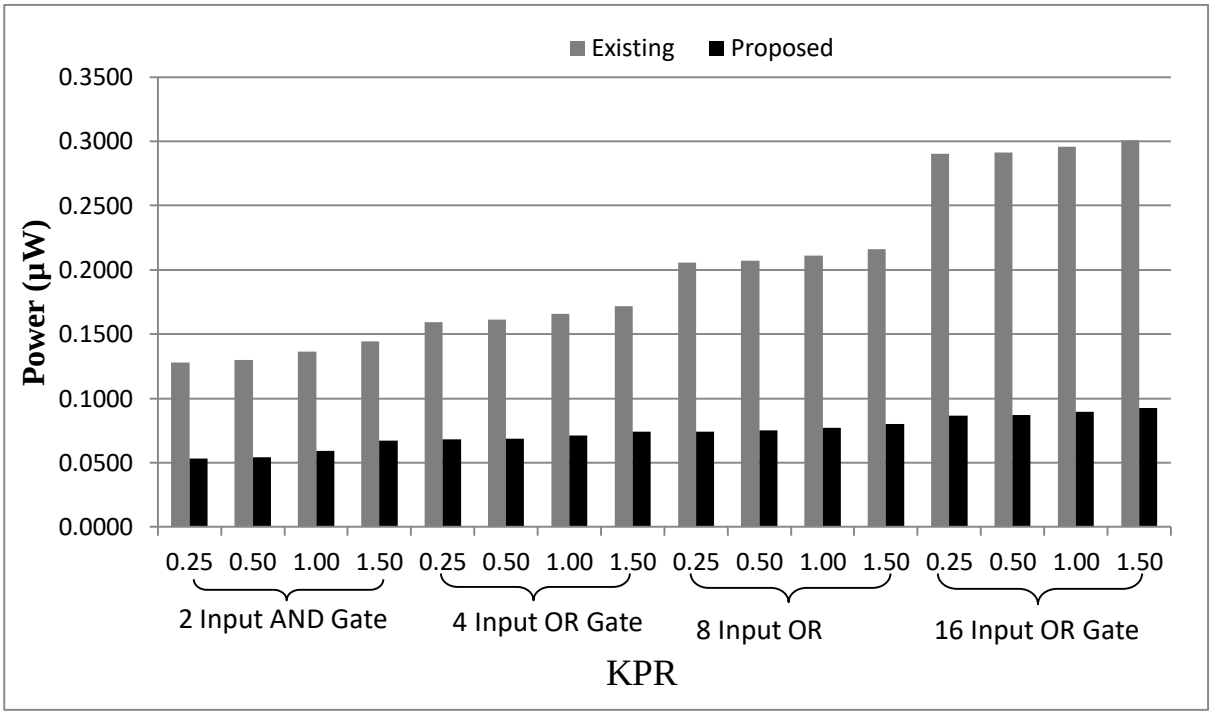

Fig .11: Comparison of power consumption in existing and proposed circuit with different keeper Ratio (KPR) (n-type: W/L = 1, p-type: W/L = 2)

The simulation results of the proposed circuit for power consumption and delay at the different keeper ratios is shown in Figs. 11, respectively. The power consumption is significantly reduced up to 68% (16-input OR with KPR=1.5) with the proposed technique when compared with the proposed CMOS technique, as shown in Fig. 10.

VI. CONCLUSION

In this paper a new circuit for the domino logic with RLC interconnects is proposed which is robust and noise tolerant. The existing and proposed circuits are simulated using HSPICE simulator with 45nm Predictive Technology Model (PTM) for bulk CMOS model card at the power supply of 1V for 8 and 16 inputs for wide fan-in OR gate. The simulation results is then compared showing an improvement in UNG from 1.12 to 1.18 times and exhibits 89% to 99% low PDP for 8 bit and 16 bit OR gate at the cost of 18% to 41% delay. The proposed circuit can be used in design of high-speed embedded processors where low power consumption is an essential requirement. The proposed circuit

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also shows noise efficiency compared to previous work in the literature. The circuit is flexible and quite applicable for large fan-in gates.

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ISSN: 2005-4238 IJAST
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