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Analytical Model of the Surface and Center Potential for GAA Si-Nanowire MOSFETs

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Abstract

Integrated circuits are in demand to be invetigated for its economical performance. Therefore, it is vialbe to experiment on ternary based operations[7]. A ternary half adder based on ternary multiplexer and logic primitives is proposed and its performance is analyzed in detail. This proposed ternary half is sensibly designed with the simplified expressions using the ternary k-map. The combinational logic blocks for the SUM and CARRY are designed, verified, constructed and simulated with Tanner EDA (130nm) at 1.2 V. Analytical modeling of potential distribution has been derived by using Poisson equation for short channel gate all around (GAA) Si-nanowire MOSFET. The architecture of the proposed device based on equal number of gates have been utilized to calculate effective natural length (λc). Comparison of center and surface potential along the channel length have been obtained by using ENL based on Poisson equation with suitable boundary condition. Further to investigate the Figure of merits, such as ON/OFF current, DIBL, subthreshold slope and threshold voltage is done by using different silicon thickness. The effect of physical devices parameters such as radius of silicon (tSi), gate oxide thickness (tox) ,total channel length (L) and drain biases (Vds) have been investigated on the devices by using MATLAB

Keywords: *-DIBL; GAA; SCE; Subthreshold slope*

1 Introduction:

For further miniaturization of CMOS devices, many devices structure has been explored [1-2] , like Fin-gate, pi gate, double gate ,tri-gate etc , which follow Moore's law CMOS transistors for continue scaling of devices feature size provide increase packing density improves the circuit performance and lower power consummation [3-4]. Multiple-gate SOI MOSFETS i.e. double, triple or quadruple gate devices were proposed by J . P. colinge et . *al*; [5], which claimed these devices offered high current drive and optimal short channel effects (reduce DIBL and SS). B . Iniguez et.al.[6] proposed a compact model for Multiple-gate SOI MOSFETS considered different transport models (drift-diffusion and quasi-ballistic models) and claimed that this model provides smooth transition between different operating regimes. Among these GAA Si-NW is attracting device which brought broad attention from semiconductor industry in order to enable further scaling and improve the transistors performance, multiple gate improve sub threshold slope, reduce ballistics transport of carrier near Si-Sio_2 interface as compare to other planer [7-8-9]. Due to small geometry of GAA get better the short channel 8641effects, low leakage current and enhance the gate controllability and reduce natural length and improve surface to volume ratio. Iwai Hiroshi et.al; [10] presented Si Nanowire FET and its modeling which provided high drain current and off leakage control.

In this paper, the analytical expression of center & surface potential is derived and ENL has been solved by 3-D Poisson equation in channel region with appropriate boundary condition. After calculating center

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and surface potential it has been formulated minimum potential. This paper is divided into many sections along with introduction. Section-2 describe devices structure and simulation description that includes all dimension materials and doping of Si-NW-GAA. Section-3 explains analytical modeling of centre and surface potential and sections-4 includes model verification, results and discussion.

2 Devices Structure And Simulation Description

Figure (1) simulated 3-D of Si-NW GAA MOSFETs structure used for modeling and simulation. The main parts are source, drain, channel, gate oxide and metal gate contact like conventional MOSFETs. Longitudinal and transverse direction are assumed along the X axis and Z axis of cylinder shown in fig (1). Na are doping concentration in channel region and Nd are uniform doping concentration in source and drain region. Channel length L=30nm and radius t_{Si}=10nm is choose in such a way that quantum mechanical effects are negligible. Oxide thickness t_{ox}=2nm are chose that avoid tunneling effect.

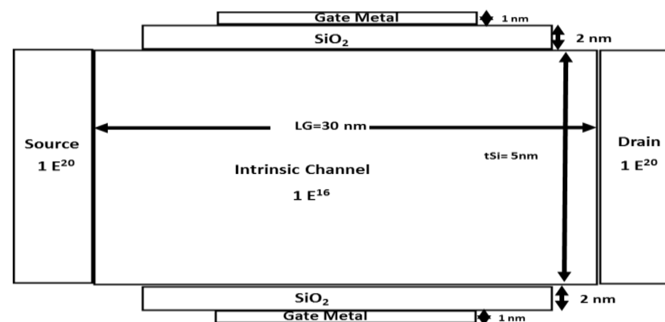

Figure 1: 3-D cross sectional view of GAA Si-NW MOSFET

Transfer characteristics of drain current and gate voltage (Id-Vgs) are plotted at different radius such as 15nm,10nm,8 nm at V_{DS}=0.1V and 1 V is obtained from 3D simulator genius semiconductor tool as shown in fig (2), it is observed that reduction in leakage current obtained due to down scaling of the silicon thickness.

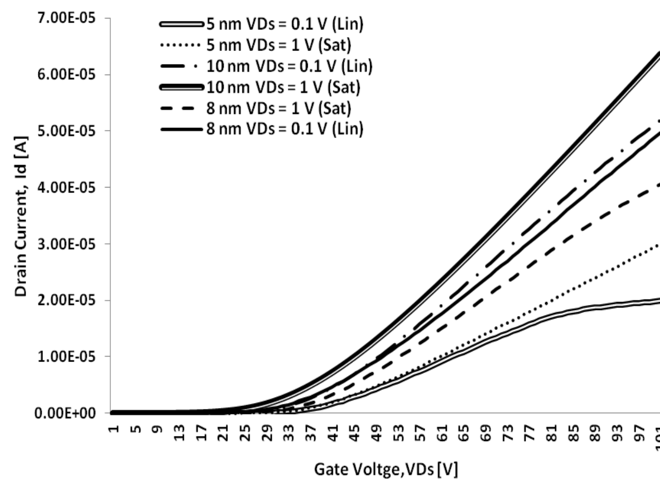

Figure 2: Id-Vgs characteristics at Silicon thickness tSi 5nm,8nm,10nm VDS=0.1V and 1V

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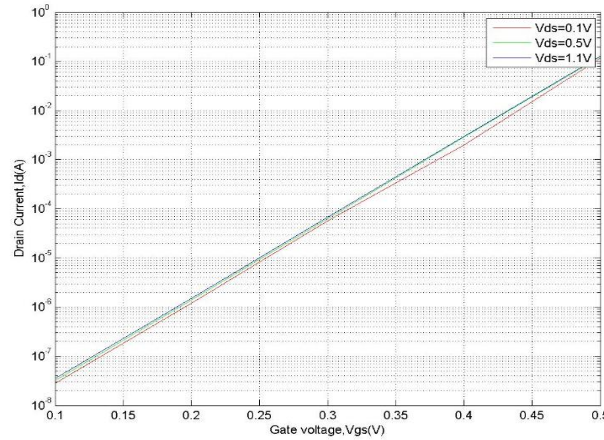

Figure 3: Id-Vgs characteristics at VDS=0.1V,0.5V and 1V(Linear scale)

Analytical drain current observed with different drain biases as evident shown in Figure (3)

Table 1 Various Performance Metric of SCEs for GAA-NW-MOSFET at Silicon Thickness 5nm, 8nm, 10nm

Parameter/Device	nMOS GAA-NW device t_{Si} = 5 nm	nMOS GAA-NW device t_{Si} = 8 nm	nMOS GAA-NW device t_{Si} = 10 nm
Wg (µm)	0.0314	0.5024	0.0628
Lg (µm)	0.03	0.03	0.03
Vth Lin (V)	0.363915	0.357741	0.242555
Vth Sat (V)	0.341765	0.325551	0.175798
DIBL (mV/V)	0.0246116	0.0357664	0.0741747
SubSlope Lin (mV/dec)	63.9329	69.426	76.0762
SubSlope Sat (mV/dec)	63.7913	71.2174	82.6831
ON Current (A)	2.17E-05	4.06E-05	5.02E-05
OFF Current (A)	$2.58E^{-13}$	$3.22E^{-11}$	$1.60E^{-10}$

The comparison of various performance metric of SCEs for GAA-NW-MOSFET at different silicon thickness 5nm,8nm,10nm it was manifested that silicon thickness 5nm offered better result in terms of ON/OFF current which in order of 10^{-05} to 10^{-13} , reduction of leakage current improve the performance and reliability of the device and subthreshold slope was very close to ideal value 63.79 mV/dec which is very helpful for switching applications, decline the DIBL which improve the controllability of the gate on the channel and increase the threshold voltage essential for conducting the device as evident in table 1.

Work function of gate materials are (4.7ev). table-2 show the list of parameter used in simulation.

This work accomplished by fabricating device in devices simulator achieved by Drift diffusion model carrier transport model ,Shockley- read –hall carrier recombination model combined has been chosen for developed the structure of devices in various regions and doping profile obtained by mobility model using tcad simulators Editor. All electrode were defined with respective boundary condition. Equation of

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the devices and thermal equation has been solved by Self–consistently, possion equation, continuity equation and Netwon method. All simulation work is based upon the assumptions that the structure the junction unexpected at room temperature for different biasing condition. We analyzed the device parameters on the surface potential and threshold voltage by selecting the simple polynomial approximation to reduce computational complexity.

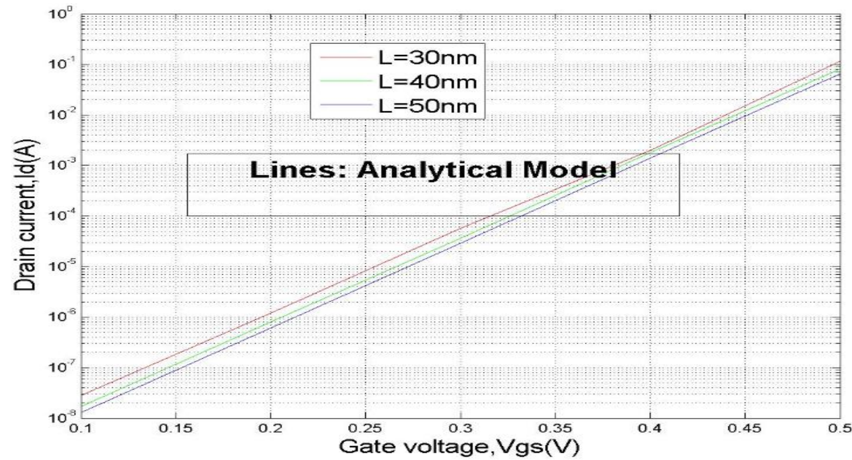

Figure 4: Leakage current variation with different channel length L=30nm,40nm,50nm

Analytical leakage current observed with variation of different channel lengths 30nm,40nm,50nm respectively. Result reveled that lowest leakage current at channel length 30nm.

Table 2 Parameters Used for Simulations Purpose

Symbol	Parameters	Value
ε_{0x}	Oxide Permittivity	$3.9\times \varepsilon_0$
ε_{Si}	Silicon Permittivity	$11.8\times\varepsilon_0$
ε_0	Permittivity of vacuum	$8.85\times10^{-12F/m}$
t_{si}	Thickness of silicon film	10nm
t_{ox}	Gate Oxide thickness	2nm
L	Total length	30 nm
VT	Thermal voltage	0.0256 V
N_a	Concentration for Acceptor ion	10^{16} cm−3
N_d	Concentration for Donor ion	10^{20} cm−3
φ_M	Metal work function	4.6eV
K	Boltzmann Constant	1.38×10^{-23} j/k
T	Temperature in Kelvin	300 K
Q	Electrical charge	$1.6\times10\text{-}^{19}$

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3 Analytical Center And Surface Potential Model

By using 3-D Poisson equation in the GAA MOSFETs the potential distribution $\varphi(r,z)$ in the channel region has been obtained in cylindrical coordinate system of GAA Si-NW MOSFETs

$$\frac{1}{r}\frac{d}{d_r}(\mathrm{r}\frac{d_\varphi(r,z)}{d_r}) + \frac{1}{r^2}\frac{d^2\varphi(r,z)}{d_\theta{}^2} + \frac{d^2\varphi(r,z)}{d_z{}^2} = \frac{qN_a}{\varepsilon_{si}} \quad (1)$$

Where φ is the electrostatics potential of the longitudinal and transverse direction in the channel region [10], θ is negligible in GAA Si- NW MOSFET, then modify equation (1) can be rewritten

$$\frac{1}{r}\frac{d}{d_r}(\mathrm{r}\frac{d_\varphi(r,z)}{d_r}) + \frac{d^2\varphi(r,z)}{dz^2} = \frac{qN_a}{\varepsilon_{si}} \quad (2)$$

The solution of this as a simple parabolic function

$$\varphi(r,z) = a_0(z) + a_1(z)r + a_2(z)r^2 \quad (3)$$

Where a_0, a_1, a_2 are coefficient of that is z dependent function can be found by boundary condition as follows:

1. The potential at the body center φ_c given by $\varphi(r,z)|_{r=0} = \varphi_c$(z) (4)
2. The potential at the surface φ_s given by

$$\varphi\left(\frac{t_{si}}{2}, z\right)\Big|_{r=\frac{t_{si}}{2}} = \varphi_s(\mathrm{z}) \quad (5)$$

The potential at source channel and drain channel interface respectively given by

$$\varphi(r,0)|_{r=0} \qquad V_{bi} \quad (6)$$

$$\varphi(r,L)|_{r=0} \qquad V_{bi} + V_{ds} \quad (7)$$

Where V_{bi} is the inbuilt voltage between source /drain and silicon channel junction and V_{ds} is biasing drain to source.

$$V_{bi} = V_T \log (N_a N_d/ni^2) \quad (8)$$

Electrical field distribution at the Si-SiO_2 interface of center and surface potential are:

a. Center potential can be formulated by putting r=0 in equation(3)as given below:

$$\varphi(r,z)|_{r=0} = 0,\ \varphi(0,z)|_{r=0} = \qquad 0\ \varphi_c(\mathrm{z}) = a_0(z) \quad (9)$$

b. Electrical field in the Center of silicon pillar is zero by symmetry

$$\frac{d_\varphi(r,z)}{d_r}\Big|_{r=0} = a_1(z) \quad (10)$$

c. The electrical field at the silicon oxide interface can be derived from the gate potential $\varphi_{gsi} = V_{gs} - V_{fb}$,where V_{fb} is the channel flat band voltage of silicon film i.e. $V_{fb} = \varphi_M - \varphi_{si}$ (metal work function & silicon work function). $\varphi_{si} = \chi_{si} + E_{g\text{-}}si/2 + KT/q$

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IN(N_a/ni) , So surface potential $\varphi(r,z)$, gate oxide thickness

$$t_{ox1}= \frac{t_{si}}{2} In\left(1+\frac{2t_{ox}}{t_{si}}\right)$$

and silicon thickness are as below

$$\left.\frac{d_{\varphi}(r,z)}{d_r}\right|_{r=\frac{t_{si}}{2}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{(Vgs-Vfb-\varphi(r,z))}{t_{ox1}} \quad (11)$$

The coefficient of equation (3) can be found by using this boundary condition i.e. a_0 as below

$$\varphi(r,z)|_{r=0} = 0=\varphi_c(\text{z}) = a_0(z) \quad (12)$$

Coefficient a_1 can be found by differentiating equation (3) w.r.t. 'r' and equating the equation (10) , then we get $\left.\frac{d_{\varphi}(r,z)}{d_r}\right|_{r=0} = 0 + a_1(z) + 2r\, a_2(z) = a_1(z)$ (13)

Now equation (3) becomes after putting equation (13), we get

$$\varphi(r,z)= a_0 (z) +a_2(z)\, r^2 \quad (14)$$

Again differentiating equation (14) w. r. t 'r' and solve by using boundary condition and then find the coefficient value of a_2

$$a_2(z)= \frac{1}{2r} \frac{d_{\varphi}(r,z)}{d_r} \quad (15)$$

putting equation (11) in equation (15) then we get

$$a_2 (z)= \frac{(V_{gs}-V_{fb-}\varphi_c(z))}{\frac{t^2{}_{si}}{4}(1+\frac{4\, t_{ox1}}{t_{si}}\frac{\varepsilon_{si}}{\varepsilon_{ox}})}$$

where $\lambda c = \frac{4\, \varepsilon_{ox}}{(t^2{}_{Si}\ \varepsilon_{ox}+2\varepsilon_{si}\log(1+\frac{2t_{ox}}{t_{si}}))}$ λc *is natural length*

$$a_2(z)=\frac{1}{\lambda c}(V_{gs} - V_{fb-}\varphi_c(z)) \quad (16)$$

now put equation (16) in equation (14), then we get

$$\varphi(r,z)=\varphi_c(z)+\frac{1}{\lambda c}\left(V_{gs} - V_{fb} - \varphi_c(z)\right)r^2 \quad (17)$$

With the help of equation (2) we can find the center potential at 'r=0' by using boundary condition and above expression, we can get

$$\frac{1}{r}\frac{d}{dr}\left.\left(r\frac{d_{\varphi}(r,z)}{d_r}\right)\right|_{r=0} + \left.\frac{d^2}{dz^2}\varphi(r,z)\right|_{r=0} = \frac{qN_a}{\varepsilon_{si}} \quad (18)$$

The equation (18) non-homogenous can be solved by boundary condition and other expressions, we get central potential

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$$\varphi_c(r,z) = \text{A}\, exp^{\,2\sqrt{\frac{1}{\lambda c}}\,z} + \text{B}\, exp^{\,-2\sqrt{\frac{1}{\lambda c}}\,z} + (V_{gs}-V_{fb}) -- \frac{\lambda c\, q\, N_a}{4\varepsilon_{si}} \quad (19)$$

The constant A & B can be found by using boundary condition from equation (6) & (7), then we get

$$\text{A=} \left[\frac{(V_{bi}-(V_{gs}-V_{fb}-\frac{\lambda c\, q\, N_a}{4\varepsilon_{si}}))(1-exp^{\,-2\sqrt{\frac{1}{\lambda c}}\,L})+V_{ds}}{2\sinh\left(\sqrt{\frac{4}{\lambda c}}\,L\right)}\right]$$

$$\text{B=-}\left[\frac{V_{ds}+\left(V_{bi}-\left(V_{gs}-V_{fb}-\frac{\lambda c\, q\, N_a}{4\varepsilon_{si}}\right)\right)\left(1-exp^{\,2\sqrt{\frac{1}{\lambda c}}\,L}\right)}{2\sinh\left(\sqrt{\frac{4}{\lambda c}}\,L\right)}\right]$$

Surface potential formulation

Surface potential 'r= t_{si}/2'could be calculated by utilizing equation (14-18) using the above boundary condition

$$\varphi_s(z)=\varphi_c(z)(1-\frac{t^2{}_{si}}{4\lambda c})+(V_{gs}-V_{fb})\frac{t^2{}_{si}}{\lambda c} \quad (20)$$

1. Minimum Center And Surface Potential Modeling

The position (Z_{min}) of Minimum surface potential can be calculated by differentiating the surface potential under boundary condition.

$$\left.\frac{d\varphi_c(z)}{dz}\right|_{z=Z_{min}}=0 \quad (21)$$

Z_{min} can be calculated by using equation (19) and (23) then we get

$$Z_{min}=\sqrt{\frac{\lambda c}{16}}\,\text{IN}\left(\frac{B}{A}\right) \quad (22)$$

then found minimum center potential by putting equation (22) in equation (19) , we get

$$\varphi_{c\,min}=\sqrt{AB}+(V_{gs}-V_{fb}-\frac{\lambda c\, qN_a}{4\varepsilon_{si}}) \quad (23)$$

A. Minimum surface potential formulation

$$\varphi_{s\,min}=\varphi_{c\,min}(1-\frac{\lambda c\, t^2{}_{si}}{4})+(V_{gs}-V_{fb})\frac{t^2{}_{si}}{\lambda c} \quad (24)$$

Putting Z_{min} value in equation (24) then we get

$$\varphi_{s\,min}=(V_{gs}-V_{fb})+(2\sqrt{AB}-\frac{\lambda c\, q\, N_a}{4\varepsilon_{si}})(1-\frac{\lambda c\, t^2{}_{si}}{4}) \quad (25)$$

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4 Results And Discussion

Results obtained from analytical modeling of surface and center potential were verified and plotted using MATLAB. It has been observed that center potential curves lies above the surface potential curves as shown in fig (5).

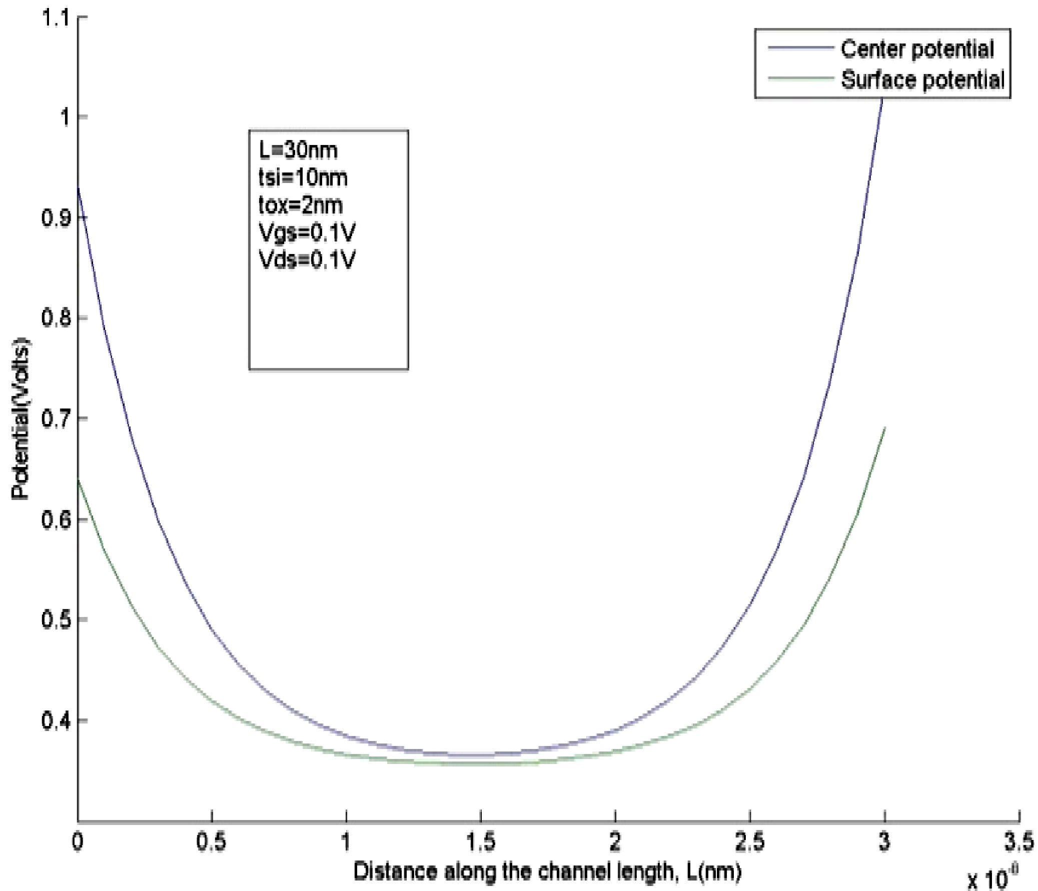

Figure 5: Potential versus distance along the channel length at the surface and center. Parameter used $\varphi_M = 4.6$eV, L=30nm, tsi=10nm Vgs=0.1V, tox=2nm, Na=1×1016cm-3, Nd=1×1020cm-3

In this fig (6) variation of the center potential versus channel length for different gate oxide thickness is shown. It has been observed that controllability of the gate over the channel is strong when the gate oxide thickness is reduced.

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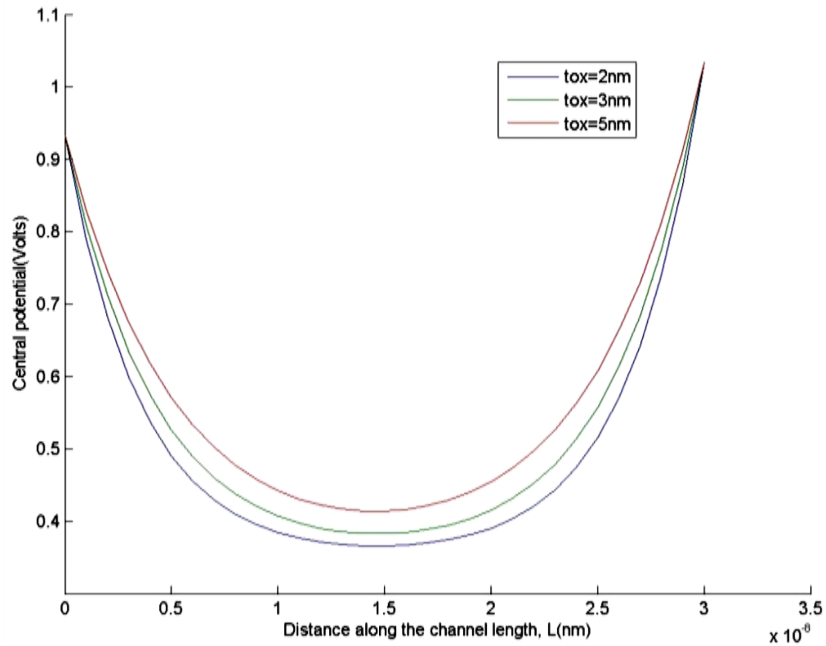

Figure 6: Center Potential versus channel length with different gate oxide thickness. Parameter used $\varphi_M = 4.6$eV, L=30nm, tsi=10nm Vgs=0.1V, tox=2nm, Na=1×1016cm-3, Nd=1×1020cm-3

In the Figure (7) variation of center potential versus the channel length for different silicon thickness is shown. It has been observed that reduction of silicon thickness reduces the value of center potential so that the controllability of the gate over the channel is improved and reduces SCEs

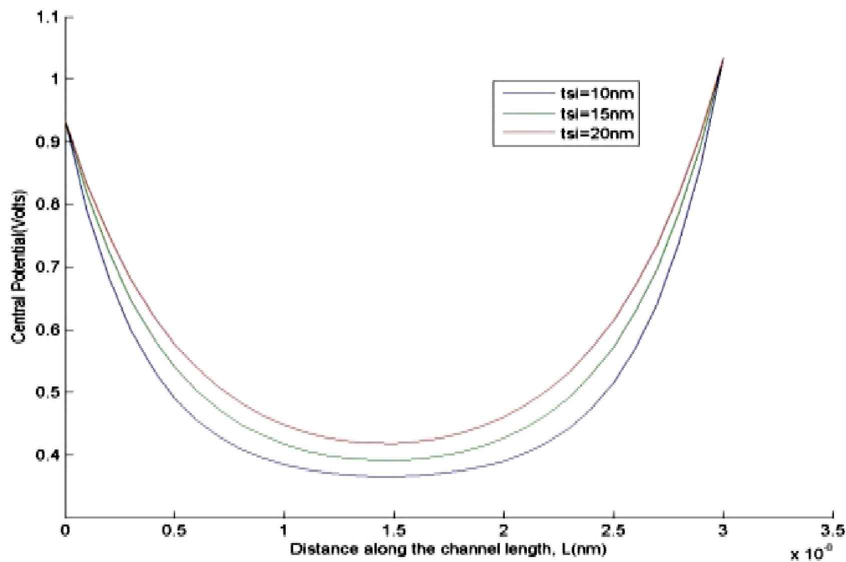

Figure 7: Center Potential versus the channel length with different silicon thickness. Parameter used $\varphi_M = 4.6$eV, L=30nm, tsi=10nm Vgs=0.1V, tox=2nm, Na=1×1016cm-3, Nd=1×1020cm-3

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In the Figure (8) variation of center potential versus the channel length for different drain voltage is plotted. It has been observed that increases the drain voltage increases potential.

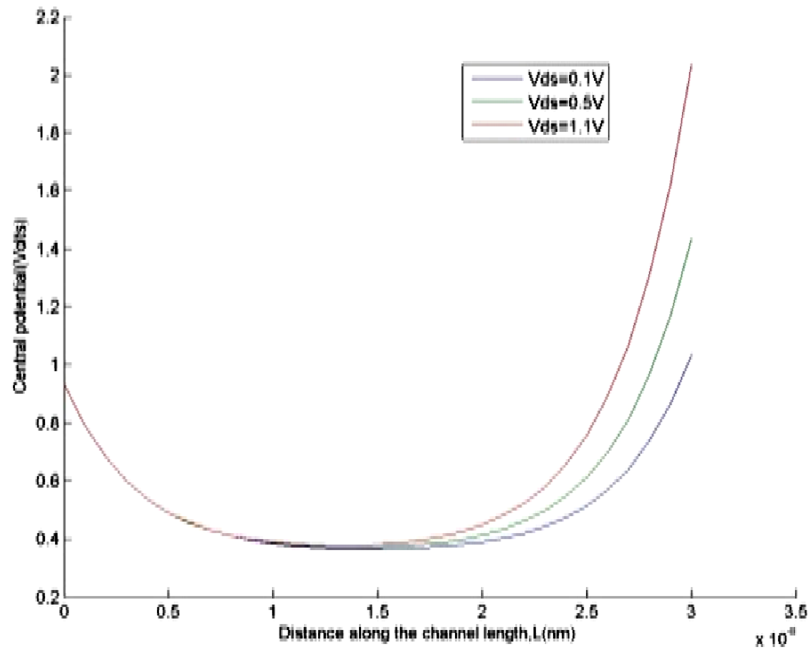

Figure 8: Center Potential versus the channel length with different drain biases. Parameter used φ_M = 4.6eV, L=30nm, tsi=10nm Vgs=0.1V, tox=2nm, Na=1×1016cm-3, Nd=1×1020cm-3

In the fig (9) variation of surface potential versus distance along the channel length is plotted.

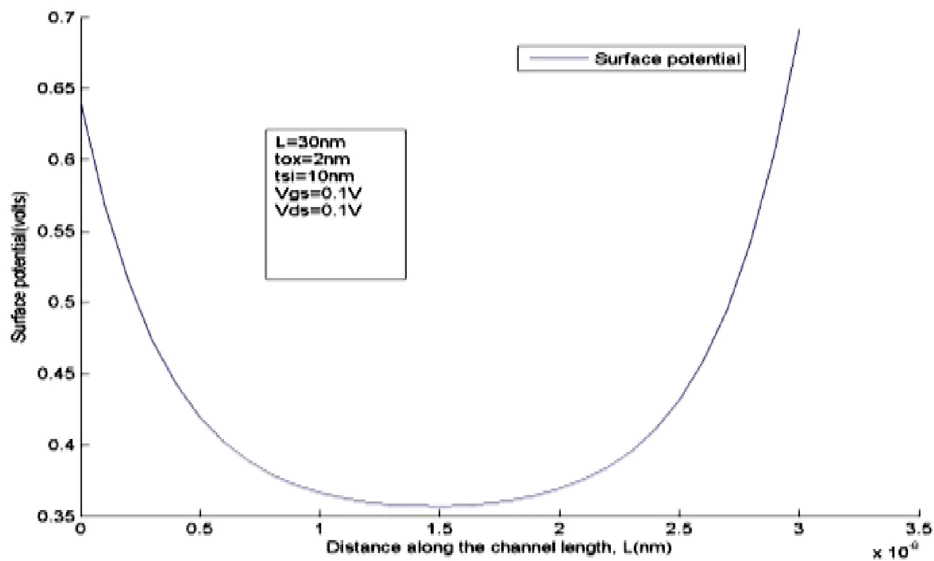

Figure 9: Surface Potential versus the channel length. Parameter used φ_M = 4.6eV, L=30nm, tsi=10nm Vgs=0.1V, tox=2nm, Na=1×1016cm-3, Nd=1×1020cm-3

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In the fig (10) variation of surface potential along the channel for different drain voltage is plotted.

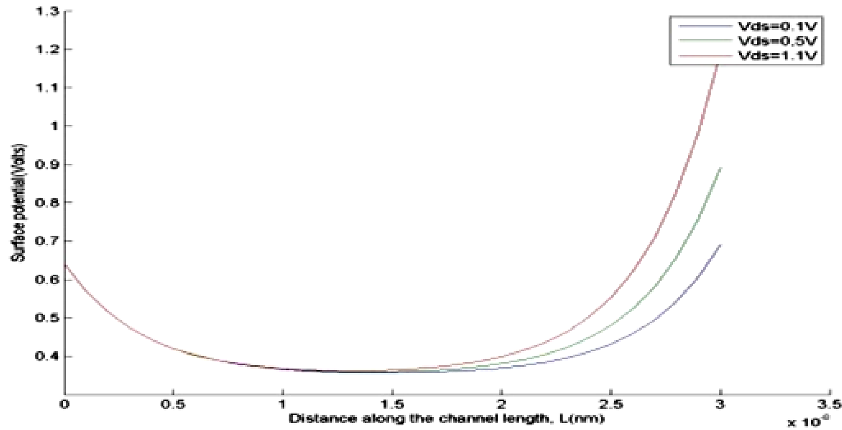

Figure 10: Surface Potential versus the different drain voltage Parameter used $\varphi_M = 4.6eV$, L=30nm, tsi=10nm Vgs=0.1V, tox=2nm, Na=1×1016cm-3, Nd=1×1020cm-3

In this fig (11) variation of the surface potential versus the channel length for different oxide thickness is plotted.

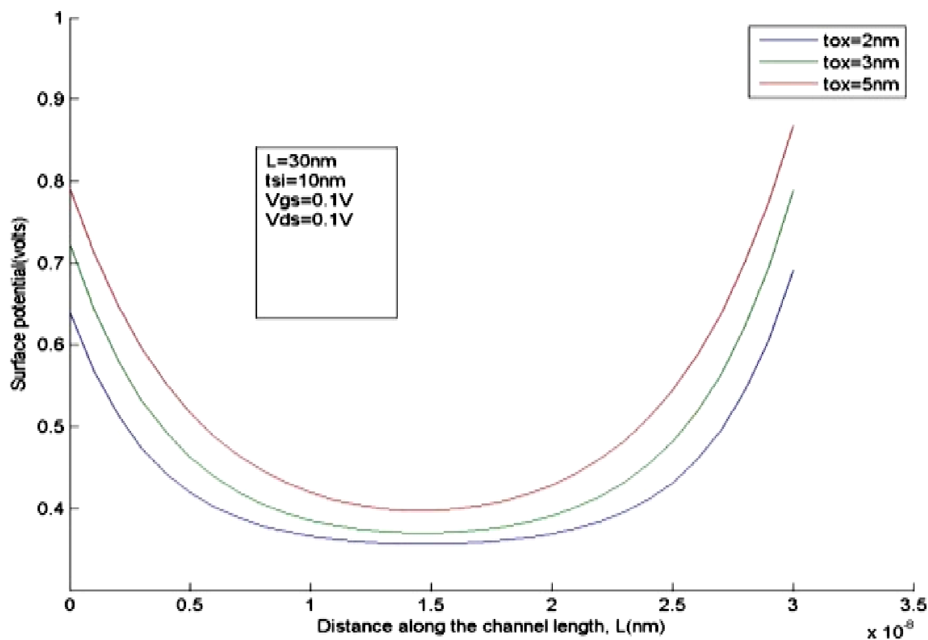

Figure 11: Surface Potential versus the different drain voltage Parameter used $\varphi_M = 4.6eV$, L=30nm, tsi=10nm Vgs=0.1V, tox=2nm, Na=1×1016cm-3, Nd=1×1020cm-3

DIBL effect can be easily observed in this Fig(12) as ploted against diametre of silicon film thickness its effect increase with the si-thickness increase.

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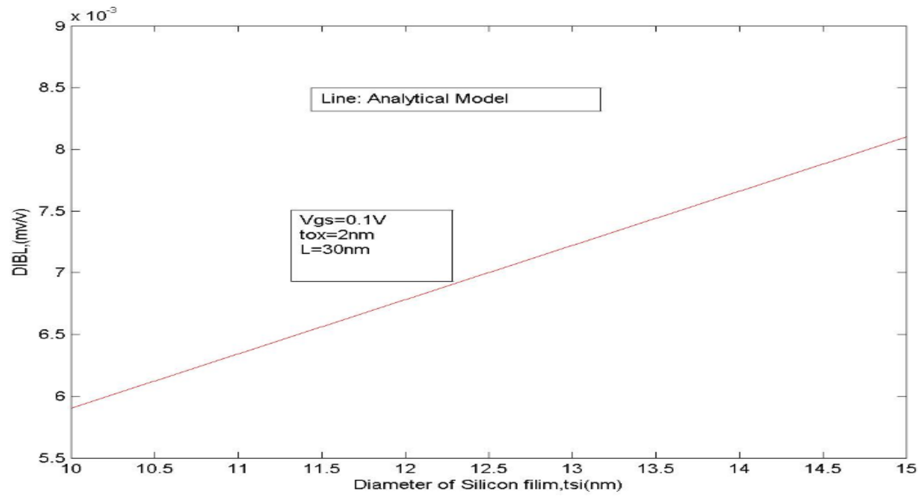

Figure 12: DIBL against silicon thickness. Parameter used $\varphi_M = 4.6eV$, Na=1*1016cm-3 ,Nd=1020cm-3

In this Fig(13) DIBL against diametre of oxide thickness it is observed that if we increase the oxide-thickness then increase the DIBL.

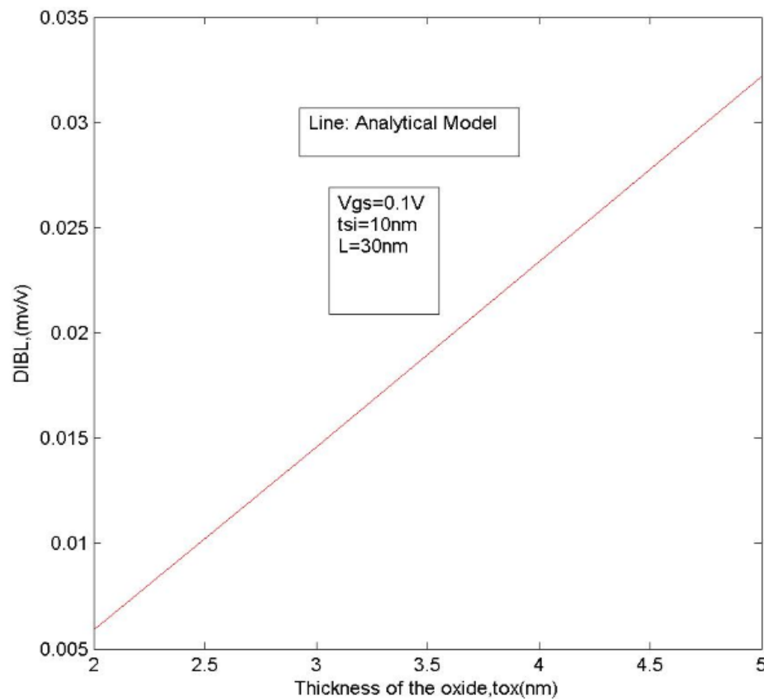

Figure 13: DIBL against thickness of oxide. Parameter used $\varphi_M = 4.6eV$, Na=1*1016cm-3 ,Nd=1020cm-3

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Table 3 Comparison Table of Minimum Center and Surface Potential and Zmin along the Channel Length**.**

φcmin	φsmin	Zmin	φM
0.3661	0.3570	1.4721e-^{8}	4.7

Table 3 shows the comparison of surface center potential. It has been observed that center potential lies above the surface potential.

5 Conclusıon

Analytical modeling of center and surface potential for GAA Si-NW-MOSFETs is expressed using 3-D Poisson equation in the channel regions. This paper present comparison of center and surface potential with appropriate parameter like t_{Si}, t_{ox}, V_{ds} and L (channel length). It has been observed that center potential more potential value than surface potential and reduces short channel effects. It is provided low leakage current decline DIBL and improve the substhreshold voltage with different silicon thickness and different channel length. The developed model may further be useful to low power devices.

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