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Reconfigured SDR for Wireless Communication with Reduced Power Consumption and High Throughput

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Abstract: ***This paper proposes a comprehensive analysis and implementation of FPGA architecture for low routing power and clock gated CLBs. As the FPGA has thousands of logic blocks and hard embedded micros spread across the chip, more numbers of routing lines and switch boxes are required. Also the clock network is built with same routing resources. The Configurable logic blocks with clock gating will allow reducing the dynamic power. The logical equivalence of CLB inputs will help to reduce the routing congestion and also to improve the timing of the design. The logic operations are in conventional carry select adder (CSLA) and binary to excess 1 converter (BEC) based CSLA to study the data dependency and to identify superfluous logic operations. The new logic formulations have been proposed by eliminating all the redundant logic operations present in the conventional CSLA. In the proposed scheme, the carry-select operation is scheduled before calculation of the final-sum. The proposed CSLA design requires significantly less area and delay than the proposed BEC-based CSLA. Due to small carry-output delay, the proposed CSLA design is good for square root (SQRT) CSLA. As per the theoretical figuring, the proposed SQRT CSLA involves nearly 35% less area lag product than the BEC based SQRT CSLA, which is the best amongst the current SQRT CSLA designs. FPGA synthesis result shows that, the BEC-based SQRT CSLA design invokes large Area-Delay Product and consumes more energy than the proposed SQRT CLSA on average for different bit widths.***

Keywords: FPGA, VTR, clock gating, CLB

I. INTRODUCTION

Traditional radio communication systems are implemented using hardware and hence it is difficult to configure the system as per the demands of the customers. This would increase the cost of the system and also the complexity of the system when it is reconfigured to meet the demands of the customers. The Software Defined Radio (SDR) overcomes the limitations of the traditional system by implementing the hardware components by means of software on a computing system such as personal computer or embedded system.

SDR is a radio which provides software defined performances over physical layer. Conventional hardware based radio equipment's depends on hardware thus they are costly and they have limited process as they were not promoting various standard on a single hardware device, whereas SDR is basically software based it provides all functionality with software instead of needed additional circuitry for different actions. According to application we need to modify the software and this makes the SDR compatible with each application on a single hardware. Every time when basic changes we need to change software only and the hardware become appropriate with the new technology, thus for prolong customer it is low cost [1]

Field Programmable Gate Array (FPGA) is the most popular reconfigurable computing technology, ideal for various applications. FPGAs are becoming viable targets for the implementation of reconfigurable designs due to their cost, adaptability, faster time to market etc. FPGAs generally consist of a system with configurable logic blocks consist of LUTs, flip-flops and hard embedded blocks like RAM, DSP block, arithmetic blocks like multiplier, placed in the vast array of interconnects. The reconfiguration of FPGA to a particular logic circuit is possible using hardware description languages like VHDL, Verilog and System Verilog. The FPGA architecture allows large variety of logic designs for real time applications. The FPGA architecture needs to be modified for higher performance and low power consumption. The power dissipation happens more in the routing and clock networks, designing FPGA such a way that less congestion will occur in the routing. Such experiment of FPGA architecture can be carried out using open source CAD like VTR or QFLOW The understanding of new programmable architectures, and the development of new algorithms required to synthesize designs into FPGAs requires a complex software flow that allows experimentation. In this paper we describe the modified FPGA architecture which has impact on power.

The general structure of FPGA provides very high logical capacity and offers more narrow logic resources. A FPGA is a Field Programmable Device featuring a general architecture that grants very high logic quantity. They also provide better ratio of flip-flops to logic resources compared to CPLDs which feature logic resources with a large number of inputs. FPGAs also offer a greater ratio of flip-flops to logic resources than do CPLDs. The paper is organized as follows. Section 2 deals with design requirements and implementation. Section 3 gives an overview of results and discussions and the paper is concluded in section 4.

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II. DESIGN REQUIREMENTS AND IMPLEMENTATION

A. FPGA Architectural challenges

Over the past decade, FPGAs are one of the most promising devices for the implementation of digital circuits. The architecture is designed such that it improves their programmable logic functionalities and programmable interconnect. The architecture of FPGA plays an important role on the quality, speed and power consumption of the final prototype which would account for the usability of the end application. The Logic block architecture, routing architecture and I/O architecture & capabilities are the few challenging areas of FPGA [1].

B. Verilog to Routing (VTR)

The VTR is an open source FPGA CAD mechanism which provides a complete, open-source framework for the implementation of FPGA architecture and CAD research and development [2]. The software flow of the tool takes a Verilog hardware description of digital circuits and description of the target FPGA architecture as inputs and then performs the first operation. i.e. elaboration and synthesis. Then it performs logic optimization and technology mapping. Later the packing, placement, routing and timing analysis are done. One of the challenging tasks is to study the advance FPGA architectures and algorithms due to the need for conducting quality experiments. A quality experiment on FPGA requires a good benchmark design, advanced architecture and CAD tools that are capable of mapping the designs to the architectures [3]. The VTR enables such experiments by providing a new FPGA architectural language with a flexible and robust CAD flow [4].

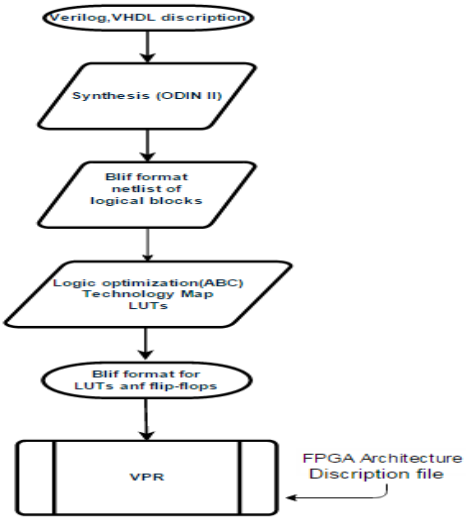

Fig. 1. VPR Flow

C. *LUT Architecture with fully populated crossbar*

The CLB architecture has many LUTs inside it which has inputs corresponding to each LUT. These input connections made configurable to the LUTs. The below figure shows the overall CLB architecture with LUTs [5].

FPGA are the most promising devices for the modern digital design. The architecture plays crucial role in the reprogrammable devices. It impacts the timing, Speed and power performance of the design. Hardcoded clock gating helps to improve the dynamic clock power consumption. The 4-LUT is the best option for the FPGAs due its less power and area consumption with good efficiency to implement digital design with large number of variables. The IO pin configuration can also be made logically equivalence to reduce the routing congestion. Also the heterogeneous routing wire architecture, pipe lined architecture and LUTs input/output pin rearrangement techniques can be used to improve the FPGA performance [2].

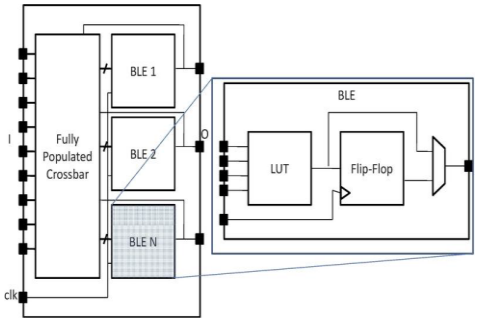

Fig. 2. LUT with populated crossbar

The internal structure of the crossbar is as shown in below diagram.

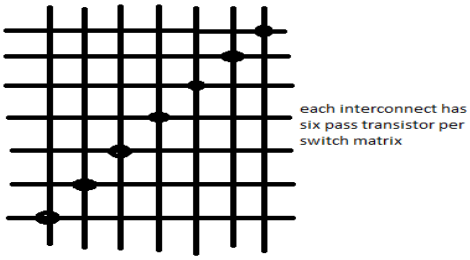

Fig. 3. Populated cross bar structure

The advantage of the programmable interconnection between LUT and inputs is the routing congestion gets reduced. The configurable LUT inputs reduce the long paths being routed. This is implemented in VPR using FPGA architectural language. We need to apply logical equivalence to the inputs and outputs so that tool will understand that connects to those pins can be interchanged and changing its functionality.

D. Clock gating to CLBs

The clock network power consumption is around 30% in the FPGA total dynamic power consumption. As the clock pin in CLBs could not make as logical equivalence, the best way to put hardcoded clock gating options so that clock power consumption can be reduced. The following diagram shows the clock gating LUTs [5].

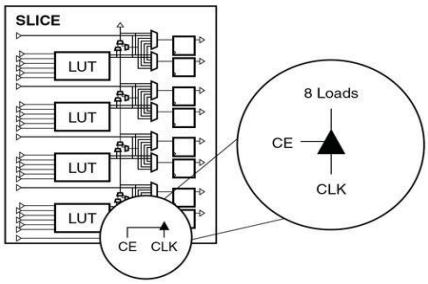

Fig. 4. LUT clock gating buffer

The clock enable signal produced is allowed changing in the non-active part of the clock. This can be achieved by introducing latch having opposite sense of the clock edge. The flowing diagram shows the clock gating.

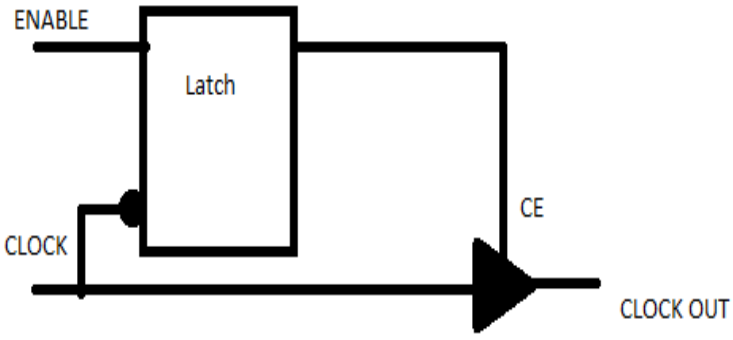

Fig. 5. Glitch free Clock gating

This clock gating with LUT is implemented in the VPR which is described in the following architectural language [5].

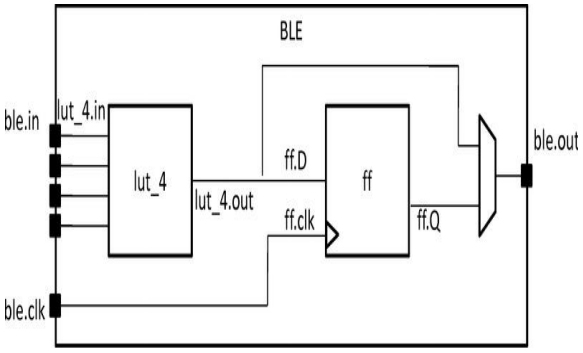

Fig. 6. Four input LUT

```
<pb_type name="ff" blif_model=".clockgate>
<interconnect>
 <direct input=“clk" output=“latch.D"/>
<direct input=“clk" output=“buff_in"/>
<direct input=“enable" output=“latch.D"/>
 <direct input=“latch.Q" output=“buff_CE"/>
 <direct input=“clock_out" output=“ble.clk"/>
<direct input="lut_4.out" output="ff.D"/>
<direct input="ble.in" output="lut_4.in"/>
<mux input="ff.Q lut_4.out" output="ble.out"/>
<direct input="ble.clk" output="ff.clk"/>
</interconnect>
</pb_type>
```

E. LUT Architecture for efficiency and performance

A bigger LUTs can be implemented from smaller LUTs and one or more multiplexers. Similarly a 5-LUT can be built from two 4-LUTs and a multiplexer, while a 6-LUT can be built with two 5-LUTs and a multiplexer. The problem with the smaller LUT architecture is that logic circuit built from it are inefficient and result in unused resources when implementing smaller functions. There is another important issue is the replication of routing to the smaller LUTs when building a larger LUT and the creation of extra delays between LUTs which results in a non-optimized logic structure [6].

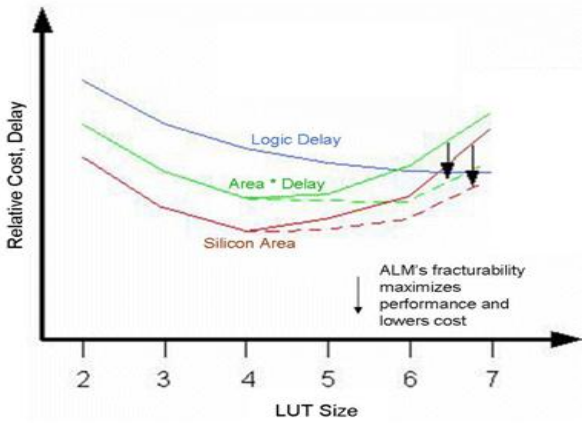

Fig. 7. Cost-logic delay tradeoff with varying LUT sizes

The above graph shows the delay and area of the LUTs with different sizes and as shown in above figure the minimum area is for 4 LUT architecture and as 5-LUt and 6-LUT can be implemented using 4-LUT area wise and routing wise it is efficient to use 4-LUt for FPGA architecture.

F. Timing Driven Routing and Placement

VPR supports the placement and routing of the design driven by the timing. The constraints are written in the standard SDC format.

```
create_clock -period 3 -waveform {1.25 2.75} clk create_clock -period 2 clk2
create_clock -period 1 -name input_clk
create_clock -period 0 -name output_clk set_clock_groups -exclusive -group input_clk -group clk2
set_output_delay -clock output_clk -max 1[get_ports {out*}]
```

III. RESULTS AND DISCUSSIONS

The routing power of the design reduced due to populated cross bar FPGA CLB architecture. Also the hardcoded clock gating helps to reduce the clock network dynamic power consumption and 4-LUT architecture is more efficient with respect to area and delay. The timing of overall design was improved.

Table-I: Device 3s500efg320-4 Utilization

No of CLBs	FPGA Architecture without Clock Gating and populated Crossbar	FPGA Architecture with Clock Gating and populated Crossbar	Timing
4930	58.77%	56.43%	322.32MHz
4342	33.48%	27.22%	345.72MHz

The routing power of the design reduced due to populated cross bar FPGA CLB architecture. Also the hardcoded clock gating helps to reduce the clock network dynamic power consumption and 4-LUT architecture is more efficient with respect to area and delay. The timing of overall design was improved.

IV. CONCLUSION

FPGA are the most promising devices for the modern digital design. The architecture plays crucial role in the reprogrammable devices. It impacts the timing, Speed and power performance of the design. Hardcoded clock gating helps to improve the dynamic clock power consumption. The 4-LUT is the best option for the FPGAs due its less power and area consumption with good efficiency to implement digital design with large number of variables. The I/O pin configuration can also be made logically equivalence to reduce the routing congestion. Also the heterogeneous routing wire architecture, pipe lined architecture and LUTs input/output pin rearrangement techniques can be used to improve the FPGA performance.

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