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Performance Analysis of ALU design using Irreversible and Reversible gates

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Abstract

Now-a-days, the VLSI industry is tilting towards the application of reversible logic in the designing. Certain constraints like quantum cost, power dissipation and efficiency in producing the outputs mandates to employ the reversible logic gates over the irreversible logic gates.By deploying the logic which can be reversed , the generation of flaw outputs causing loss of information bits are eliminated. In this paper, we design an ALU holding restoring output logic gates and compare it with an ALU employed irrevocable logic gates. COG gate and HNG gate are the restoring logic gates mooted in developing the proposed design. The factors like average power, quantum cost are analyzed in this paper.

Keywords: *ALU, reversible logic, COG gate, HNG gate)*

1 Introduction:

In the recent days, the major concerns in VLSI chip designing are about size, power dissipation which may hinder the performance of the circuit. This makes the application of reversible logic technology mandatory because of its significance over conventional logic gates. The irreversible logic gates do not adhere to the constraints like size, power dissipation etc. Reversible logic plays a vital role in quantum computing and its implementation in nano technology scale. Also, many researches have made efforts towards the reduction of the power dissipation in many circuits. There are great losses associated with power dissipation and it has been proven that reversible logic has been one of the solutions.

In irreversible logic gates the input vector quantity is not equal to the output vector quantity. It may lead to the production of garbage outputs. These garbage outputs may in turn lead to the power dissipation in the circuits. This drawback of irreversible gates makes the use the logic gates which can be restored is mandatory. Here the output vector quantity has the same value as the input vector quantity. This helps in mapping the inputs and outputs in a one-to-one manner. In this way, it is also helpful in tracing the inputs with the outputs and re-utilizing them for the further stages. Above all quantum cost can be decreased with the reversible logic gates. Reversible logic has applications in computer security and transaction processing.

These advancements in reversible logic and its wide spread applications in designing, paves the way for designing an ALU. The ALU which in turn has many applications in performing complex operations and in multi-precision arithmetic algorithms also.

2 Reversible gates:

The reversible gates used are the COG and HNG gates. COG stands for Controlled Operation Gate. COG

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symbol is illustrated in diagram 1 and in Table 1 ,the truth table is depicted.

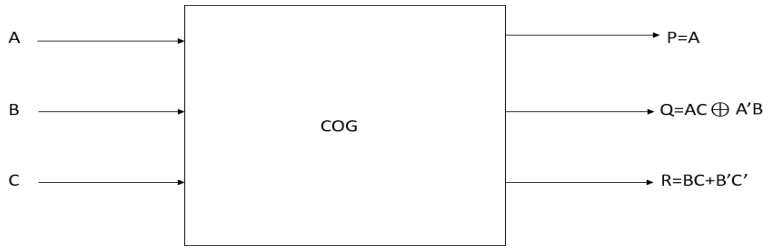

Figure 1: Restoring reversible (COG) gate

Chart 1: Restoring logic COG gate

Input A	Input B	Input C	Output P	Output Q	Output R
1	1	1	1	1	1
1	1	0	1	0	0
1	0	1	1	0	1
1	0	0	1	1	0
0	1	1	0	1	1
0	1	0	0	0	1
0	0	1	0	0	0
0	0	0	0	1	0

The HNG gate used produces outputs sum and carry. Diagram 2 represents the HNG gate symbol.

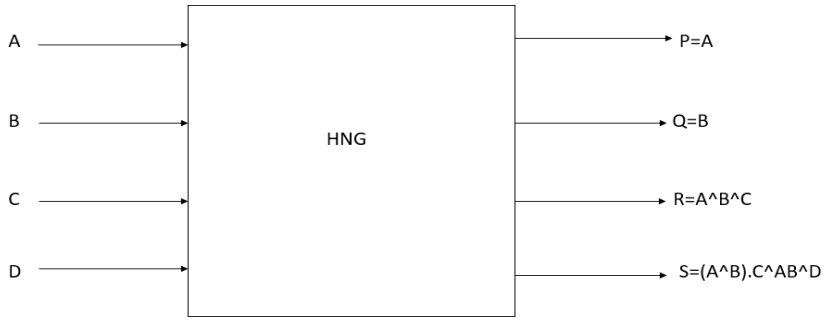

Diagram 2: HNG reversible circuit structure

These are the gates used in construction of ALU using reversible gates.

3 Operation of irreversible ALU:

Using these irreversible gates, ALU is constructed. This ALU carries out 8 operations. Those operations are namely addition, subtraction, Increment A, Decrement A, OR, NOR, XOR, XNOR. These operations

are implemented as circuits using logic gates and then their results are connected to the multiplexer. The multiplexer used here is an 8:1 multiplexer. Based on the selection lines and the respective sequence of operations performed the ALU is implemented. The block diagram of the ALU using irreversible gates is shown below as Figure 3. The circuit is implemented using Cadence Virtuoso tool as shown in the Figure 4.

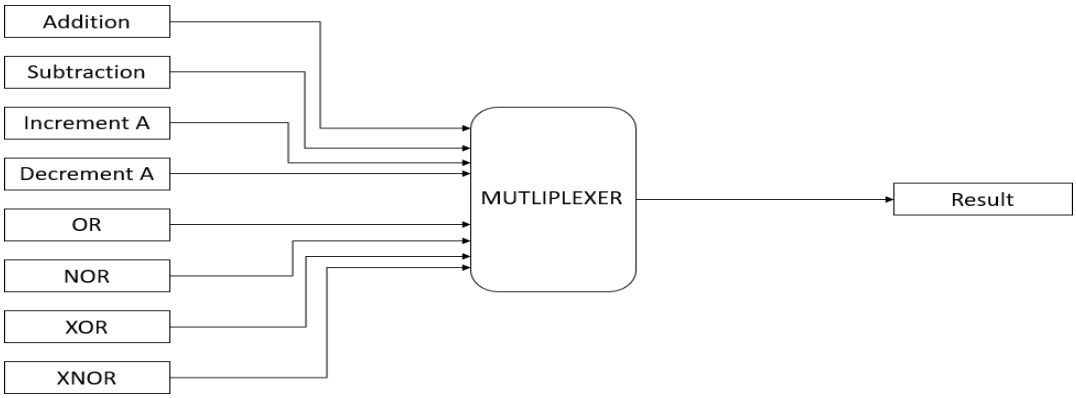

Figure 3: Block Diagram of ALU using irreversible gates

The circuit is implemented using Cadence Virtuoso tool as shown in the Figure 4.

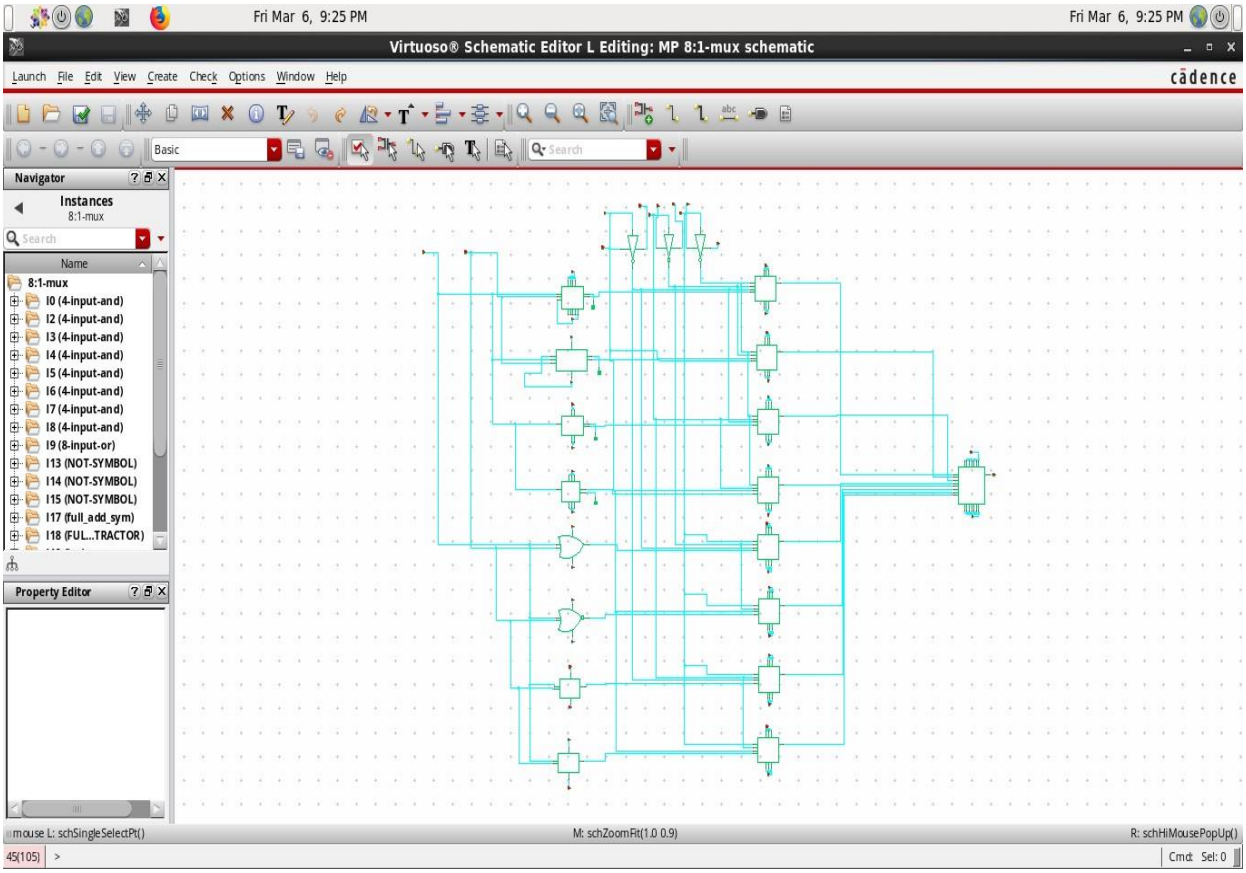

Figure 4: Schematic of ALU using irreversible gates

4 Operation of reversible ALU:

Restoring structure gates employed for implementation of ALU here are gates like COG and HNG gates. The usage of these gates helps reduce power consumption and the number of transistors. Illustration 5 represents the control circuitry . It consists of COG gates.

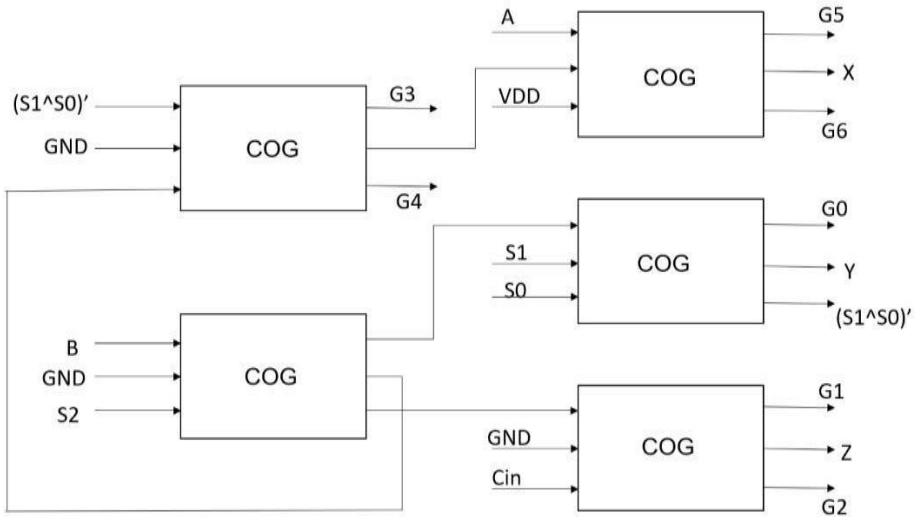

Figure 5: Block diagram of Electronic Control circuitry

Illustration 6 represents represents ALU .

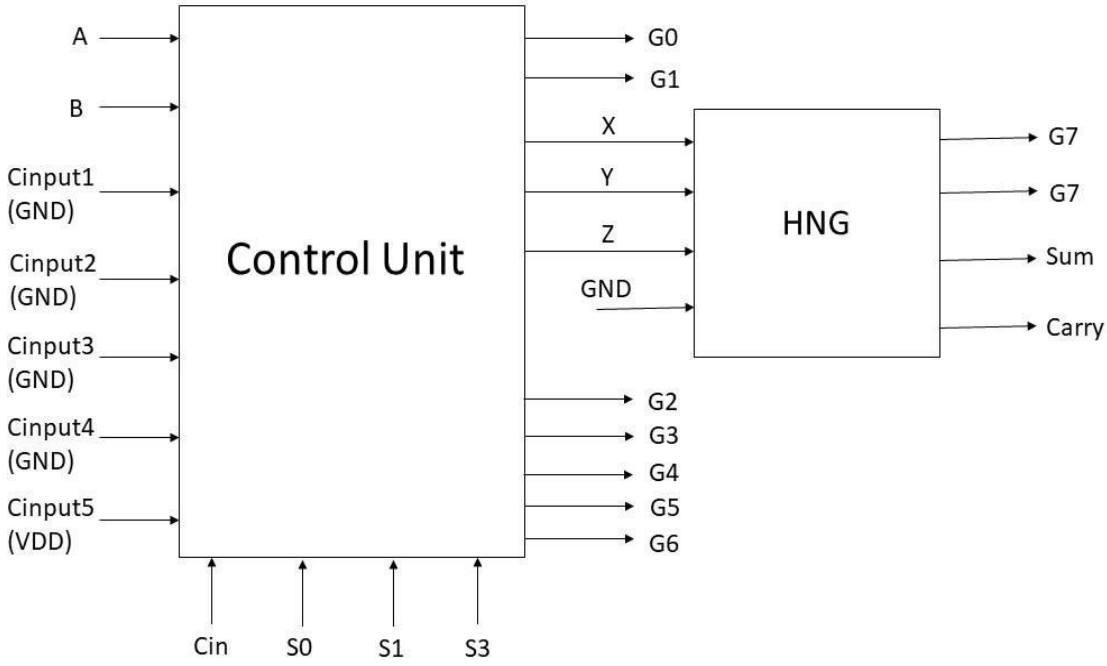

Figure 6: Block diagram of reversible Arithmetic and logical structure

Chart 2 represents (reversible) restoring arithmetic and logical structure

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Table 2 : Function Table of reversible ALU

S1	S2	S3	Cin	function
0	0	0	1	Increment A
0	0	1	0	Addition
0	1	0	1	Subtraction
0	1	1	0	Decrement
1	0	0	0	OR
1	0	1	0	XOR
1	1	0	0	Exnor function
1	1	1	0	NOR

The schematic of the circuit implemented in the cadence tool is shown in the Figure 7.

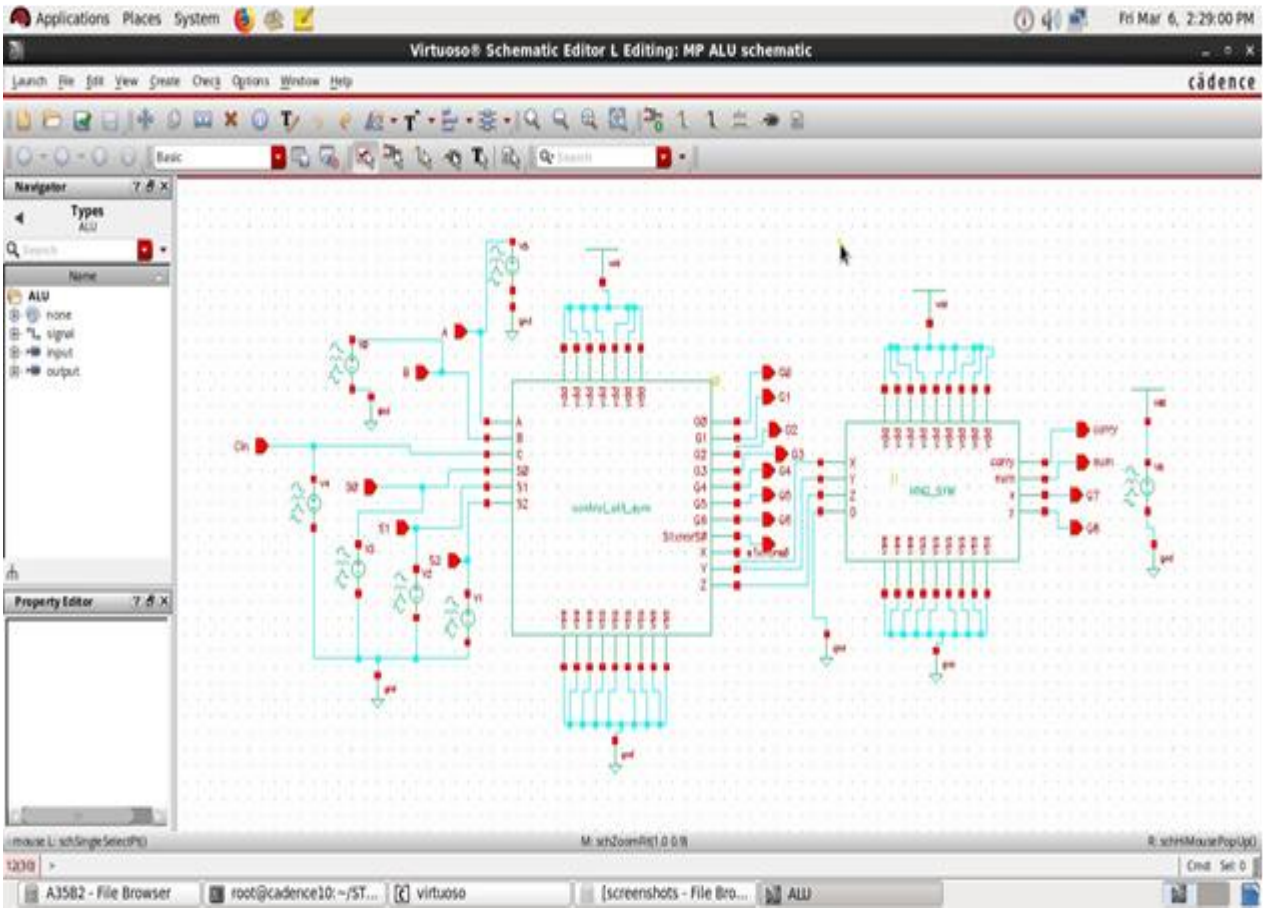

Figure 7 : Schematic of reversible ALU

5 Results and Discussions:

ALU using irreversible gates and reversible gates are both implemented in the cadence virtuoso tool. The number of transistors required for the construction of ALU using irreversible gates is 420 but it is 332 in

the case of construction of ALU using reversible gates. The average power required for both the circuits is calculated using the tool and is obtained to be 460.2E-6W in case of reversible ALU and 1.646E-3W.

Chart 3: ALU examination using irreversible gates and reversible ALU

Parameter	Irreversible structure ALU	reversible structure ALU
Number of transistors	420	332
Average Power in Watts	1.646E-3	460.2E-6

6 Conclusion:

ALU is the basic circuit that is used in many digital circuits where there is a need of computation. ALU is a major part that carries out various operations according to the user requirement. Thus, the power required for its operation plays a vital role in a circuit's overall operation. Implementation of reversible circuit ALU reduces transistor quantity with the power requirement which are major boundary when analyzing the performance of the circuit. This paper proves the same with circuits implemented using cadence virtuoso tool.

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