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Design And Simulation of Different Comparators Using Cadence Virtuoso Analog Design- A Comparative Study

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Abstract

Comparator is the main building block of any analog-to–digital converter. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison In this paper we have designed the comparators using process parameter in gpdk_180 and UMC_180 technology and compared the simulated results of the open loop high gain comparator, composite comparator, preamplifier, latch and output buffer based comparators. the results of AC, DC, and transient analysis have been performed for gain, slew rate, offset DC power etc. All three high gain comparators are designed and simulated in Cadence Virtuoso Analog Design Environment.
Keywords*: Comparator, Gain, Amplifier.*

Introduction

Today, where demand for portable battery operated devices is increasing, a major effort is made towards low power methodologies for high resolution and high speed applications. This reduction in power can be achieved by moving towards smaller feature size processes. However, as we move towards smaller feature size processes, the process variations and other non-idealities will greatly affect the overall performance of the device in question. [1-7] one such application where low power, high resolution and high speed are required is Analog-to-Digital Converters (ADCs) for mobile and portable devices [8-9]. Analog-to-Digital Converters are effectively used in modern era. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. For n-bit flash ADC, (2^n-1) comparators are needed. So low power consumption in comparators is required for design of low power ADC.[10-13] The other application of comparator is as Null detectors. A Null detector is a circuit that functions to identify zero input. When using a comparator as a null detector, there are limits as to the accuracy of the zero value. Comparators are also used in the front-end of a radio-frequency receiver in most of the modern telecommunication systems, sense amplifiers (SAs) in memories and data receivers [14-15].

Literature Review

For high resolution high speed analog-to-digital applications, low offset dynamic comparator was proposed [2] these are favorable for flash and pipeline data conversion applications. Comparator structure was designed [4] to increase accuracy, reduce power dissipation and increase the speed of an ADC. A novel dynamic latched comparator [7] demonstrates higher load drivability and lower offset voltage. An improved design of two stage Op-Amp based CMOS Comparator[10] having ultra low power consumption, a high precision circuit with low power[11] capable of distinguishing DC voltage difference of around 5mV, preamplifier using negative resistance as a load and a double regenerative dynamic latch

[12], CMOS comparator of high gain with slew rate of 10v/μs [13], to enhance latch regeneration speed novel comparator based on double-tail architecture [14], a novel low power comparator capable of resolving 1mV voltage difference between its input nodes [15],conventional architecture of common-mode current feedback with the modified gain booster topology to achieve high slew rate and boosted gain[16], Strong Arm comparator was compared with the double tail topology[17],dynamic-latch-based comparator to achieve area-efficient realization at lower power dissipation [18] was proposed by researchers to analyze the performance of different comparators.

Circuit Design

In this section we have demonstrated the circuit design of three high gain comparators that are open loop high gain comparator, composite comparator, preamplifier latch and output buffer based comparators. All three high gain comparators are designed in Cadence Virtuoso Analog Design Environment. Table 1.1 and 1.2 shows the values of process parameter in gpdk_180 and UMC_180 technology. The symbol $|V_t|$ represent the threshold voltage in case of NMOS and PMOS, μ represents the mobility of electron in case of NMOS and hole in case of PMOS and t_{ox} is the oxide thickness.

Table 1.1 Process Parameter for gpgk_180 nm technology

Process Parameters	NMOS	PMOS
$\|V_t\|$(volt)	.48	.46
μ (cm^2 /V-S)	300	110
tox (Å)	40	40

Table 1.2 Process Parameter for UMC_180nm technology

Process Parameters	NMOS	PMOS
$\|V_t\|$(volt)	0.32	0.45
μ (cm^2 /V-S)	314.1	114.5
tox (Å)	42	42

Open Loop High Gain Comparator Schematic Design

The design dimensions of open loop high gain comparator are shown in Table 1.3 for the schematic corresponding to Fig 1.1. The calculated values (second column of Table 1.3) of (W/L) are used in the circuit first. They are optimized to new values. The circuit is simulated corresponding to optimized values. The simulated design dimensions are shown in third column of Table 1.3.

Table 1.3 Design dimensions of open loop comparator

Dimensions	Calculated values	Simulated values
$(W/L)_{NM6,7}$	2.8u/180n	500n/.18u
(W/L)PM1,0	.72u/180n	500n/.18u
$(W/L)_{PM2}$	8u/180n	15u/.18u

$(W/L)_{NM3}$	3u/180n	4u/.18u
$(W/L)_{NM4}$	2u/.36u	720n/.36u
$(W/L)_{NM0}$	2u/.36u	900n/.36u

The schematic of an open loop stage high gain comparator is drawn using cadence schematic editor as shown in Fig 1.1. One more stage is cascaded at the output to drive the output capacitance and to increase gain. A gain of grater then 80 dB achieved with a UGB in the range of GHz. The supply voltage is taken as 1.8V. The value of DC current source is 18µA. The value of load capacitance is 3pf. All the MOS transistors are operated in saturation.

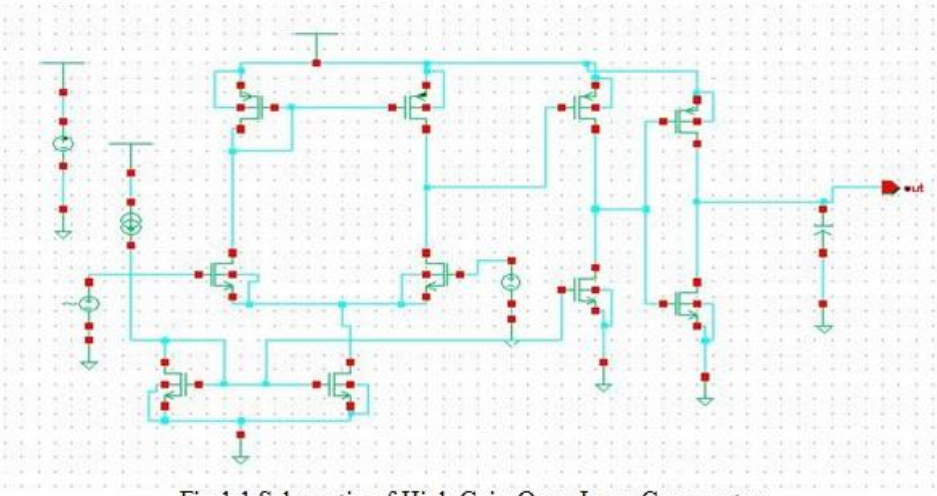

Fig 1.1 Schematic of High Gain Open Loop Comparator

Composite Comparator Schematic Design

The design dimensions of composite comparator are shown in table 1.4 for the schematic corresponding to fig 1.2. The dimension (W/L) is calculated by design equation. The calculated values (second column of table 1.4) of (W/L) are used in the circuit first. They are optimized to new values. The circuit is simulated corresponding to optimized values. The simulated design dimensions are shown in third column of Table 1.4.

Table 1.4 Design Dimension of Composite Comparator

Dimension	**Calculated values**	**Simulated values**
$(W/L)_{1,7\ MN}$	5µ/180nm	8µ /180n
$(W/L)_{0,8\ MN}$	5µ/180nm	8µ /180n
$(W/L)_{2,0\ PN}$	1µ /180nm	500n /180nm
(W/L)1,3 PN	1µ /180nm	500n /180nm
$(W/L)_{11\ MN}$	900n/180nm	500n/180nm
$(W/L)_{4PM}$	10µ /180nm	30µ /180nm
$(W/L)_{4NM}$	3µ/180nm	800/180nm

The schematic of a two stage composite comparator is shown in Fig 1.2. It is drawn using cadence schematic editor and simulated using cadence spectre simulator in gpdk_180nm technology. A gain of greater than 80dB is achieved. The supply voltage is taken as 1.8 V and the load capacitance is 2pf.

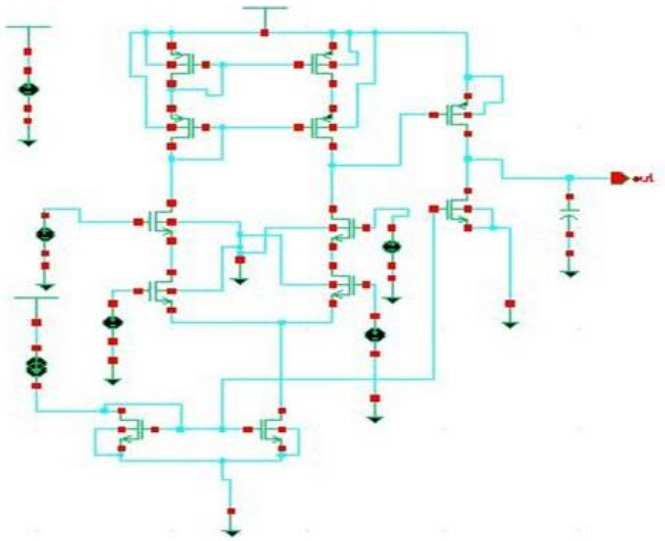

Fig 1.2 Schematic of Composite Comparator

Preamplifier Latch and Output Buffer Based Comparator Schematic

The schematic of Preamplifier latch and output buffer based comparator is shown in Fig 1.3. It is drawn using cadence schematic editor and simulated using cadence spectre simulator. A gain of greater than 80dB is achieved. The supply voltage is taken as 1.8 V and the load capacitance is 3pf.

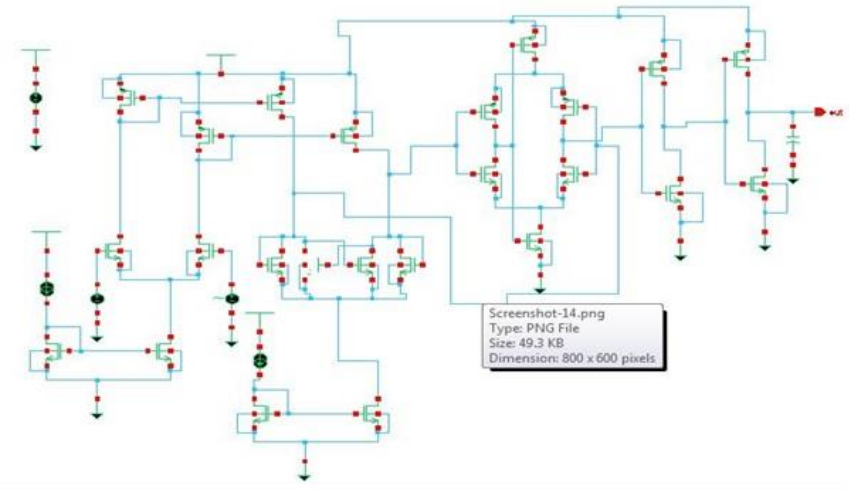

Fig 1.3 Schematic of Preamplifier Latch and Output Buffer Based Comparator.

Simulation Results and Discussion

In the previous section, design of open loop comparator, composite comparator and preamplifier, latch and output buffer based comparator were discussed. This section presents the simulation results of the open loop high gain comparator, composite comparator, preamplifier, latch and output buffer based

comparators and the results of AC, DC, and transient analysis been performed for gain, slew rate, offset DC power etc. All three high gain comparators are simulated in Cadence Virtuoso Analog Design Environment.

Simulation of Open Loop High Gain Comparator

AC Analysis Fig 1.4 shows the AC analysis for the schematic of Fig 1.1 including input and output voltages. Using this AC analysis, the open loop comparator gain is obtained and its value is found to be 81.46db as shown below in Fig. 1.4

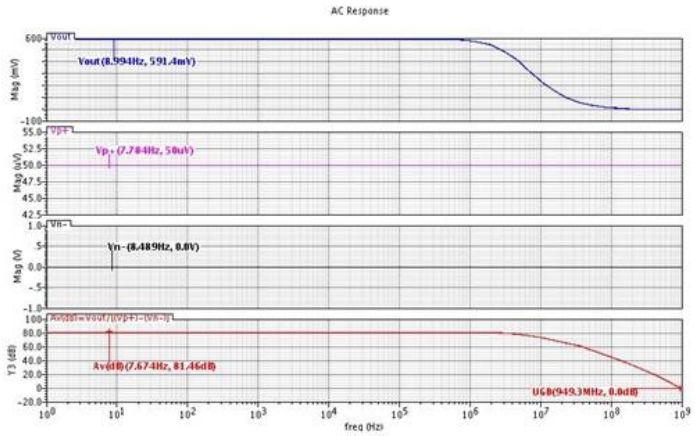

Fig.1.4 AC Plot of Open Loop Comparator.

Transient Analysis

Fig 1.5 shows the transient analysis of the circuit shown in Fig 1.1. For this analysis of a comparator an AC source of 0.5mv AC amplitude with 10 MHz frequency is applied to one input V_{P+}, and V_{n-}(reference) set to 0.7V and simulated by cadence spectre simulator. The output waveform of comparator is shown below.

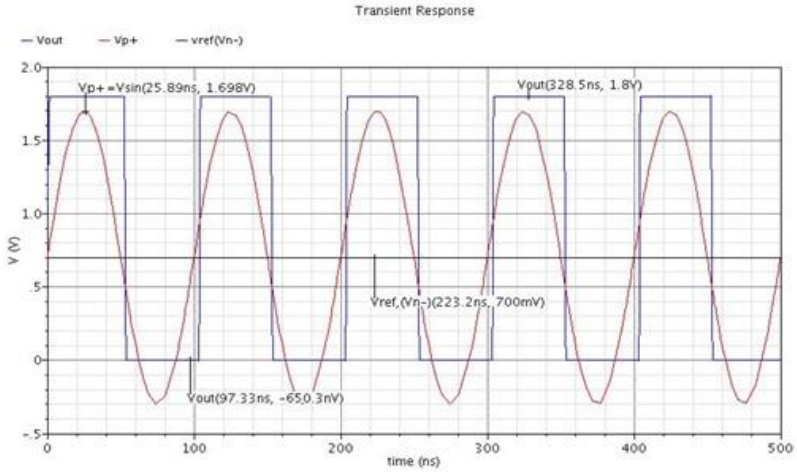

Fig 1.5 Transient Plot of Open Loop Comparator.

Rise Time

Rise time is defined as the time taken by output waveform to reach from 10 % to 90% of the final value. As shown in Fig 1.6 a zoomed part of output waveform is use to find out the rise time. By selecting the transition part of waveform, the rise time is calculated directly from the calculator used in cadence, analog design environment. The rise time is found to be 0.65 ns.

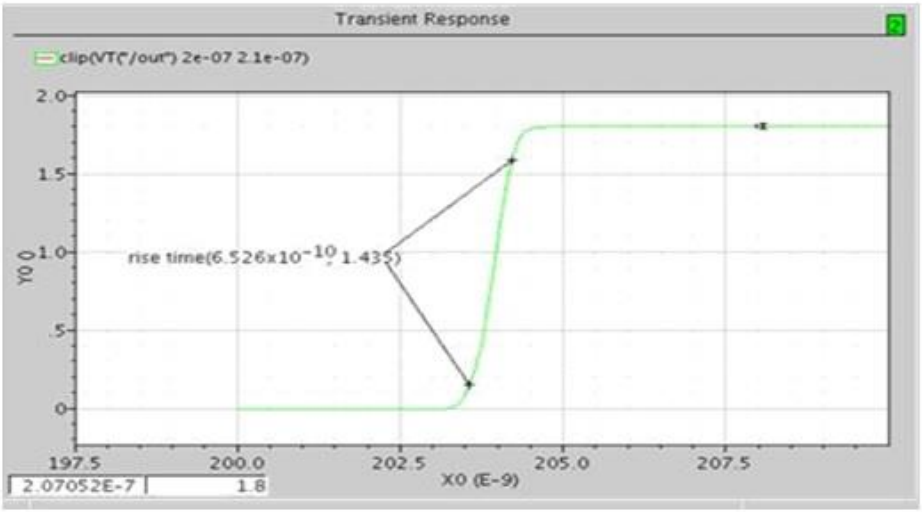

Fig 1.6 Transient Plot for Rise Time of Open Loop Comparator

Slew Rate

Transient analysis (Fig 1.5) is used to find out the slew rate. As shown in Fig 1.7 the red line waveform is the transition part of output waveform and blue line is the derivative of output waveform. The maximum value of the derivative of output waveform gives the positive slew rate. The value of positive slew rate is 2.85V/nsec.

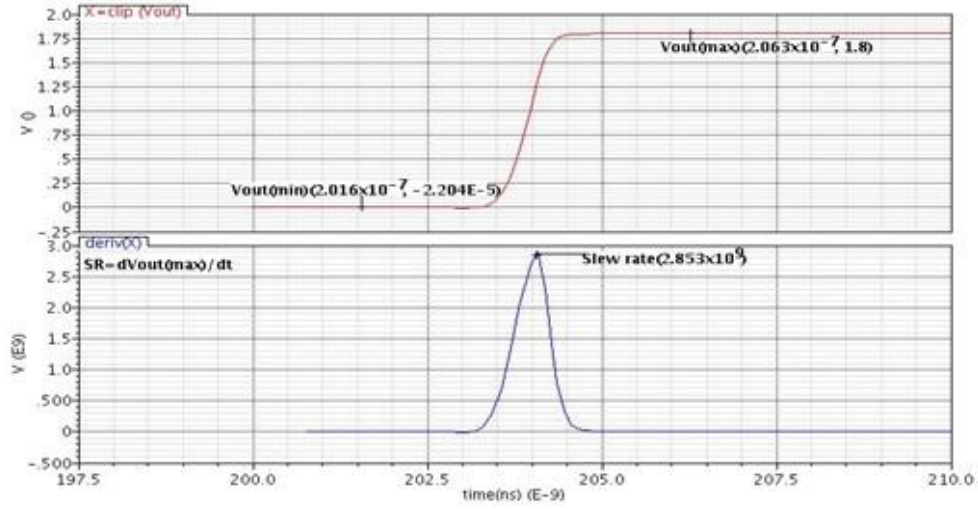

Fig 1.7 Positive Slew Rate Plot for Open Loop Comparator

The negative slew rate is shown in the Fig 1.8. The negative slew rate is equal to -1.9V/nsec. As shown in Fig 1.8 the red line is an output waveform and blue line waveform is the derivative of output waveform. The minimum value of blue line waveform gives the negative slew rate.

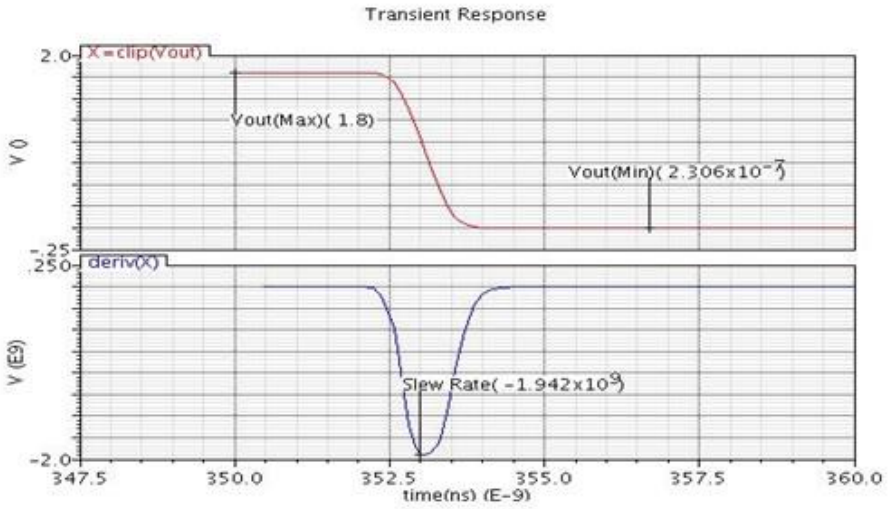

Fig 1.8 Negative Slew Rate Plot of Open Loop Comparator

For performing DC analysis, apply the DC voltage source (1.8V) at one input terminal and reference voltage (0.6V) on another terminal. Then the Input voltage is swept from 0V to 1.8V and reference voltage is kept at 0.6 V. Find out Offset by DC analysis. As shown in Fig 1.9, offset is calculated by taking voltage difference between input (swept voltage) and output crosses reference voltage. The voltage offset value is 3.58mV.

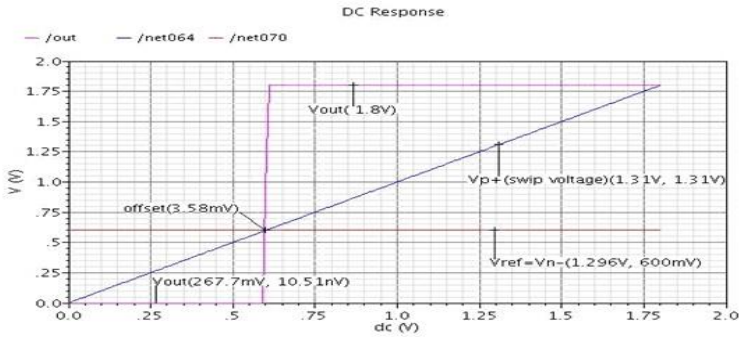

Fig 1.9 DC Response of Open Loop Comparator

Simulation Results of Open Loop Comparator

The schematic of open loop comparator shown in Fig 1.1 is simulated in cadence spectra simulator. The results obtained after simulation are shown in Table 1.5. The gain is achieved 81.44dB.

Table 1.5 Simulated Parameters of Open Loop Comparator

Parameter	Simulation Result
Ao(dB)	81.46

SR(V/nS)	2.85,-1.9
Risetime(ns)	0.65
Offset(mv)	3.58
Power Consumption	71.6128

Simulation of Composite Comparator

AC Analysis

Fig 1.10 shows the AC analysis for the schematic of Fig 1.2 including input and output voltages. By using AC analysis, the composite comparator gain is obtained as 80.63db (shown in below Fig 1.10).

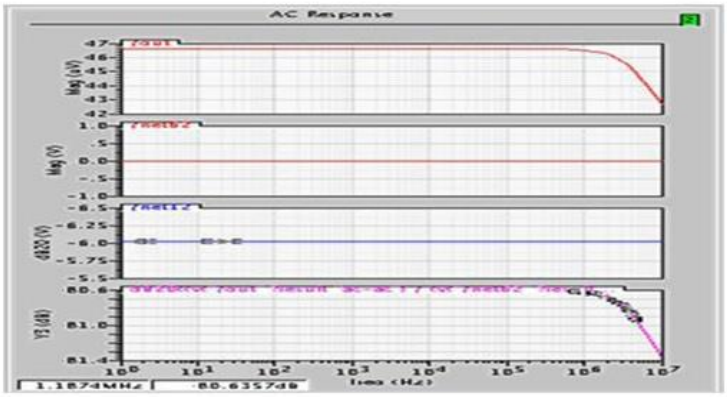

Fig 1.10 AC Plot for Gain of Composite Comparator

Transient Analysis

Fig 1.11 shows the transient analysis of the Schematic of Composite Comparator shown in Fig 1.2. For this analysis of a comparator an AC source of 0.5mV AC amplitude with 10 MHz frequency is applied to one input V_{P+}, and V_{n-}(reference) is set to 0.7V. The circuit is simulated by cadence spectre simulator. The output waveform of comparator is shown below.

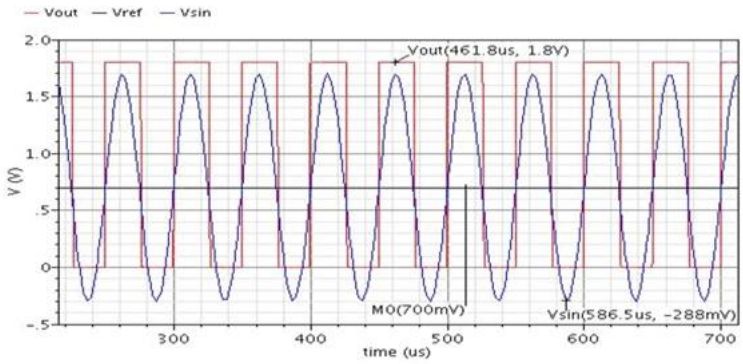

Fig 1.11 Transient Plot of Composite Comparator

Rise Time

Rise time is defined as the time taken by output waveform to reach from 10 % to 90% of the final value. As shown in Fig 1.12, a zoomed part of output waveform is used to find out the rise time. By selecting the

transition part of waveform, the rise time is calculated directly from the calculator used in cadence, analog design environment. The rise time is found to be 143 ns.

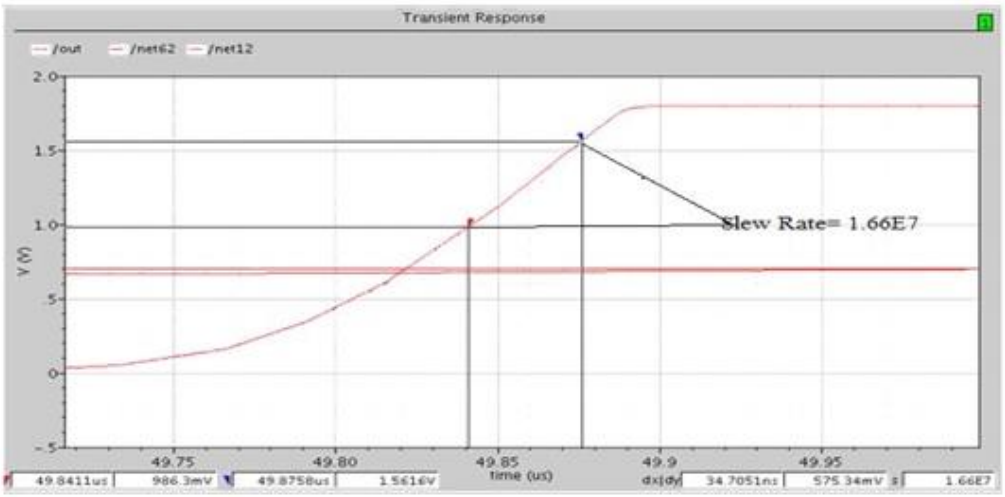

Fig 1.12 Rise Time of Composite Comparator

Slew Rate

For slew rate calculation, transient analysis is performed. A positive slew rate is shown in Fig 1.13. The positive slew rate is shown in the bottom right box of Fig 1.13. "s" represents the slew rate. The positive slew rate is equal to +16V/usec.

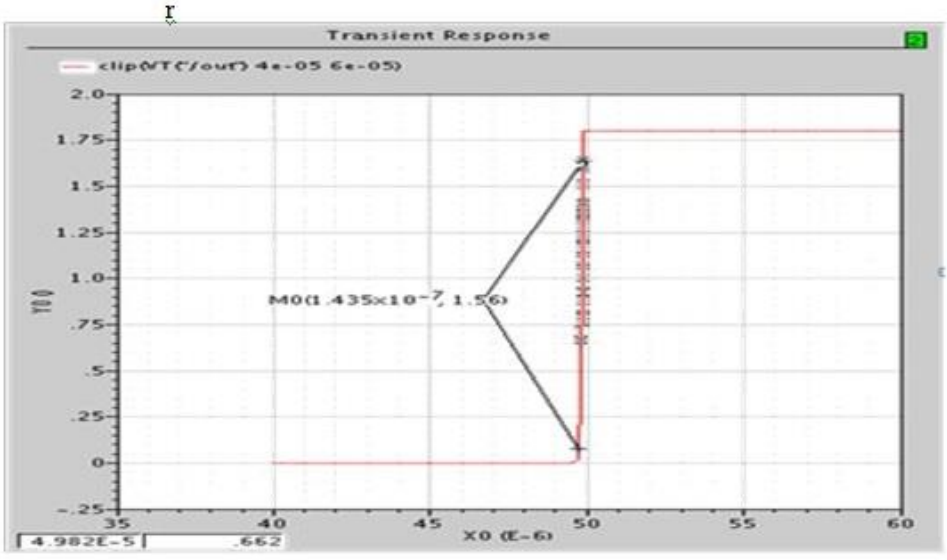

Fig 1.13 Positive Slew Rate Plot of Composite Comparator

DC Analysis

Figure 1.14 shows the DC analysis of composite comparator. For performing DC analysis, the DC voltage source(1.8V) is applied at one input terminal and reference voltage (.7V) on another terminal and then

Input voltage is swept from 0V to 1.8V and reference voltage is taken as .7 V. Offset is found out by DC analysis. As shown in Fig 1.14, offset is calculated by taking the voltage difference between input (swept voltage) and output crosses reference voltage. The voltage offset value is 44.61mV.

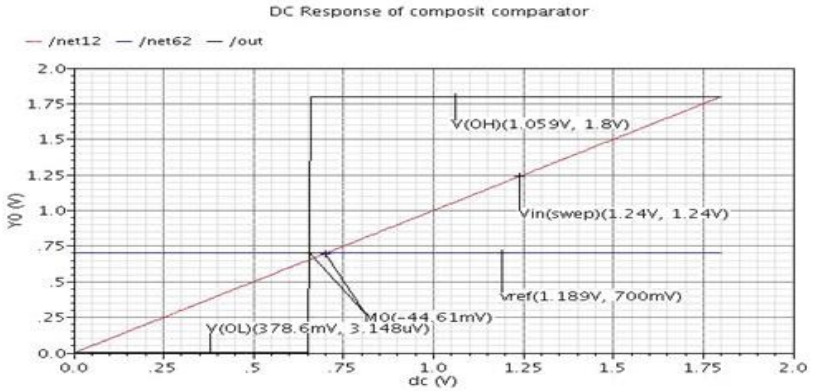

Fig 1.14 DC Plot of Preamplifier Latch Based Comparator

Simulation Result of Composite Comparator

The schematic of composite comparator is shown in Fig 1.2 is simulated in cadence spectra simulator. The results obtained after simulation are shown in table 1.6.

Table 1.6 Simulated Parameters of Composite Comparator

Parameter	Simulation Result
Ao(dB)	80.63
SR(V/μS)	16
Rise time(nS)	143
Offset(mV)	44.49
Power Consumption (μW)	18.135

Simulation of Preamplifier Latch and Output Buffer Based Comparator

AC Analysis

Fig 1.15 shows the AC analysis for the schematic of Fig 1.3. By AC analysis, the comparator gain (blue line) is obtained as 97.61db (shown below in fig 1.15.)

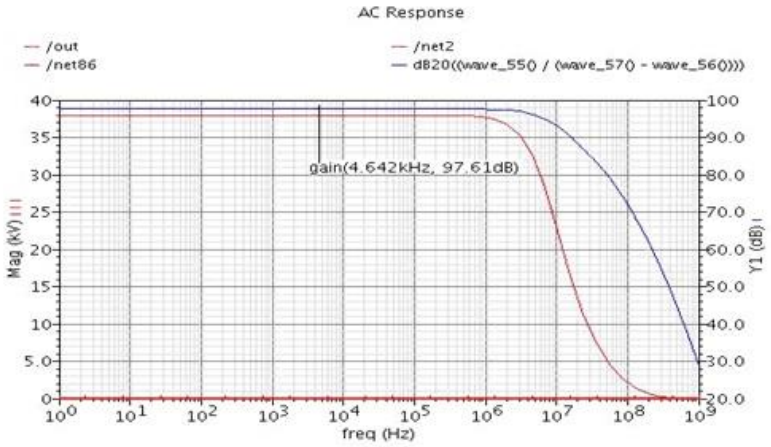

Fig 1.15 AC Plot of Preamplifier Latch Based Comparator

Transient Analysis

Fig 1.16 shows the transient analysis of the preamplifier, latch and output buffer based Comparator Fig 1.3. For this analysis of a comparator an AC source of 0.5mV AC amplitude with 10 MHz frequency is applied to one input V_{P+}, and V_{n-}(reference) set to 0.6V. The circuit is simulated by cadence spectre simulator. The output waveform of comparator is shown below.

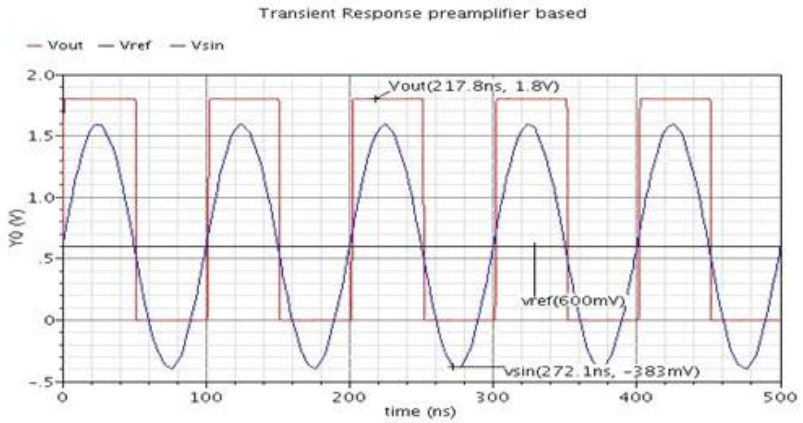

Fig 1.16 Transient Plot of Preamplifier Latch Based Comparator

Rise Time

Rise time is defined as the time taken by output waveform to reach from 10 % to 90% of the final value. As shown in Fig 1.17. a zoomed part of output waveform is use to find out the rise time. By selecting the transition part of waveform, the rise time is calculated directly from the calculator used in cadence, analog design environment. The rise time is found to be 0.54 ns.

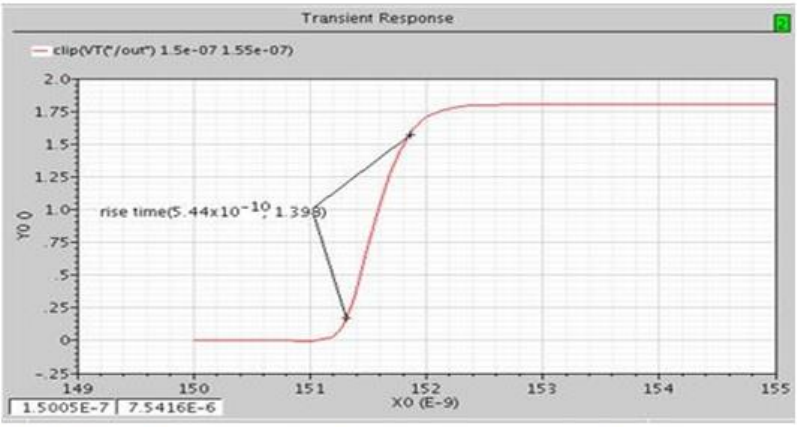

Fig 1.17 Rise Time of Preamplifier Latch and Output Buffer Based Comparator

Slew Rate

Transient analysis (fig 1.16) is used to find out the slew rate. As shown in fig 1.18, the red line waveform is the transition part of output waveform and blue line is the derivative of output waveform. The maximum value of the derivative of output waveform gives the positive slew rate. The value of positive slew rate is 3.3V/nsec.

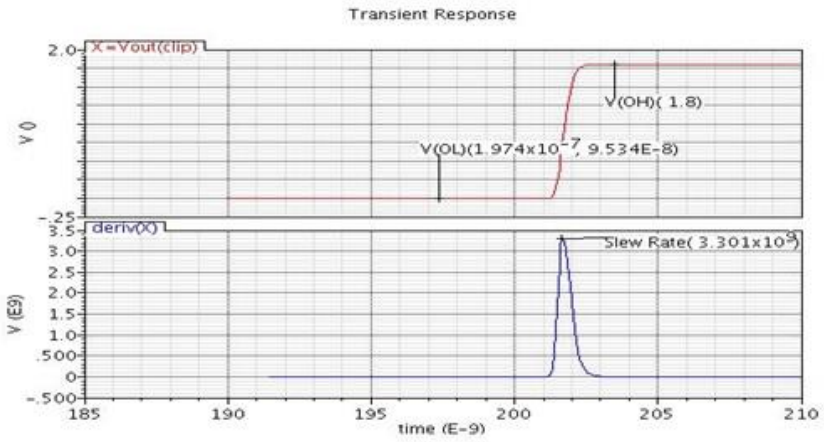

Fig 1.18 Positive Slew Rate Plot of Preamplifier Latch Based Comparator

The negative slew rate is shown in the fig 1.19. The negative slew rate is equal to - 7.57V/nsec. As shown in fig 1.19 the red line is an output waveform and blue line waveform is the derivative of output waveform. The minimum value of blue line waveform gives the negative slew rate.

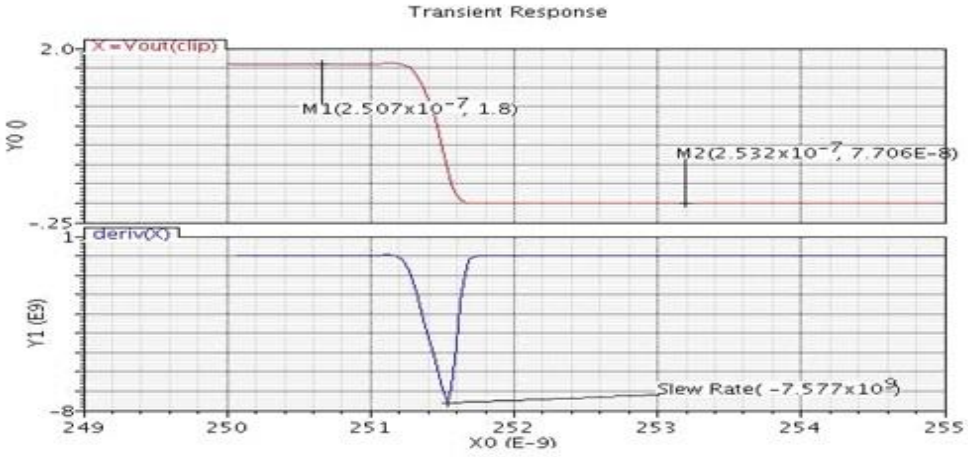

Fig 1.19 Negative Slew Rate Plot of Preamplifier Latch Based Comparator

DC Analysis

Figure 1.20 shows the DC analysis of composite comparator. For performing DC analysis, the DC voltage source(1.8V) is applied at one input terminal and reference voltage (0.6V) is applied on another terminal and then Input voltage is swept from 0V to 1.8V and reference voltage is taken as 0.6 V. Offset is find out by using DC analysis. As shown in Fig 1.20, offset is calculated by taking the voltage difference between input (swept voltage) and output crosses reference voltage. The voltage offset value is 633.8 V.

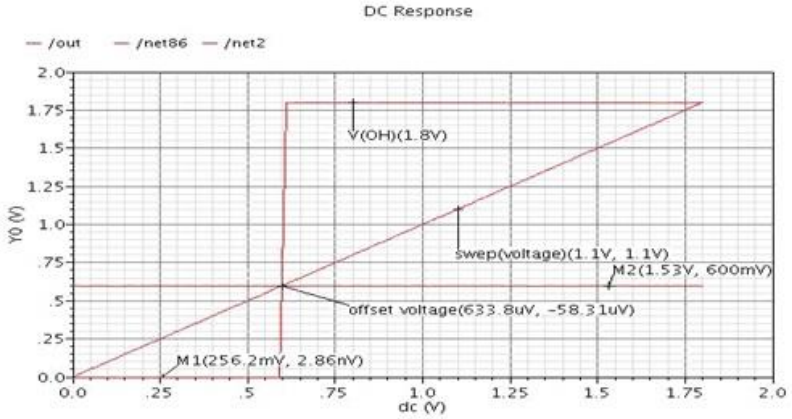

Fig 1.20 DC Response of Preamplifier Latch Based Comparator.

Simulation Result of Preamplifier Latch and Output Buffer Based Comparator

The schematic of preamplifier, latch and output buffer based comparator is shown in Fig 1.3 is simulated in cadence spectra simulator. The results obtained after simulation are shown in Table 1.7.

Table 1.7 Simulation Result of Preamplifier Based Comparator

Parameter	Simulation Result
Ao(dB)	97.61
SR(V/nS)	3.301,-7.57

Rise Time(ns)	.54
Offset(mV)	633.8
Power Consumption (µW)	1.812

Table 1.8 Comparison of three Comparator Circuits

Parameters	Open loop comparator	Composite comparator	Preamplifier latch and output buffer based comparator
Gain (dB)	81.44	80.63	97.6
Slew rate	2.82,-1.9 (v/nsec)	16(v/ µsec)	3.2,-7.1 (v/nsec)
Rise time(ns)	65	143	54
Offset voltage	3.628 mV	44.49 mV	633.8 µV
DC power	71.6128(µW)	18.135(µW)	1.812(mW)

Conclusion

The objective of this work was to design various comparators and compare their performance parameters. During this exercise we were able to design three comparators viz. Open loop comparator, Composite comparator and Preamplifier latch and buffer based comparator. We have also compared their performance parameters like Gain, Slew rate, Rise time, Offset voltage and DC power dissipation. The comparison table given below shows the comparison of all three comparators. The comparison shows that we are able to achieve the minimum specifications of the comparator. Out of all comparators preamplifier latch and output buffer based comparator results are well above the minimum specification values. Typically gain (97.6dB), Offset (811.3 and slew rate are exceptionally above the specified values.

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