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Single Bit 7T Sub-threshold SRAM cell for Ultra Low Power applications

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Abstract

Extensive use of portable low power consuming devices motivates to VLSI designers to develop system on chip design for modern applications. In this paper, PP 7T SRAM cell has been proposed which operates at ultra low supply voltage i.e. in sub threshold, near threshold and super-threshold region. Detailed analysis of SRAM parameters such as stability, delay and power dissipation has been performed with Cadence virtuoso tool at 45nm technology node. It has been observed that read static noise margin (RSNM) of proposed PP 7T SRAM cell is 2.05× and 4.1× improved as compare to conventional 6T and reported 7T SRAM cell, respectively. Read power of proposed PP 7T SRAM cell has reduced by 0.91×/0.66× and write access time improved by 3.22×/1.07× in comparison of Conv. 6T and reported 7T SRAM cell, respectively at 0.5V supply.

Keywords: *RSNM, WSNM, Access time, Sub threshold region.*

1. Introduction

Static random access memory (SRAM) is a kind of semiconductor memory that utilizes bi-stable latch circuitry to store each bit. It is used in portable electronic devices such as body sensor nodes (BSNs), wearable electronics and space applications [1]. In all these applications power dissipation becomes the primary concern and performance is secondary. According to prediction of ITRS 2011 (International technology road map for semiconductor) projection, SRAM occupies over 90% of a processor's chip area. So it occupies a significant portion of area of the processor's. It is therefore, necessary to reduce the power consumption of SRAM. Scaling of the supply voltage is a way to reduce the power dissipation. Nevertheless, the static noise margin (SNM) of 6 T SRAM has been drastically reduced due to a reduction in VDD. Therefore SRAM suffers from read disruption and data instability in the sub-threshold or near-threshold region. The key design parameter for SRAM is depending to its applications [2]. Tomar et al. [13] describes the different low power reduction techniques and implemented on 90nm technology node to minimize the power dissipation. Theoretically, sub-threshold voltage is that voltage in which no conduction current is flow between the drain and source terminal, but in practical applications, due to Boltzmann distribution of electron energies, a flow of electrons between the source-to-drain take place causing the flow of a very small amount of drain current [3].

$$I_D \approx I_{D0} e^{\frac{V_{GS}-V_T}{nV_T}} \quad \ldots\ldots\ldots\ldots (1)$$

In the Eq.(1) represent the sub-threshold current equation [3]. It shows that the drain current has exponential relationship with the gate to source voltage. It is one of the possible solutions for reducing standby power in the circuits. The main limitation associated with the sub-threshold region, it has poor reading stability or poor writing ability [4].

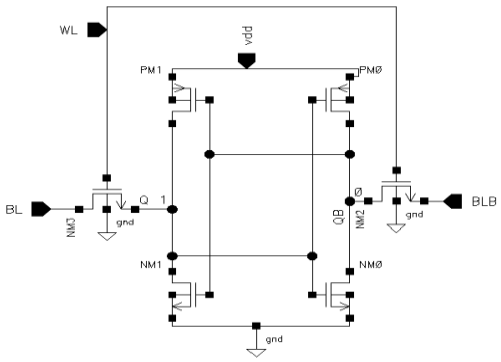

Fig.1: Standard 6T SRAM Cell [5]

For upgrading the read strength and write ability simultaneously Schmitt-trigger based SRAM cell was proposed by Manish Shrivastava et al. [7]. They used Fin-FET technology of multi-gate or tri-gate structure which has smaller area and help to reduce static-power along with improvement in SNM. Jinhui Chen et al. [8] reported that circuit speed is reduced because of small transistor drive current in sub-threshold operation. This problem may be overcome by decreasing the gates at each pipeline stage. Another limitation related to sub-threshold operation introduced in [9] that the smaller value of Ion/Ioff ratio, results to decrease in noise margins. SRAM is treated as a standard circuit and is a dominant part of any System on Chip (SoC). So, increased variations cause drastic change in the performance, stability and functionality of the circuits [10]. To resolve the read stability issue in sub-threshold region is by the help of decoupling the true storing node from the bit lines during read operation [11] Moreover, in order to have improved write-ability, a wider access transistor is desirable [12]. To overcome the issues related to 6T SRAM cell can be resolved by proposed PP 7T SRAM cell with the capability of operating at a sub-threshold voltage with better noise margin.
The rest of the paper is arranged as follows: Proposed PP 7T STAM cell is defined in section II. Simulation results have been thoroughly discussed in Section III. Section IV concludes the paper.

2. Proposed Cell

Fig. 2 depicted the proposed PP 7T SRAM circuit. In this cell transistor NM6 is used for isolated the read and write path to improve the noise margin as well as performance of the circuit in compare with 6T SRAM cell. SRAM has mainly operates in three operating stage: write operation, hold operation and read operation

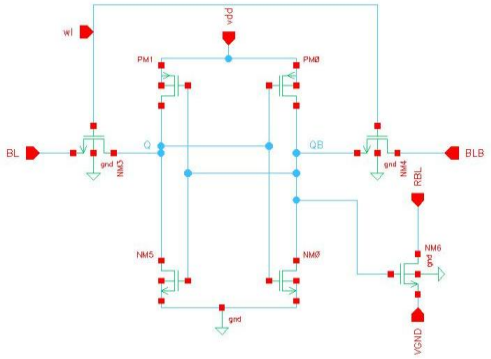

Fig. 2: PP 7T SRAM cell

During read operation the bitline RBL is pre-charged to Vdd while WL signal is disable to perform disturbance free read operation. The read assist transistor (NM6) is connected with the RBL, and source of NM6 is connected with VGND signal. Let us assume that Logic "0" is at storage node Q. It turn on the PMOS of right hand inverter due to that QB maintain its logic "1" and it turn on the NM6 transistor due to that RBL bitline is discharge and give the output logic "0". During write the RBL is at logic "0" and WL signal is at logic "1" that turns on the access transistor to write the data at storage node (Q and QB) by the help of BL and BLB signal. During hold operation RBL and WL signal is disabling to maintain the data at storage node (Q and QB). The supply voltage we used as 0.5V-1.0V to performance evaluation of the circuit.

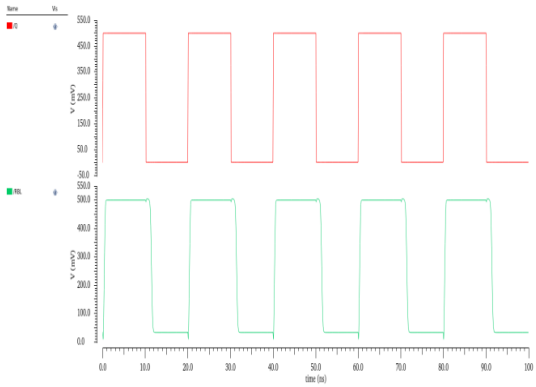

Figure 3: Read Wave form of PP **7T** SRAM

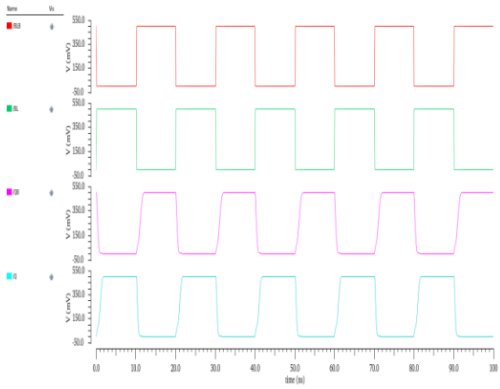

Figure 4: Write Waveform of PP 7T SRAM

3. Simulated Results

In these simulation results of SRAM cells, author uses GPDK 45nm technology file. Author compares the proposed PP 7T SRAM cell with conventional 6T SRAM cell and reported 7T SRAM cell. Supply voltage has been varied from 0.5V to 1.0V.

3.1. Stability

The stability of SRAM cell can be analyzed based on the SNM value. SNM is defined in the form of voltage i.e. the minimum DC noise voltage required to change the state of storage node. In the design of SRAM cell read static noise margin (RSNM) and write static noise margin (WSNM) are the parameters to define the stability.

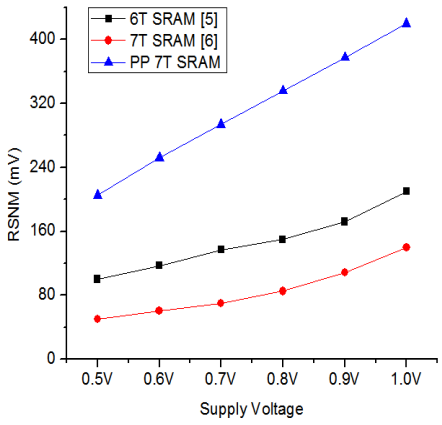

Figure.**5**: RSNM of SRAM topologies

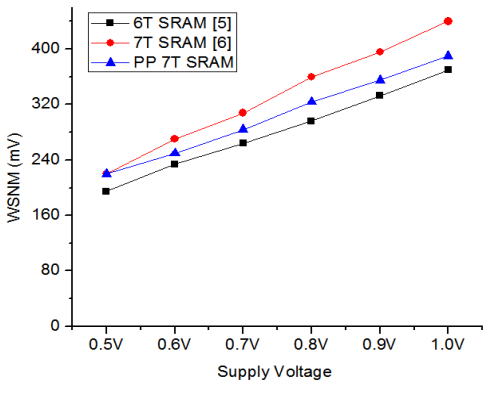

Figure **6**: WSNM of SRAM topologies

The RSNM of the proposed PP 7T SRAM cell is 2.05× and 4.1× improved in comparison with conventional 6T [5] and SRAM [6] respectively. It's because of isolated read and write operation through NM6 transistor. It provides disturb free discharging of RBL in read operation. The proposed cell has 1.21× higher WSNM in comparison of conventional 6T SRAM [5] at 0.5V supply.

3.2. Power Analysis

Basically, power dissipation in SRAM cell involves two major components. One is dynamic power and another is standby power consumption. Standby power, consumed due to leakage current while dynamic power consumed due to the charging and discharging of capacitance during read and write operation.

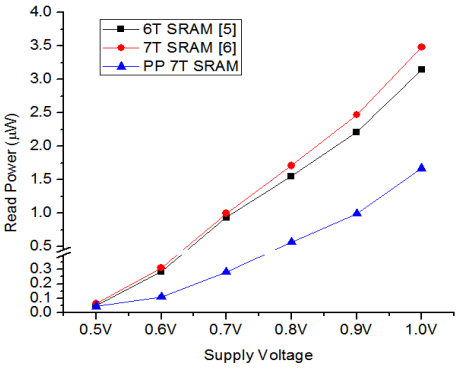

Figure **7**: Read Power of SRAM topologies

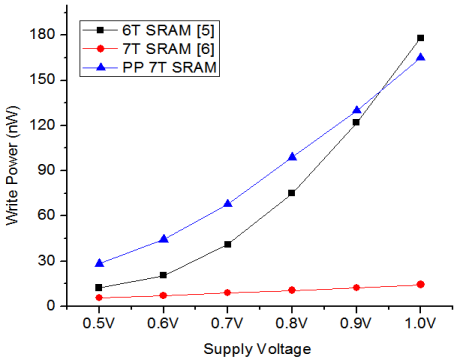

Figure **8**: Write Power of SRAM topologies

Read power of the PP 7T SRAM cell has reduced by a factor of 0.91× and 0.66× with compare to conventional 6T [5] and PP 7T SRAM [6] respectively as shown in Figure 7. It is because during read operation access transistor is off and NM6 transistor provides the fast charging and discharging of bitline capacitance with power dissipation.

3.3 Read/Write access time

In SRAM circuits, access time is classified in two types i.e. read and write access time. Read access time is defined as the crucial time to stream the data from storage to both the bitline while time require to flow the data from write driver circuit to the storage node of the cell, called write access time.

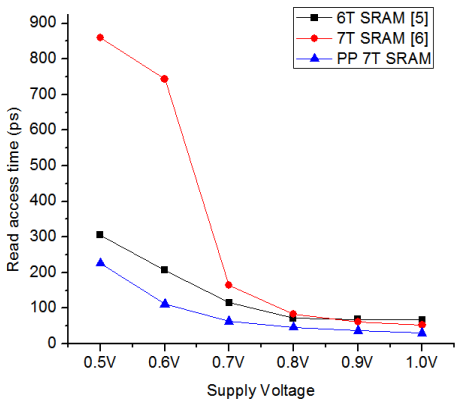

Figure **9**: Read access time

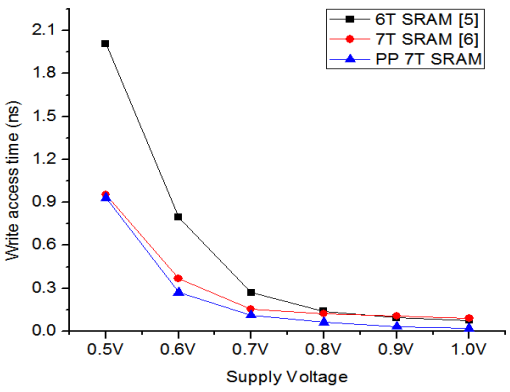

Figure.10: Write access time

Read access time of the proposed PP 7T SRAM cell has reduced by a factor of 5.58× as comparison of 7T SRAM [6]. During read operation access transistor is off and NM6 transistor that provides fast charging and discharging of bit-line capacitance. The write access time of reported PP 7T SRAM cell is 3.22× and 1.07× less as comparison of conventional 6T SRAM [5] and 7T SRAM [6] respectively.

3.4. Layout Area

Layout of the circuit defines the area occupied by the design. It depends on the transistors count as well as transistor channel length.

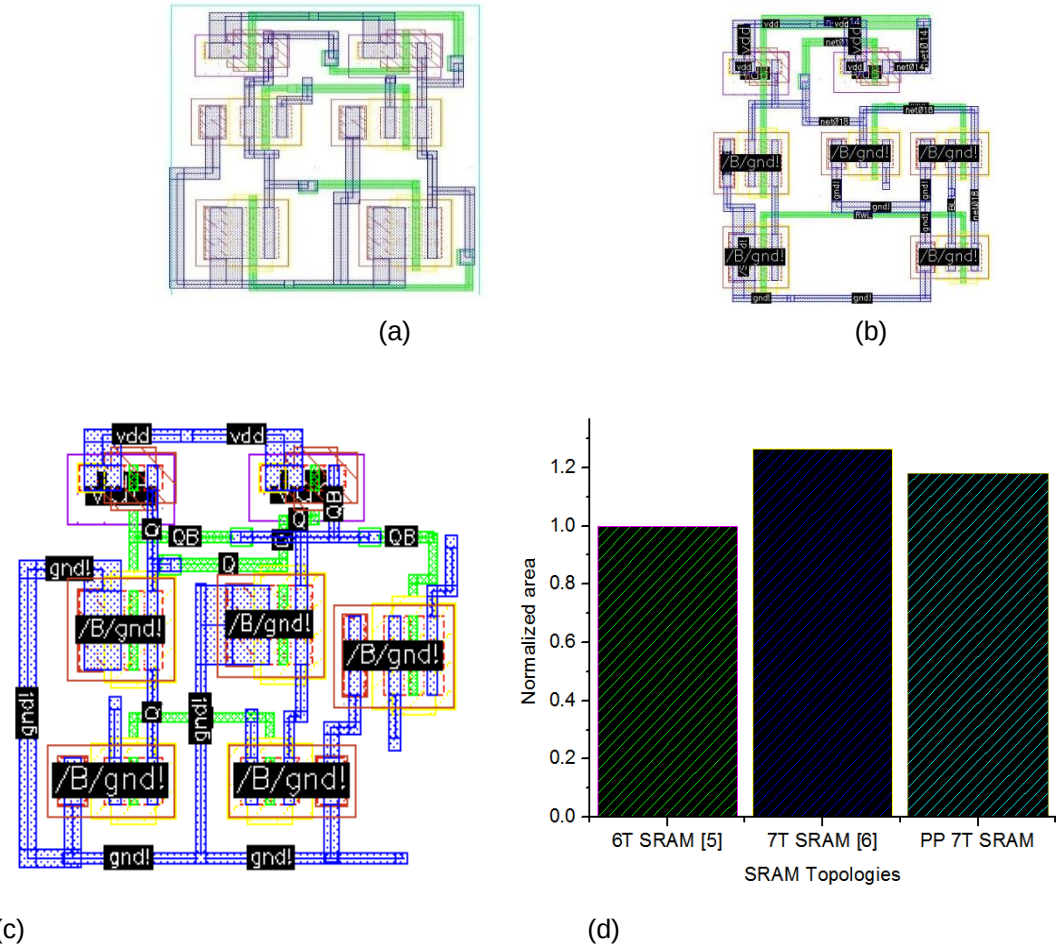

Figure.11 (a) Layout of Conv. 6T SRAM[5] (b) Layout of 7T SRAM [6], (c) Layout of PP 7T SRAM,(d) Normalized area of SRAM Topologies.

Table 1 : Performance Comparison of various simulated bit cell topologies

Parameters ↓	6T SRAM [5]	7T SRAM [6]	**PP 7T SRAM**
RSNM(mV)	100	50	**205**
WSNM(mV)	195	220	**220**
Read access time (ps)	305.2	1860	**333.03**
Write access time (ps)	3090	5170	**956.8**
Read Power (nW)	47	64.69	**43**
Write Power (nW)	12.26	5.17	28.16
Normalized area	1	1.2	**1.1**

All the obtained results of simulated topologies have been summarized in form of table1. In this table it seems that PP7T has better result in comparison of other considered SRAM topologies.

4. CONCLUSION

In this paper, a PP 7T SRAM topology has been proposed and compare with conventional 6T [5] and reported 7T SRAM cell [6]. It has been found that the RSNM of proposed PP 7T SRAM cell better in comparison of conventional 6T and 7T SRAM respectively. Read power dissipation of PP 7T SRAM has reduced in comparison of conventional 6T and 7T SRAM respectively. The write access time of PP 7T SRAM cell has also reduces in comparison of conventional 6T SRAM and 7T SRAM respectively at 0.5V supply. The area of PP7T is less as comparison of previous reported 7T SRAM cell with less complexity.

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Harekrishna Kumar[1*] received the M.Tech Degree in Electronics & Communication from the GLA University, Mathura, Uttar Pradesh, India, in 2018 and the B.Tech degree from the Uttar Pradesh Technical University, India, in 2015. He is pursuing Ph.D. from GLA University Mathura since 2018. He has more than two research papers in reputed conference and international Journals.

V.K. Tomar [2] received Ph.D. degree at Department of Electronics, North Maharashtra University, Jalgaon, Maharashtra in 2008. He was awarded Senior Research Fellowship on the CSIR sponsored project. He is having 15 years of teaching experience which includes 6 years of postgraduate teaching. He has authored more than 45 technical papers in various international conferences and journals of high repute. Presently, He is working as Associate Professor in Department of Electronics and Communication Engineering, GLA University, Mathura. His area of interest includes Low power VLSI design, Sub-threshold Logic Design, High-K and Low –K dielectric materials, Optoelectronics. He is a Member of IEEE.