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Performance Analysis And Design Of 6t Sram Cell Using Different Circuit Techniques

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Abstract

Power Dissipation Is An Important Constraint In Today's Vlsi Technology. In Earlier Days Dynamic Power Dissipation Is Regarded As Major Source Of Power Dissipation. However, Because Of Technology Scaling The Static Power Predominates The Dynamic Power. Static Power Is Mainly Depending On Leakage Current That Flows When The Circuit Is In Idle State. This Leakage Current Increases Exponentially With Reduction In The Supply Voltage And Threshold Voltage [1][2]. Therefore, It Is Necessary To Control The Leakage Power By Early Estimation. The Memory Unit In Today's Digital Systems Are Built Using Dram Or Sram Cell. Sram's Are Widely Used In The Form Of Register Files, Buffers, Instruction Windows And Caches In The High-Performance Processors. Sram Also Contribute Some Amount Of Static Power. Through This Paper We Are Comparing The Performance Analysis Of 6t Sram Cell Using Different Circuit Techniques In Terms Of Power Dissipation And Delay. All Different Circuit Designs Of Sram Cell Is Simulated Using Hspice In 90nm Process Technology With Bsim4 Mos Transistor Models Of Level 54.

Keywords-*Sram Cell, Leakage Power, Lector, Vclearit*

Introduction: Recently There Is A More Demand For High Performance Battery Operated Portable Devices With Large Memory Backup. In These Devices The Memory Is Made Of Sram Or Dram. However, Sram's Are Largely Used At The Processor Level For Faster Operation. Sram Also Consumes Power During Both Active And Idle Mode. In The Idle Mode The Leakage Power Arises From The Leakage Current That Flows When There Are No Transitions At The Input. Power Dissipation Is Composed Of Dynamic And Static Power. Dynamic Power Is Due To Logic Transitions When The Inputs Are Active And Charging And Discharging Of Load Capacitances. Static Power Is Due To Sub-Threshold Leakage Current Which Depends On Current Between Source And Drain Of The Transistor, Reverse Biased Pn Junction, Gate Oxide Tunnelling, Gate Induced Drain Leakage, Drain Induced Barrier Lowering And Hot Carrier Effects [3]. The Leakage Current Is Expressed As

$$\mathrm{I_{Sub}} = \mathrm{I_O}\left(\mathrm{E}^{\frac{\mathrm{V_{Gs}}-\mathrm{V_{Th}}-\mathrm{V_{Off}}}{\mathrm{NV_T}}}\right)\left(1-\mathrm{E}^{-\frac{\mathrm{V_{Ds}}}{\mathrm{V_T}}}\right) \qquad \text{-1}$$

Where I_o Is The Current Dependent On The Geometry Of The Transistor And Equal To $\mathrm{I_{So}}\left(\frac{\mathrm{W}}{\mathrm{L}}\right)$, W Is Width And L Is Length Of The Channel, V_{gs} Is Gate To Source Voltage, V_{th} Is Threshold Voltage, V_{off} Is A Model Parameter, V_t Is The Thermal Voltage Equal To Kt/Q; K And Q Are Physical Constants And T Is The Absolute Temperature, N Is Derived Device Parameters. It Is Observed From Equation (1) That Sub-Threshold Leakage Exponentially Increases With Decrease In Threshold Voltage.

With Technology Scaling And According To Butts And Sohi [4], For A Single Off Device, $V_{ds} = V_{cc}$ And $V_{gs} = 0$ And Using The Approximation $V_{ds} = V_{cc} >> V_t$ The Equation (1) Reduces To

$$\mathrm{I_{Sub}} = \frac{W}{L} I_{so} e^{-\frac{V_{off}}{nV_t}} e^{-\frac{V_{th}}{nV_t}} \qquad \text{-2}$$

$$\mathrm{I_{Sub}} = \frac{W}{L} K_{tech} 10^{-\frac{V_{th}}{sV_t}} \qquad \text{-3}$$

$$\mathrm{I}_{sub} = \mathrm{WI_{Leakage}(T, V_T)} = \mathrm{WI_L} \qquad \text{-4}$$

Where $\mathrm{K_{Tech}} = \mathrm{I_{So}E}^{-\frac{\mathrm{V_{Off}}}{-\mathrm{NV_T}}}$ And S=2.303nv_t. For Devices Such As Sram, All Parameters In The Equation (3) Are Constant Except Width And Length [5]. In Equation (4) $\mathrm{WI_{Lealage}(T, V_T)}$ Is A Constant For A

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Given Threshold Voltage And Temperature. The Above Equations Hold Only Under The Assumption $V_{ds}=V_{cc.}$ For Analytical Leakage Power Estimation, The Leakage Current Of Nmos And Pmos Will Be Considered Separately Since Nmos And Pmos Characteristics Are Different.

Sram: Sram Is A Type Of Random-Access Memory And Is Used To Store Binary Information. Each Sram Cell Can Be Accessed For Read And Write Operation By Enabling Address Decoder In The Memory Array. Sram Cell Is Constructed Using Two Cross Coupled Inverters Along With Access Transistors To Control Data Flow During Read And Write Operation. A 6t Sram Cell Is Shown In The Figure (1). The Cell Operates In Three Modes; Idle, Read And Write Mode.

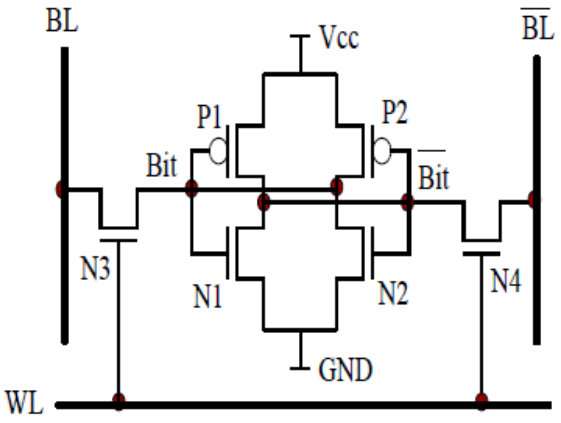

Fig 1. 6t Sram Cell Schematic

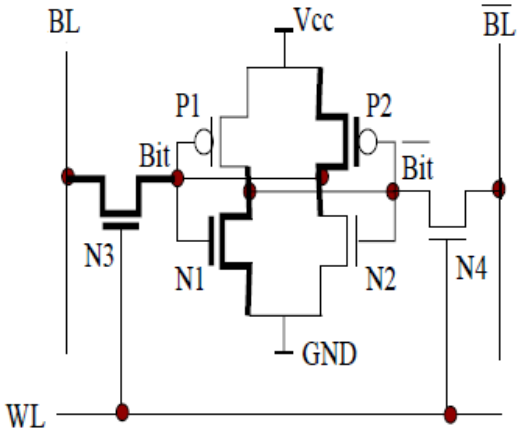

Fig 2. Idle Mode Wl=0, Bit =0, Bl=Blbar=0

Idle Mode: In The Idle Mode As Long As The Word Lines Are Enabled The Bit Lines Are Pre-Charged And Depending Upon The Data On The Cell The Two Cross Coupled Inverters Will Be In Off State For Bit Zero As Shown In The Figure (2). Independent Of Data In The Cell The Leakage Current In The Idle State Is Expressed As

$$I_{Idle} = I_{Sub}(N1) + I_{Sub}(N3) + I_{Sub}(P2) \quad -5$$

Putting Equation (4) In Equation (5), We Obtain

$$I_{Idle} = (W_{N1} + W_{N3})I_{Ln} + W_{P2}I_{Lp} \quad -6$$

Where I_{ln} And I_{lp} Are The Leakage Current Per Unit Width For Nmos And Pmos Transistors.

Read Mode: During Read Mode, Word Lines Are Enabled And Bit Lines Are Pre-Charged To Read The Data On The Cell. Once The Data Is Transferred To The Bit Lines, Now One Of The Bit Line Is Charged To The Supply Voltage And Another Discharge To Zero. The Schematic Of The 6t Sram Cell In The Read State Is Shown In The Figure (3). The Leakage Current During Read State Depends On Two Cases; Case1 When Wl=0 And Case 2 When Wl=1. Assuming Symmetry Of The Transistors The Leakage Current In Two Cases Is Given In The Expression (7).

$$I_{Read} = \begin{cases} (W_{N1} + W_{N3})I_{Ln} + W_{P2}I_{Lp} & \text{For Wl} = 0 \\ W_{N1}I_{Ln} + W_{P2}I_{Lp} & \text{For Wl} = 1 \end{cases} \quad -7$$

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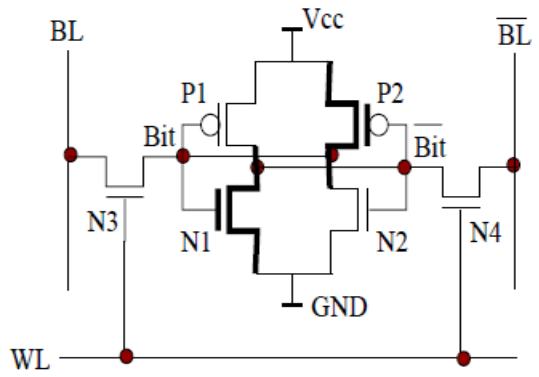

Fig 3. Read State Wl=1, Bit=0

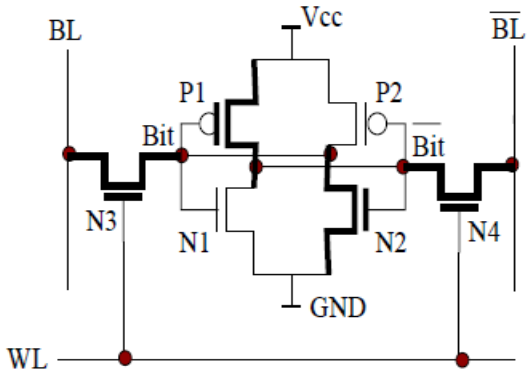

Fig 4. Write State Wl=0, Bit=1, Bl=0, Blbar=1

Write Mode: In The Write Mode, Initially The Word Lines Are Disabled And The Data To Be Stored Is Put On The Bit Lines. Now The Word Lines Are Enabled To Store The Data On The Bit Lines In The Cell. The Schematic Of 6t Sram Cell In Write State Is Shown In The Figure (4). The Leakage Current In The Cell Is Depends On The Word Line Wl, Data In The Cell (Bit, Bit Bar) And Write Data (Bl, Bl Bar). Since The Data In The Cell Is Unknown Initially, Assuming Equal Probability Of 0.5 When Bl==Bit And Bl≠Bit, The Leakage Current Can Be Expressed As

$$I_{Write} = (W_{N1} + W_{N3})I_{Ln} + W_{P2}I_{Lp} = (W_{N1} + 2w_{N3}) + W_{P2}I_{Lp} \quad \text{For Wl=0 And Bl≠Bit} \quad -8$$

$$I_{Write} = W_{N1}I_{Ln} + W_{P2}I_{Lp} \quad \text{For Wl=0 Or 1 And Bl==Bit} \quad -9$$

Sram Cell Using Lector Approach: [6] Leakage Controlled Transistor (Lector) Is A Circuit Technique To Reduce The Leakage Current By Creating Resistance Path Between Supply And Ground In The Standby Mode Of Operation. Figure (5) Shows A Schematic Of 6t Sram Cell Constructed Using Lector Approach In Which A Leakage-Controlled Transistors Pmos And Nmos Are Connected In Series With The Inverters In The Cross Coupled Connection. The Gate Of Leakage-Controlled Transistor Pmos Is Connected To The Source Of Leakage-Controlled Transistor Nmos And Vice Versa. Thus, Each Of The Leakage-Controlled Transistors Operates In Near Cut-Off Region In The Standby Mode And Hence Reduction In The Leakage Current.

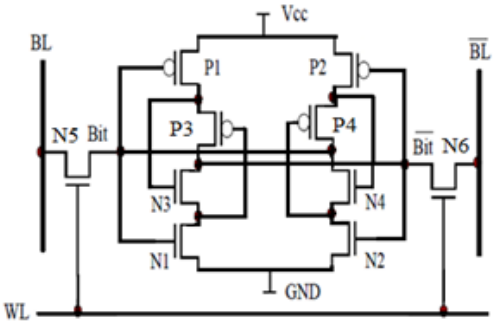

Fig 5. Schematic 6t Sram Cell Using Lector Technique

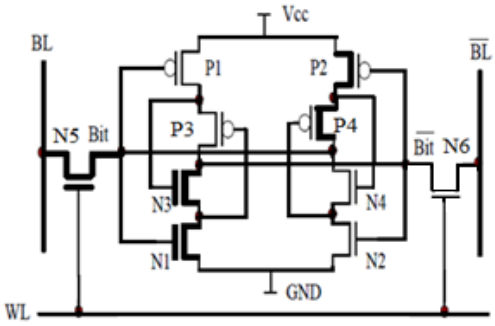

Fig 6. Idle Mode Wl=0, Bit =0, Bl=Blbar=0

Idle Mode: Figure (6) Shows The Schematic Of Sram Cell Using Lector Technique In The Idle Mode Of Operation. In This Mode The Cross Coupled Inverters Reinforce Each Other As Long As The Bit Line Are Pre-Charged And Word Lined Are Enabled. The Leakage-Controlled Transistors Act As Stacked Transistors Operates In Near Cut-Off Region And Provides High Resistance Path. The Leakage Currents In The Ide Mode Is Expressed As

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$$I_{Idle} = (W_{N1} + W_{N3} + W_{N5})I_{Ln} + (W_{P2} + W_{P4})I_{Lp} \quad -10$$

Read Mode: In The Read Mode, The Bit Lines Are Pre-Charged And Word Lines Are Enabled To Read The Bit Stored In The Cell. The Schematic Of 6t Sram Cell Using Lector Technique In Read Mode Is Shown In The Figure (7). The Expression For The Leakage Current In The Read Mode Is

$$I_{Read} = \begin{cases} (W_{N1} + W_{N3} + W_{N5})I_{Ln} + (W_{P2} + W_{P4})I_{Lp} & \text{For Wl} = 0 \\ (W_{N1} + W_{N3})I_{Ln} + (W_{P2} + W_{P4})I_{Lp} & \text{For Wl} = 1 \end{cases} \quad -11$$

Write Mode: The Schematic Of 6t Sram Cell Using Lector Technique In Write Mode Is Shown In The Figure (8). In This Mode The Data To Be Stored In The Cell Is Put In The Bit Lines And Word Lines Are Enabled To Write Data Into The Cell. The Leakage Current In The Cell Is Depends On The Word Line Wl, Data In The Cell (Bit, Bit Bar) And Write Data (Bl, Bl Bar). Since The Data In The Cell Is Unknown Initially, Assuming Equal Probability Of 0.5 When Bl==Bit And Bl≠Bit, The Leakage Current Can Be Expressed As

$$I_{Write} = (W_{N1} + W_{N3} + W_{N5} + W_{N6})I_{Ln} + (W_{P2} + W_{P4})I_{Lp} = (W_{N1} + W_{N3} + 2w_{N5}) + (W_{P2} + W_{P4})I_{Lp} \quad \text{For Wl=0 And Bl≠Bit} \quad -12$$

$$I_{Write} = (W_{N1} + W_{N3})I_{Ln} + (W_{P2} + W_{P4})I_{Lp} \quad \text{For Wl=0 Or 1 And Bl==Bit} \quad -13$$

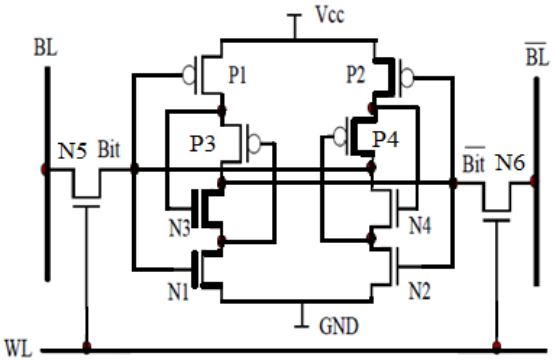

Fig 7. Read State Wl=1, Bit=0

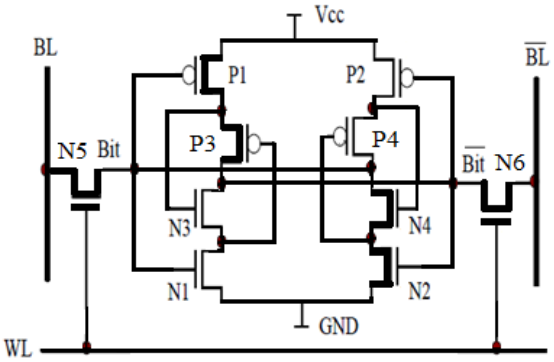

Fig 8. Write State Wl=0, Bit=1, Bl=0, Blbar

Sram Cell Using Vclearit Approach: [7] Vlsi Cmos Leakage Reduction (Vclearit) Is A Circuit Technique To Reduce Leakage Current By Using Combination Of Sleep Transistors. Figure (9) Shows A Schematic Of 6t Sram Cell Using Vclearit Technique In Which A Combination Of High V_t And Low V_t Sleep Transistors Are Connected In The Pull-Up And Pull-Down Circuit.

Idle Mode: In The Idle Mode Of Operation Sleep Transistors Are Turned On To Provide A Direct Path Between The Supply And Ground. Figure (10) Shows The Schematic Of Sram Cell Using Vclearit In The Idle Mode Of Operation. Since Both The Sleep Transistors In The Pull-Up And Pull-Down Operates In The Off Mode During Standby Mode The Leakage Current Due To These Transistors Is Negligible Compare To The Transistors In The Cross Coupled Connection Hence The Leakage Current In The Idle Mode Is

$$I_{Idle} = (W_{N1} + W_{N3})I_{Ln} + W_{P2}I_{Lp} \quad -14$$

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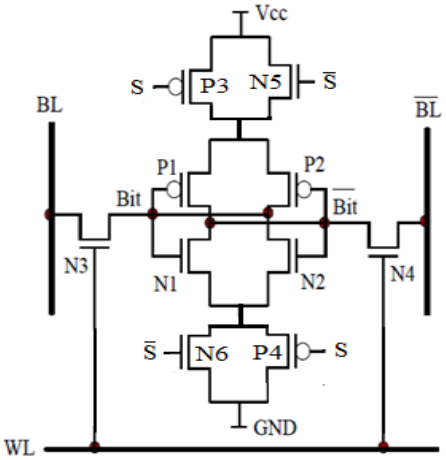

Fig 9. Schematic 6t Sram Cell Using Vclearit Technique

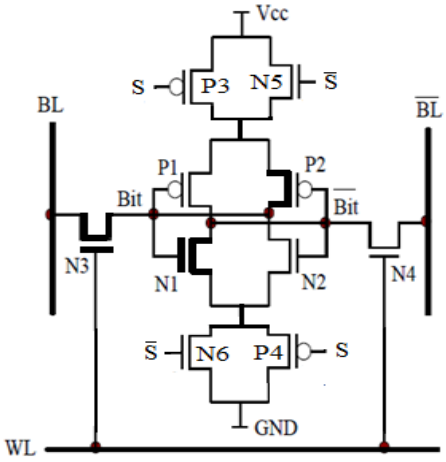

Fig 10. Idle Mode Wl=0, Bit =0, Bl=Blbar=0

Read And Write Mode: In The Read And Write Mode The Sleep Transistors Are Turned On To Behave Like A Cmos Logic. The Schematic Of Sram Cell Using Vclearit Is Shown In The Figure (11) And (12). The Leakage Current Expression In The Read And Write Operation Is

$$I_{Read} = \begin{cases} (W_{N1} + W_{N3})I_{Ln} + W_{P2}I_{Lp} & \text{For Wl} = 0 \\ W_{N1}I_{Ln} + W_{P2}I_{Lp} & \text{For Wl} = 1 \end{cases} \quad \text{-15}$$

$$I_{Write} = (W_{N1} + W_{N3})I_{Ln} + W_{P2}I_{Lp} = (W_{N1} + 2w_{N3}) + W_{P2}I_{Lp} \quad \text{For Wl=0 And Bl≠Bit} \quad \text{-16}$$

$$I_{Write} = W_{N1}I_{Ln} + W_{P2}I_{Lp} \quad \text{For Wl=0 Or 1 And Bl==Bit} \quad \text{-17}$$

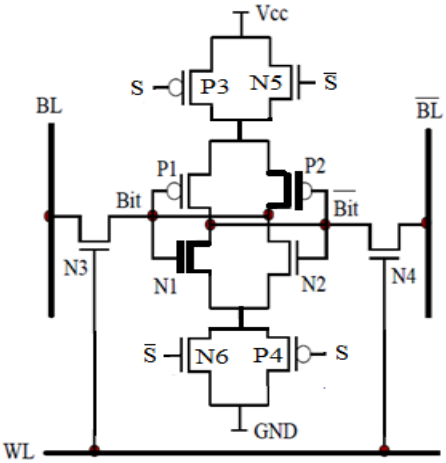

Fig 11. Read State Wl=1, Bit=0

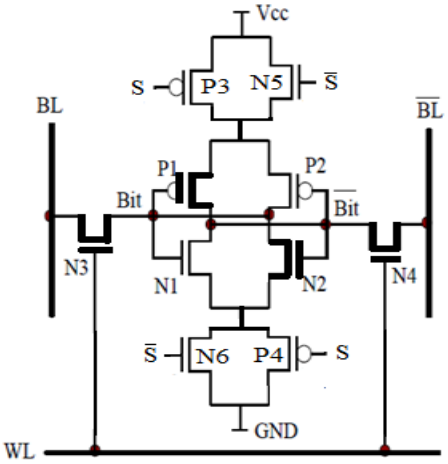

Fig 12. Write State Wl=0, Bit=1, Bl=0, Blbar

Simulation Results: In This Paper We Are Comparing The Performance Analysis Of 6t Sram Cell In Three Different Configurations In Terms Of Average Power Dissipation And Delay. Hspice Simulator Is Used To Simulate All The Three Configurations. Simulation Is Performed In 90nm Process Technology With Bsim4 Mos Transistor Models Of Level 54 For Four Different Supply Voltages. Table 1. Depicts The Power Computation Of Sram Cell In Basic Form, Using Lector And Vclearit Methods. Figure 13, 14 And 15 Depicts The Graph Of Average Power Dissipation Vs Supply Voltages In Idle, Read And Write Mode Respectively. Table 2 And 3 Depicts The Delay Computation In Read And Write Mode Of Operation. Also Figures 16 To 19 Depicts Graph Of Delay Vs Supply Voltages In Three Different

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Configurations. From The Table And Graph, We Can Observe That The Performance Of Sram Cell Using Lector Technique Offers Better Advantage Than Others. It Is Also Observed That Extra Control And Monitor Circuit Is Not Required For Sram Cell Using Lector Technique. In Addition To This Lector Technique Does Not Affect The Dynamic Power Which Is The Main Concern In Reducing The Power Dissipation.

Table 1: Power Computation Of Sram Cell In Idle Mode Of Operation

Idle Mode	Sram Cell				Sram Cell Using Lector				Sram Cell Using Vclearit			
	Vdd In Volts				Vdd In Volts				Vdd In Volts			
	0.8	1	1.2	1.5	0.8	1	1.2	1.5	0.8	1	1.2	1.5
Avg. Power Dissipation (Nw)	13.73	11.48	51.29	181.1	6.636	8.686	27.75	129.1	19.17	11.49	59.44	195.9

Table 2: Power Computation Of Sram Cell In Read Mode Of Operation

Read Mode		Sram Cell				Sram Cell Using Lector				Sram Cell Using Vclearit			
		Vdd In Volts				Vdd In Volts				Vdd In Volts			
		0.8	1	1.2	1.5	0.8	1	1.2	1.5	0.8	1	1.2	1.5
Avg. Power Dissipation (Nw)		20.58	4.554	44.21	165.2	33.08	14.27	74.9	228.8	29.52	6.352	53.59	203.1
Delay (Ps)	Lh	173.3	362.8	362.9	363.3	201.8	201	212.8	212.8	205.8	212.8	212.7	213
	Hl	350.5	362.4	362.9	363.0	130.1	191.8	212.5	212.7	203.8	208.7	212.5	212.8

Table 3: Power Computation Of Sram Cell In Write Mode Of Operation

Write Mode		Sram Cell				Sram Cell Using Lector				Sram Cell Using Vclearit			
		Vdd In Volts				Vdd In Volts				Vdd In Volts			
		0.8	1	1.2	1.5	0.8	1	1.2	1.5	0.8	1	1.2	1.5
Avg. Power Dissipation (µw)		0.497	0.341	0.444	0.852	0.306	1.027	2.893	4.642	0.0322	0.0572	4.05	1.15
Delay (Ns)	Lh	32.93	47.9	70.53	81.7	0.995	1.045	0.996	0.997	37.64	37.68	37.64	38.2
	Hl	26.35	43.05	68.19	99.5	30.89	43.91	61.36	82.54	77.86	77.85	77.83	77.5

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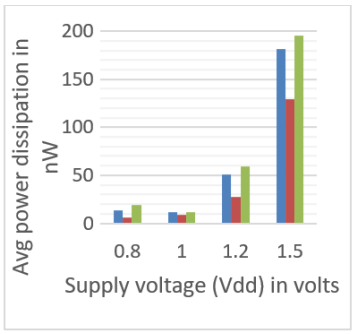

Fig 13. Avg. power dissipation (nW) in idle mode

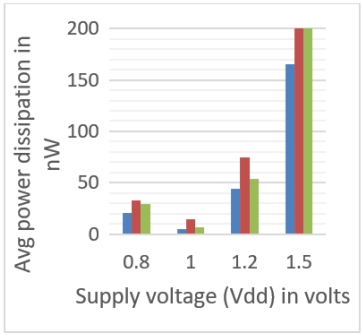

Fig 14. read mode

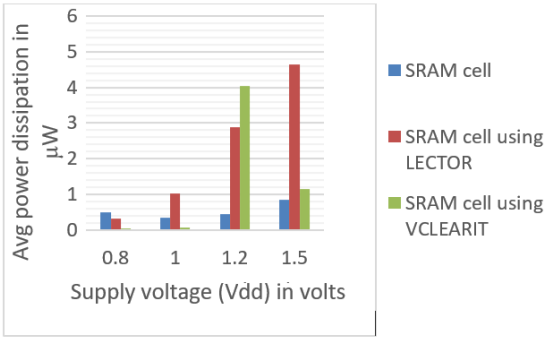

Fig 15. write mode

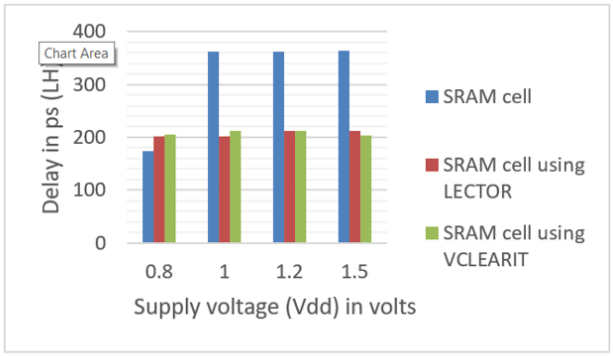

Fig 16. Delay in ps (LH) in read mode

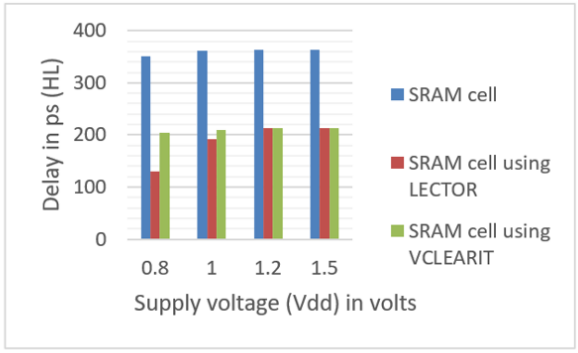

Fig 17. Delay in ps (HL) in read mode

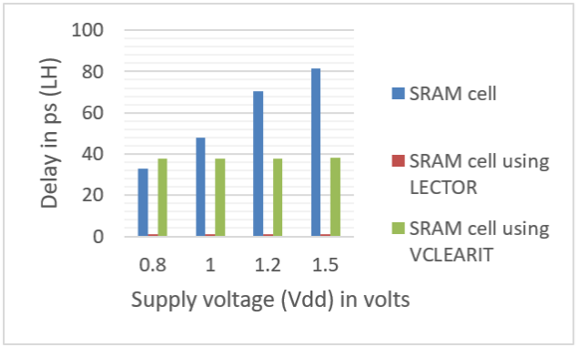

Fig 18. Delay in ps (LH) in write mode

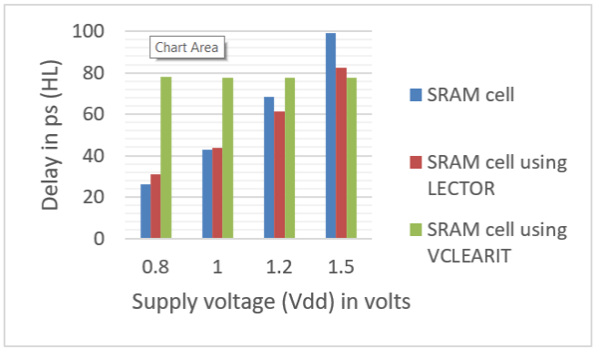

Fig 19. Delay in ps (HL) write mode

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