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Nine Level Symmetrical Modified Multi-Level Cascaded H-Bridge Inverter

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Abstract

In this paper, a 9-level symmetrical modified multi-level cascaded H-bridge inverter with reduced switch count is considered. The operation and control of 9-level inverter is discussed. This multi-level inverter uses four symmetrical DC input sources and twelve unidirectional power semiconductor switches. The basic operation with equal width modulation and resistive and Resistive-Inductive loads are verified with the help MATLAB simulation. The simulation outputs are presented and confirm the operation of nine level inverter operations. Together with the traditional topologies and some other inverters, this inverter topology is capable to produce more number of output voltage levels by means of less number of power switches and driver circuits. Simulation results confirm the probability of this inverter topology

Keywords: *Multi-Level inverter, Cascaded H-Bridge (CHB), Reduced number of switches, Harmonics, Modified H-bridge (MHB).*

1. Introduction

In recent years, immense numbers of researchers are working in the area of multi-level inverters (MLIs). The MLI principle comprises the use of power semiconductor switches to achieve the power translation with smaller voltage steps in the output. There is more attraction towards the MLIs in contrast with the traditional 2-level inverters owing a number of rewards such as lower harmonics distortions in the output, lower voltage pressure on power semiconductor switches, the opportunity of using power semiconductor switches with low voltage rating matured technologies, and inferior electromagnetic interference. Researchers working on MLIs are interested on the aspects of the circuit topology and its control methods.

The basic circuit topologies of "diode clamped multi-level inverter" [1], "capacitor clamped multi-level inverter" [2] and "cascaded multi-level inverter" [3] have been offered for MLIs. The circuit effortlessness, lesser number of components and easy control of multi-level cascaded inverters make this type of configuration more popular among the researchers [4-8].

This paper considers on cascaded MLIs. This topology of MLI is consisting of the number of H-Bridge (HB) inverters linked in series. Each HBs in this comprises of a DC input source and number of interconnected power switches. This inverter topology can be extended to higher voltage levels by adding more HBs in series. This Cascaded H-Bridge Multi-Level Inverters (CHBMLI) is two types: symmetrical and asymmetrical MLIs. The symmetrical CHBMLI is the inverter which uses all the DC input voltage sources has equal values. In asymmetrical CHBMI, the DC input voltage sources have dissimilar values. The symmetrical inverters require more power semiconductor switches as the number of output levels increases. This increases the complexity of the entire system, whereas the semiconductor switches requires for the identical number of output levels is less. In symmetrical inverters all the H-bridges are same and modular, this reduces the design cost. The drawback of the asymmetrical inverter is losing of its modularity due to its variation in the ratings of the power switches.

The most noticeable drawback of MLIs is more number of power switches requirement. It is significant to mention that the switches used are low voltage rating switches. Therefore it is cheaper than the high-power switches used in the traditional 2-level inverters. At the same time, each power switches needs its own driver circuits which raise the overall volume of the inverter.

In this paper, a modified CHB symmetrical MLI introduced by Bahravar *et al*. [10] and reviewed by Prabhu Omer *et al.* [11] is considered. This type of inverter uses lesser number of components to produce similar output levels in contrast with traditional CHBMLI. The operation of this topology of inverter is explained and analyzed through the simulation study of 9-level inverter with two symmetrical DC voltage sources and 12 power semiconductor switches. The simulated outputs with R-load and RL-load are presented.

2. Topology Description

In Figure 1, the basic circuit diagram of symmetrical modified CHBMLI topology with condensed assortment of values of DC voltage sources. This inverter is designed by connecting modified HBs in series. Each modified HB contains six uni-directional power switches and two DC sources. The switches S_{x1} and S_{x2} in each H-bridge should be operated in complementary manner. All the DC sources are regarded as being of equal value. The maximum voltage obtained from each HB is $V_{x1}+V_{x2}$. For 9-level output, two modified HBs with 12 unidirectional power switches and 4 symmetrical DC voltage sources are used as shown in Figure 2. For greater output levels, more number of HBs can be connected in series with this circuit. The appropriate switching operation of the switches in this topology produces a 9-level output voltage. Table 1 summarizes the switching patterns of all the switches in this topology.

For each and every level of output, three switches are in conduction mode from one H-bridge module. The voltage across the load is equivalent to the algebraic sum of the output of all the HBs.

$$V_o = V_{o1} + V_{o2} + \cdots + V_{on} \qquad (1)$$

For positive output voltage from the each HB module, the switches T_{x1} and T_{x4} are in ON position and for negative output voltage the switches T_{x2} and T_{x3} are in ON position. The switches S_{x1} and S_{x2} are operated in complementary to get different levels of output.

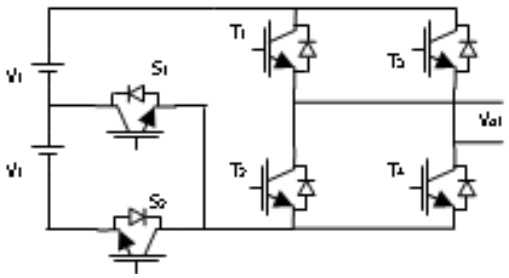


Figure 1 Generalized Basic Circuit for Cascaded Modified H-Bridge inverter

The DC input source values are equal and considered as V_{dc}.

$$V_{11} = V_{12} = V_{21} = V_{22} = V_{dc} \qquad (2)$$

The quantity of output steps (N_{step}) = $4n + 1$ (3)
where, n is the quantity of H-bridges.

The quantity of power semiconductor switches (N_{sw}) = $6n$ (4)

The number of DC input sources (N_{source}) = $2n$ (5)

Maximum generated output voltage (V_{omax}) = $2nV_{dc}$ (6)

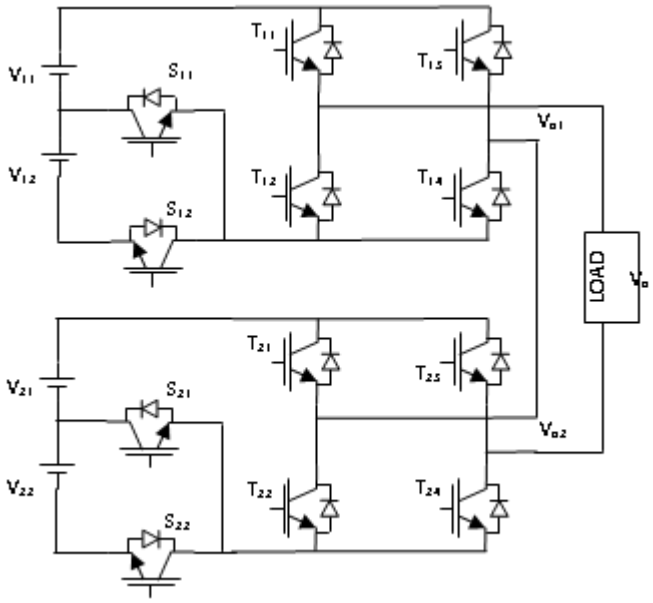


Figure 2 Circuit Diagram of Symmetrical 9-Level Modified CHBMLI

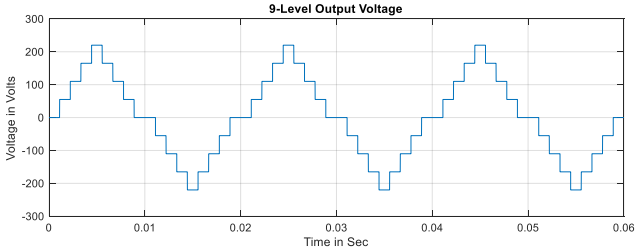
Table 1 Switching functions of 9-Level Symmetrical Modified CHBMLI

Lev	Outpu Volta	Switching Functions	
		S_{11} S_{12} T_{11} T_{12} T_{14}	S_{21} S_{22} T_{21} T_{22} T_{24}
1	4V	011001	011001
2	3V	011001	101001
		101001	011001
3	2V	101001	101001
		011001	xx1010/xx0101
		xx1010/xx0101	011001
4	V	101001	xx1010/xx0101
		xx1010/xx0101	101001
5	0	xx1010/xx0101	xx1010/xx0101
6	-V	100110	xx1010/xx0101
		xx1010/xx0101	100110
7	-2V	100110	100110
		010110	xx1010/xx0101
		xx1010/xx0101	010110
8	-3V	010110	100110
		100110	010110
9	-4V	010110	010110

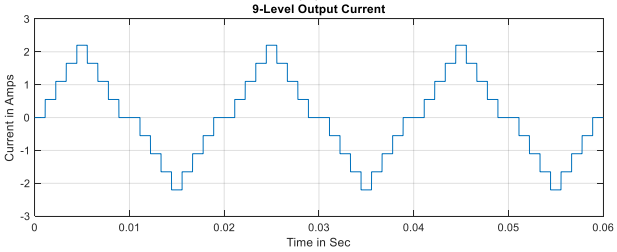
3. Results and Discussions

The feasibility of the 9-level symmetrical modified CHBMLI, we performed simulations using MATLAB / Simulink. The composition of this topology corresponds to the inverter discussed earlier, two modified H-bridges with 4 DC input voltage sources and twelve unidirectional power switches were used. The triggering pulses for the power switches were produced using the pulse generators.

The 9-level simulated load voltage and load current for R-load are shown in Figure 3(a) and Figure 3(b). The harmonic spectra of the corresponding outputs are shown in Figure 4. It produces 9-level voltage and current outputs with the Total Harmonic Distortion (THD) of 25.62% and also nearly all the harmonics of the lower order are much less than the third harmonic which is around 20%. The simulated voltage and current output waveforms with RL-load is shown in Figure 5(a) and Figure 5(b) respectively. The harmonic spectra of output voltage and current with RL-load are shown in Figure 6. From these figures, output voltage is the 9-level multi-stepped waveform and the current waveform is almost the sine waveform because of the inductive nature of the load. The THD of the voltage and current output are 25.57% and 12.65% respectively. From the FFT spectrum of the output current, it is interesting to note that all harmonics of the lower order are below 2% except for the third harmonic.



(a)



(b)

Figure 1 Voltage and Current Output waveforms of 9-Level Inverter with R-Load

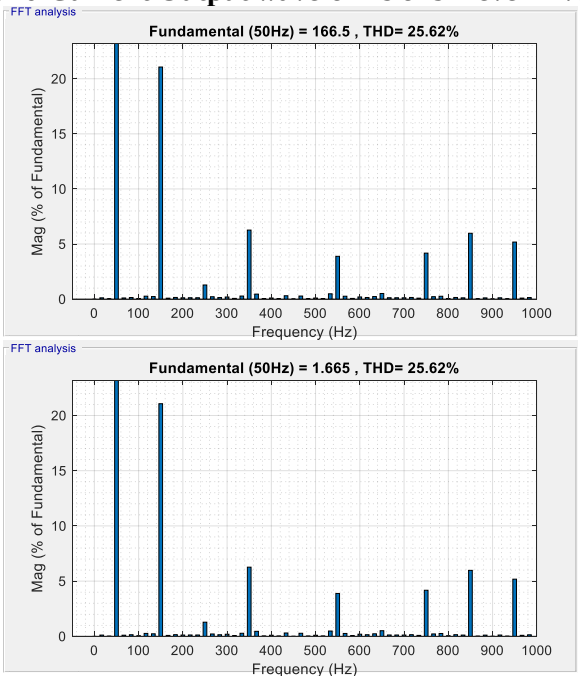
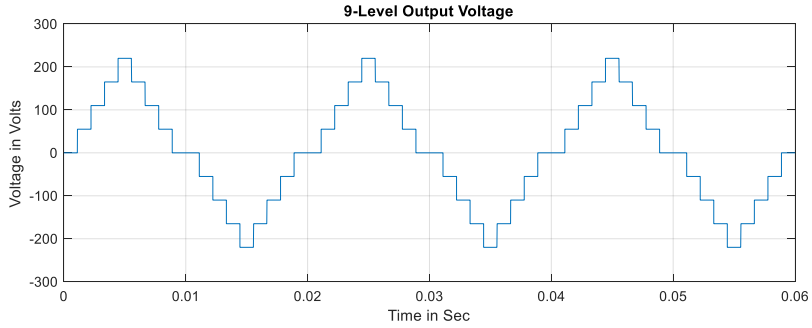
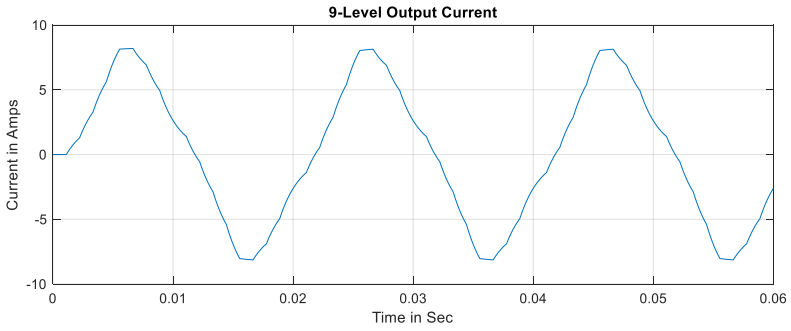


Figure 2 Harmonic Spectra of Nine-Level Voltage and Current Output with R-Load



(a)



(b)

Figure 3 Voltage and Current Output waveforms of 9-Level Inverter with RL-Load

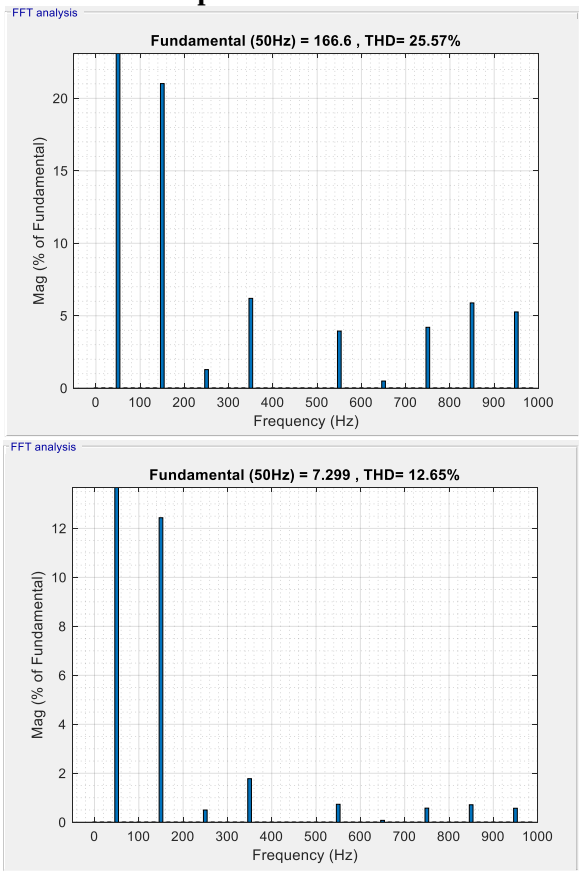


Figure 4 Harmonic Spectra of 9-Level Voltage and Current Output with RL-Load

4. Conclusion

In this paper, a modified CHB 9-level symmetrical MLI with 4 DC voltage sources and 12 unidirectional switches was successfully studied with the help of MATLAB simulation. The operation of this topology of inverter is analyzed. The simulation results are at satisfactory level.

The harmonics in the output voltages are comparable with the other topologies in the literature. This topology of inverter required less number of switches could assure enhanced performance, efficiency, consistency and decrease in price and volume of the inverter. The performance of this inverter topology can be improved by employing harmonic elimination techniques.

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