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Simulation Analysis of New Symmetric/Asymmetric Type Multilevel Inverter Topology

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Abstract:
Multilevel inverters can synthesize a high output voltage staircase waveform using much lower rated switches. This article proposes a new inverter topology with least number of switching devices. The proposed inverter comprises of four sources and ten switches to create higher output levels. This topology can be worked with equal and unequal voltage magnitudes. To prove the superiority of the proposed topology, the comparison study is performed with other existing topologies based on various performance indices. To exhibit the operation and overall performance of the proposed topology, the simulation results are presented for 9-level, 17-level and 25-level inverter operations.
Keywords: multilevel inverter, symmetric, asymmetric, switching angle, THD

1. Introduction

Multilevel inverter (MLI) is a prominent power converter for medium voltage applications since it offers various advantages like low dv/dt stress, high voltage capability, reduced common mode voltages, lesser harmonics, minimum switching losses and reduced electromagnetic interferences. It synthesizes a stepped waveform with the help of multiple sources, switches and its control circuit [1]. MLI technology can be used in various medium voltage, high power applications such as flexible AC transmission system (FACTS), traction drives, high voltage dc (HVDC) system, grid-connected renewable energy applications etc. [2, 3]. The most commercial MLI topologies include cascaded H bridge (CHB),diode-clamped and flying-capacitor [4,5]. MLI topologies can be grouped as symmetric and asymmetric topology. In symmetric, the magnitude of the sources are same whereas they are not same in asymmetric configuration[6]. As compared with the symmetric topology, more output levels can be generated with same number of sources and switches using asymmetric configuration[7]. In recent years, various MLI topologies have been suggested for reducing the number of switches and associated driver circuits which in turn reduces the space and cost of the inverter [6-10]. However, this will increases the number of sources and power rating of the switching devices for higher levels. The objective of this paper is to propose a symmetric and asymmetric type inverter circuit with reduced switch count to generate higher output levels. Section 2 explain the various operating modes of the inverter. The comparison study is given in Section 3. Section 4 presents the simulation results for 9-level, 17-level and 25-level inverter operations. Section 5 concludes the paper.

2. Proposed Inverter Topology

The proposed MLI-topology consists of four dc sources and ten switches is shown in Fig.1. It can create 9-level output voltage during symmetric operation and 25-level output voltage during asymmetric operation. The proposed inverter can be operated during equal and unequal magnitude of dc voltage sources and it creates both the positive and negative output voltage levels without any polarity changing circuit. The maximum output voltage obtained across the load is given by

$$V_o = V_1 + V_2 + V_3 + V_4 \qquad (1)$$

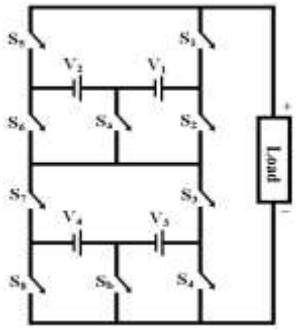
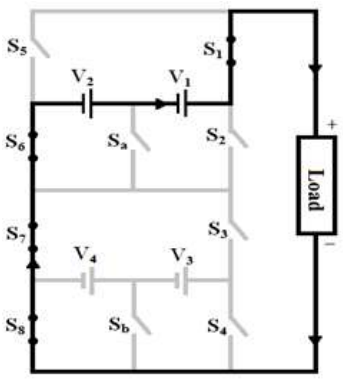
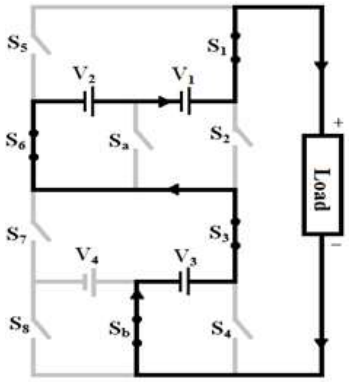


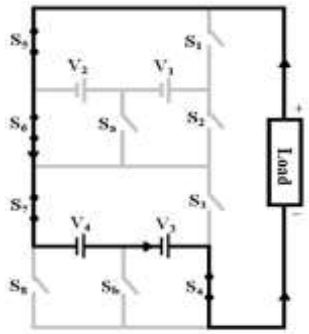
Fig. 1. Proposed inverter



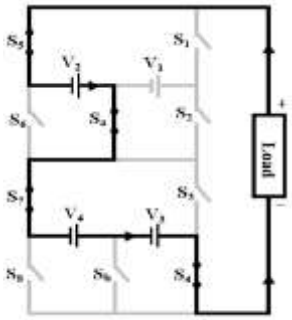
(a) V_1+V_2



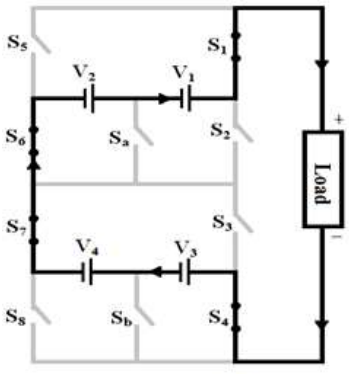
(b) $V_1+V_2+V_3$



(c) $-(V_3+V_4)$



(d) $-(V_2+V_3+V_4)$



(e) $V_1+V_2-V_3-V_4$

Fig. 2. Different output levels

Fig. 2 shows the different output levels of the proposed inverter topology. To avoid short circuit, the pair of switches (S1,S5), (S3,S7), (S2, S6, Sa) and (S4, S8, Sb) should not be turned on at the same instant. The maximum output level during positive cycle is achieved by turning on the switches S1, S3, S6 and S8. Similarly, the maximum output level during negative cycle is achieved by turning on the switches S2, S4, S5 and S7. The zero voltage can be obtained either by tuning on the switches (S1,S2,S3,S4) or (S5,S6,S7,S8) respectively. It is seen that only four switches were conducting to synthesize any required output levels.

3. Comparison Study

To prove the superiority of the proposed topology, the comparison study is performed with other existing topologies based on various performance indices such as the number of sources, switches and on-state switches are discussed in this section. Table 1 and Table 2 presents the detailed comparison of the proposed topology during symmetric and asymmetric operations respectively. From the table, it is observed that the proposed topology uses minimum number of switches and dc voltage sources to generate larger output level, thereby reduce the size and cost of the inverter. In the proposed inverter topology, the number of on-state switches is minimum as four as compared with other topologies. This will minimizes the switching losses and improves the efficiency of the inverter.

Table 1 Comparison during symmetric operation

Topology	Number of Voltage sources	Number of Switches	Number of On-state Switches	Output Level
CHB	4	16	8	9
[3]	4	10	5	9
[4]	4	12	4	9
[6]	4	12	8	9
[7]	4	12	5	9
Proposed	**4**	**10**	**4**	**9**

Table 2 Comparison during asymmetric operation

Topology	Number of Voltage sources	Number of Switches	Number of On-state Switches	Output Level
[3]	4	10	5	15
[8]	4	10	4	17
[10]	4	10	4	21
CHB	4	16	8	21
Proposed	**4**	**10**	**4**	**25**

4. Simulation Results And Analysis

The simulation results of the proposed inverter topology for symmetric and asymmetric operations are presented in this section. A series RL load with R = 15 Ω and L = 45 mH is connected across the load

terminals. main switching angles corresponding to the period 0° to 90° and are determined using the following equation [9,10].

$$\theta_i = \sin^{-1}\left(\frac{2i-1}{n-1}\right), i = 1,2,\ldots,\left(\frac{n-1}{2}\right) \qquad (2)$$

Table 3 shows the main switching angles of the proposed inverter topology.

Table 3 Main Switching Angles

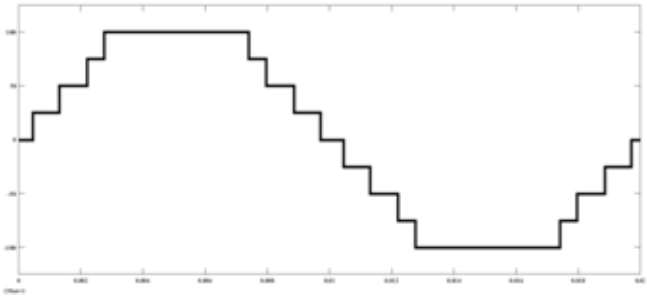
Output Level	Switching Angles (in degree)			
9-Level	θ_1= 7.18	θ_2 = 22.02	θ_3= 38.68	θ_4= 61.04
17-Level	θ_1= 3.58	θ_2=10.81	θ_3= 18.21	θ_4= 25.94
	θ_5=34.23	θ_6= 43.43	θ_7= 54.34	θ_8= 69.63
25-Level	θ_1= 2.39	θ_2= 7.18	θ_3= 12.02	θ_4= 16.96
	θ_5= 22.02	θ_6= 27.28	θ_7= 32.80	θ_8= 38.68
	θ_9= 45.10	θ_{10}= 52.34	θ_{11}= 61.04	θ_{12}= 73.40

A. Symmetrical -9-level

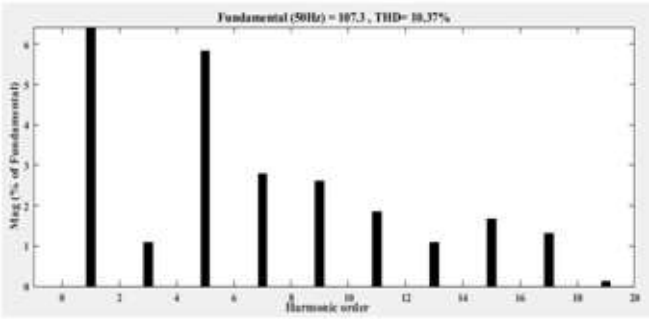
In this case, the magnitude of the all dc voltage sources are equal to 25 V i.e., $V_1 = V_2 = V_3 = V_4 = 25$ V. Therefore, the maximum output voltage obtained across the load is 100 V. Fig. 3 shows the simulation results of symmetric 9-level inverter. The switching table for the 9-level inverter is given in Table 4.It is shown that the THD of the 9-level waveform is 10.37%.

Table 4 On-state Switches for 9-level inverter

Output Voltage	On-State Switches	
	Positive Cycle	Negative Cycle
0	S_1,S_2,S_3,S_4	S_5,S_6,S_7,S_8
V_{dc}	S_1,S_2,S_3,S_b	S_5,S_7,S_8,S_a
$2V_{dc}$	S_1,S_2,S_3,S_8	S_2,S_5,S_7,S_8
$3V_{dc}$	S_1,S_3,S_8,S_a	S_2,S_5,S_7,S_b
$4V_{dc}$	S_1,S_3,S_6,S_8	S_2,S_4,S_5,S_7



(a) Output voltage

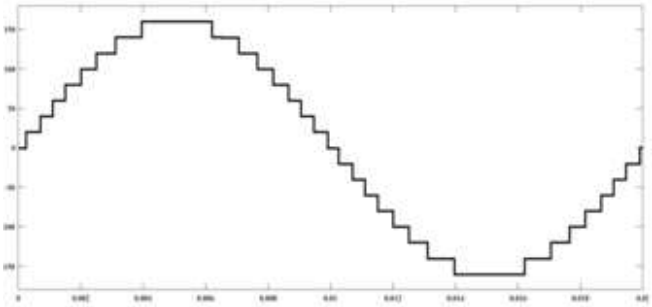


(b) THD

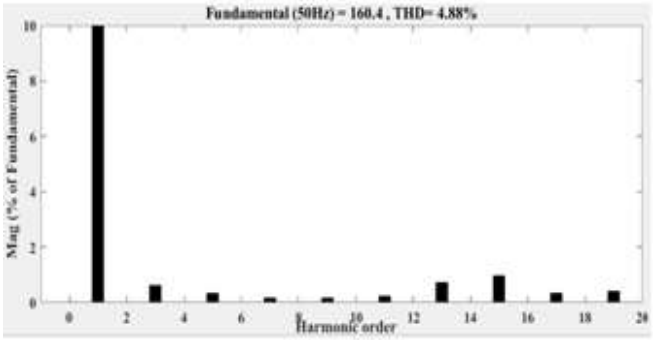
Fig. 3. Simulation results of 9-level inverter

B. Asymmetrical -17-level

In this case, the magnitude of the dc voltage sources are chosen as $V_1 = V_2 = 20V$ and $V_3 = V_4 = 60V$. The simulation results of asymmetric 17-level inverter is shown in Fig. 4. The switching table for asymmetric operation of the 17-level inverter is given in Table 5.It is seen that the obtained maximum output voltage across the load is 160V with THD as 4.88%.



(a) Output voltage



(b) THD

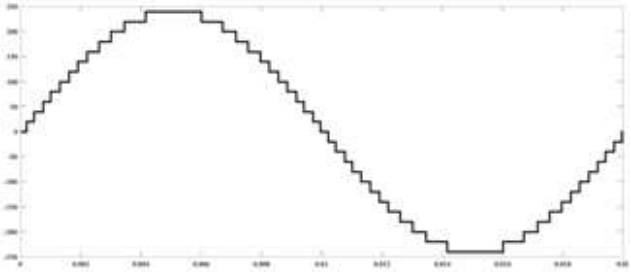
Fig. 4. Simulation results of 17-level inverter

Table 5 On-state Switches for 17-level inverter

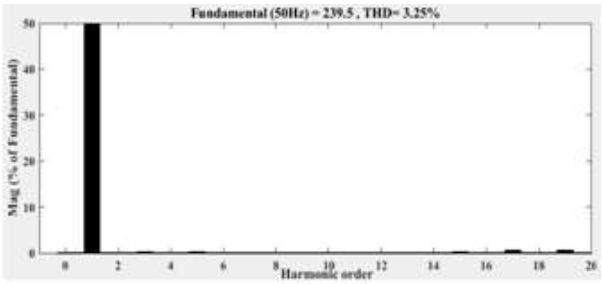
Output Voltage	On-State Switches	
	Positive Cycle	Negative Cycle
0	S_1,S_2,S_3,S_4	S_5,S_6,S_7,S_8
V_{dc}	S_1,S_7,S_8,S_a	S_3,S_4,S_5,S_a
$2V_{dc}$	S_1,S_6,S_7,S_8	S_2,S_3,S_4,S_5
$3V_{dc}$	S_1,S_2,S_3,S_b	S_5,S_6,S_7,S_b
$4V_{dc}$	S_1,S_3,S_a,S_b	S_5,S_7,S_a,S_b
$5V_{dc}$	S_1,S_3,S_6,S_b	S_2,S_5,S_7,S_b
$6V_{dc}$	S_1,S_2,S_3,S_8	S_4,S_5,S_6,S_7
$7V_{dc}$	S_1,S_3,S_8,S_a	S_4,S_5,S_7,S_a
$8V_{dc}$	S_1,S_3,S_6,S_8	S_2,S_4,S_5,S_7

C. Asymmetrical -25-level

In this case, the magnitude of the dc voltage sources are chosen as $V_1 = V_2 = 20V$ and $V_3 = V_4 = 100V$. The maximum output voltage obtained across the load is 240V. The simulation results of asymmetric 25-level inverter is shown in Fig. 5. It is seen that the THD of the 25-level output voltage waveform is 3.25%.



(a) Output voltage



(b) THD

Fig. 5. Simulation results of 25-level inverter

The switching table for asymmetric operation of the 25-level inverter is given in Table 6.

Table 6 On-state Switches for 25-level inverter

Output Voltage	On-State Switches	
	Positive Cycle	Negative Cycle
0	S_1,S_2,S_3,S_4	S_5,S_6,S_7,S_8
V_{dc}	S_1,S_3,S_4,S_a	S_5,S_7,S_8,S_a
$2V_{dc}$	S_1,S_3,S_4,S_6	S_2,S_5,S_7,S_8
$3V_{dc}$	S_2,S_3,S_5,S_b	S_1,S_6,S_7,S_b
$4V_{dc}$	S_3,S_5,S_a,S_b	S_1,S_7,S_a,S_b
$5V_{dc}$	S_1,S_2,S_3,S_b	S_5,S_6,S_7,S_b
$6V_{dc}$	S_1,S_3,S_a,S_b	S_5,S_7,S_a,S_b
$7V_{dc}$	S_1,S_3,S_6,S_b	S_2,S_5,S_7,S_b
$8V_{dc}$	S_2,S_3,S_5,S_8	S_1,S_4,S_6,S_7
$9V_{dc}$	S_3,S_5,S_8,S_a	S_1,S_4,S_7,S_a
$10V_{dc}$	S_1,S_2,S_3,S_8	S_4,S_5,S_6,S_7
$11V_{dc}$	S_1,S_3,S_8,S_a	S_4,S_5,S_7,S_a
$12V_{dc}$	S_1,S_3,S_6,S_8	S_2,S_4,S_5,S_7

5. Conclusion

A new MLI topology with minimum switches has been presented in this paper. The presented topology is capable to operate in both symmetric and asymmetric configurations. The proposed inverter generate both positive and negative levels without any additional circuit at the inverter output terminals. The different comparisons have been carried out to show the superiority of the proposed inverter. The performance of the proposed topology is examined for 9-level, 17-level and 25-level inverters using MATLAB/Simulink software. The results exhibit the good feasibility of the proposed inverter for low and medium voltage applications.

6. Acknowledgement

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