International Journal of Advanced Science and Technology
Vol. 29, No. 7s, (2020), pp. 1481-1487

# Parametric Optimization of Architectural Modified FIR Filter

T.Shanmugaraja*, B.Jai Shankar# K.Siddharthraju*, K.Murugan*, T.Venkatesh*, R.Dhivyadevi*, M.Supriya,

** Assistant professor, KPR Institute of Engineering & Technology, Coimbatore*
*# Associate professor, KPR Institute of Engineering & Technology, Coimbatore*

***Abstract:***

*In digital signal processing, FIR filters are used with a finite time impulse response and because of it, in a finite time, it settles to zero. Before settling into zero, N+1 precise samples are taken by Nth order discrete time FIR filter's impulse response. It may be digital, continuous, analog or discrete FIR filter used in VLSI projects requires low power, low area or low delay for different applications. In order to implement the FIR filter with low area and less delay application in single structure, the proposed architecture which Systolic Architecture along with Associativity is designed in this project. Once the functionality of the FIR filter is verified using Verilog coding, the different architectures are implemented in Spartan in XILINX ISE to obtain the performance analysis. The proposed structure which includes FIR structure designed with Systolic architecture along with Associativity is designed and performance analysis is determined. For 8-tap FIR filter LUT consumed by the Associativity architecture is 77% less than the direct form structure and the delay obtained by the systolic architecture is 60.46% less than the direct form structure for 8-tap FIR filter and LUT consumed by the proposed architecture(Systolic with Associativity )is 28% less than the direct form structure ,the delay obtained by the proposed architecture(Systolic with Associativity ) is 61.38% less than the direct form structure for 8-tap FIR filter. For 13-tap FIR filter the LUT consumed by the Associativity architecture is 19.23% less than the direct form structure and the delay obtained by systolic architecture is 26.46% less than direct form structure for 13-tap FIR filter and LUT consumed by the proposed architecture is 16.92% less than the direct form structure and the delay obtained by the proposed architecture is 26.5% less than the direct form structure for 13-tap FIR filter. So for the architecture with less area and less delay VLSI application the FIR filter designed using Systolic with Associativity can be designed. In future work this architecture can be implemented in Adaptive filter structures.*

**Keywords:** Folding, transpose, systolic, associativity, XILINX ISE

## 1. INTRODUCTION

A filter is the basic signal processing circuit used in communication systems and physical applications. Filters are the electronic circuits which allow or transmit the desired band of frequencies and attenuate the unwanted band of frequencies. Digital filters process and generate digital data. Digital filters consist of elements like adder, multiplier and delay unit. The properties of a causal digital filter can be completely characterized by its unit-sample response h(n), or its transfer function H(z).

Finite Impulse Response (FIR) advanced filter is a typical segment in numerous computerized signals handling (DSP) framework. In signal handling, a finite motivation reaction filter assumes an imperative job in plan and investigation. With the quick advancement in huge scope mix (VLSI) innovation, the ongoing acknowledgment of FIR filter with less equipment necessity has decreased postponement and less idleness has gotten progressively significant. By and large, the speed of the structure is contributed by the basic way for example the longest way. The basic way length is legitimately related with the interconnect way which exist between sub-modules. This interconnected configuration chooses the longest way of proliferation. In any framework structure the math units are as much significant as to make it a fruitful plan. The postpone requirement is being met by the quantity of adders and multipliers utilized in the FIR information flow chart engineering and the configuration in which how they are interlinked chooses the presentation of FIR filter. Adders and multipliers assume a significant job in the

ISSN: 2005-4238 IJAST

plan of FIR filter, since the all out deferral relies upon the postpone taken by number of adders and multipliers present in the engineering dependent on the N esteem in a N-tap filter. The speed of the structure can be improved by limiting the postponement in the design of adders and multipliers that may prompt better execution. A few calculations have been proposed for the sub-modules utilized in the writing for having compelling structures and executed utilizing ASIC and FPGA.

## 2. PROPOSED MODEL

The proposed architecture is the Fir filter design using Systolic architecture with associativity technique. Here systolic architecture includes a number of Processing Elements (PE) that computes and transfers data. It is also called as Systolic array and it regularly pump the data in and out in the network.

Conventional FIR filter's critical path is

**Tc1 = Tmult+ 3Tadd**

The critical path of 4-tap FIR filter using Systolic and Associativity is given below,

**Tc2 = Tmult +Tadd**

Where, Tmult represents multiplier delay

Tadd represents adder delay. So, it is clear that proposed FIR filter's critical path is greatly reduced to (Tmult + Tadd), compared with normal FIR filter. Thereby, enhancement in speed of the filter can be achieved.

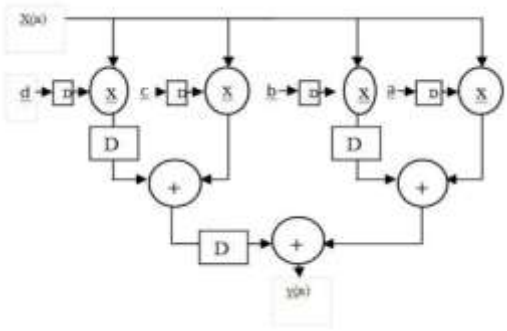


Figure 1: Proposed structure (Systolic with Associativity) for 4 tap FIR filter

DIRECT FORM: Direct-form structure provides a convenient method for FIR filters implementation. However, the direct-form implementation is not normally used in IIR filters due to problems with the design and operational stability of direct-form IIR filters.

There are M-1 delay blocks.

a) Input signal is delayed *M*-1 times and to store this delayed input signal *M*-1 memory locations are required.

b) Equation shows that present input $x(n)$ and past input are multiplied by corresponding sample of $h(n)$ hence output $y(n)$ is weighted linear combination of present input and past inputs.

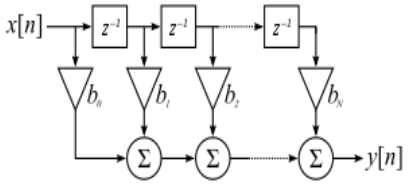


Figure 2: Direct form of N Tap FIR filter

TRANSPOSE FORM: In transpose structure, it is gotten from the immediate structure by a few controls of the filter structure: (I) Interchange information and yield, (ii) Reversal of sign flow diagram in bearing of bolt, (iii) Substitution of adders by a branch and the other way around. The primary favorable position of this structure is given by the twofold utilization of defer stages in light of the fact that the registers straightforwardly decouple the viper stages. No extra pipelining stages for the viper tree are required. The quantity of D-FFs increment since now items with m = j +1 bits are enrolled. The longest sign postpone way is with a multiplier (coefficient C0) and the last viper arrange which contains the longest wave convey chain with (m+log2(N +1)) bits [1].

The Transpose structure FIR channel just needs N postpone units, where N is the request for the channel – conceivably half as much as immediate structure. This structure is gotten by switching the request for the numerator and denominator segments of Direct Form, since they are in actuality two straight frameworks. At that point, one will see that there are two sections of postpones that tap off the middle net, and these can be consolidated since they are repetitive. The disservice is that Transpose structure expands the chance of number juggling flood for channels of high Q or reverberation. This is on the grounds that, adroitly, the sign is first gone through an all-post channel (which ordinarily helps gain at the resounding frequencies) before the consequence of that is soaked, at that point went through an every one of the zero channel (which regularly constricts a lot of what all-shaft half intensifies).

The transpose structure arrangement for FIR channel is talked about. The information stream diagrams (DFG) of transpose structure FIR channel for channel length N= 6 as demonstrated as follows.

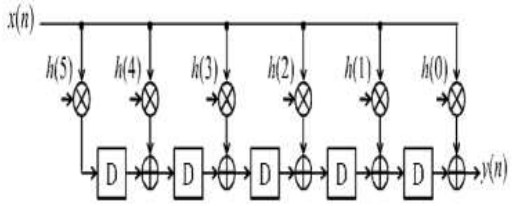


Figure 3: DFG of transpose form structure for N =6

SYSTOLIC FORM: Systolic clusters speak to a significant engineering worldview in VLSI signal handling usage because of the way that it very well may be utilized to effectively misuse the natural parallelism installed in DSP calculations by pipelining and equal preparing, However the deduction of new proficient systolic calculations is forever occupied with request to abuse the innate parallelism productively implanted in such calculations [5,6]. The method for information moving assumes a noteworthy job in the assurance of the effectiveness of a systolic calculation and its execution. This is one of the significance highlights played by cyclic convolution in computerized signal preparing. Cyclic convolution gives high registering speed, low computational intricacy and I/O cost. In addition, it tends to be productively actualized through systolic exhibits.

SYSTOLIC ARCHITECTURE: A systolic exhibit is made out of network like lines of Data Processing Units (DPUs) called cells. DPUs are like Central Processing Units (CPUs), with the exception of the typical absence of a program counter, since activity is transport-activated, implies by the appearance of an information object. In the wake of preparing every phone imparts the data to its neighbors right away.

ISSN: 2005-4238 IJAST

The systolic exhibit is frequently rectangular for the information which streams over the cluster between neighbor DPUs, regularly with various information streaming in various ways.

The information streams entering and leaving the ports of the cluster are created via Auto Sequencing Memory (ASM) units. Each ASM incorporates an information counter. In implanted frameworks an information stream may likewise be contribution from and yield to an outer source. A case of a systolic calculation is intended for grid increase. One framework is taken care of in succession at once from the highest point of the cluster and is passed down the exhibit; the other network is taken care of in a section at once from the left-hand side and goes from left to right of an exhibit. Until every processor has seen the one entire line and one entire segment the fake factors are passed. Now the aftereffect of the increase is put away in the cluster and can now the yield be a line or a segment at once, streaming down or over the exhibit.

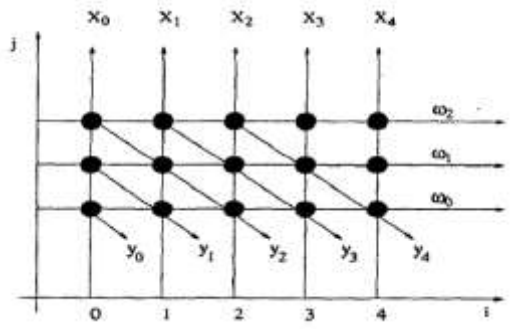


Figure 5: Dependence graph (DG) of FIR

FOLDING ARCHITETURE: An ordered set of operations executes by same functional unit. The folding set are typically obtained from a scheduling and allocation algorithm. The folding set represents underlying folding transformation.

Collapsing changes an activity from a unit-time to N unit-times handling where N is called collapsing factor. In this way, in changed framework various same tasks (not as much as N) utilized in unique framework could be supplanted with a sign activity obstruct in changed framework. Therefore, in unique framework N unit-times, in changed framework the utilitarian squares could be reused so as to perform N activities.

The collapsing change decreases the quantity of practical units in the design; since it needs more memory component to store the transitory information. It is on the grounds that that different information created from an activity square should be recognized from N information delivered from unique tasks. In this way, the quantity of registers might be expanded and it needs extra multiplexer for exchanging diverse activity ways.


Figure 4: Corresponding folded edge

## 3. RESULTS

The FIR filter is designed using HDL language for the direct, transpose, systolic and folded form for 13 tap. The designed FIR filter functionality is verified in Modelsim and the utilization of parameters is verified under Xilinx ISE tool.

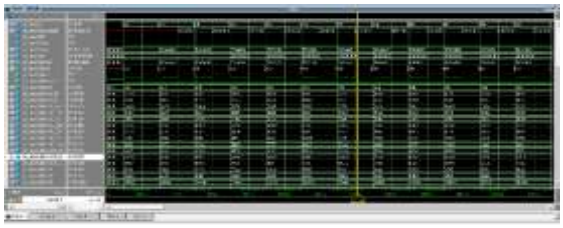

Figure 6 : Direct form FIR filter for 13 tap

From the Figure 6, the 13 tap FIR filter for the direct method is designed and simulated using HDL language. The output of Conventional 13 tap FIR filter is 1baee0 for the given 13 inputs.

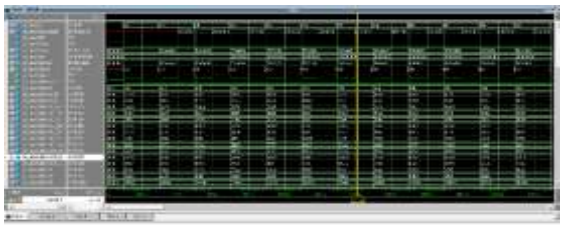

Figure 7: Transpose form for 13 tap FIR filter

From the Figure 7, the 13 tap FIR filter for the direct method is designed and simulated using HDL language. The output of Conventional 13-tap FIR filter is 1baee0 for the given 13 inputs.

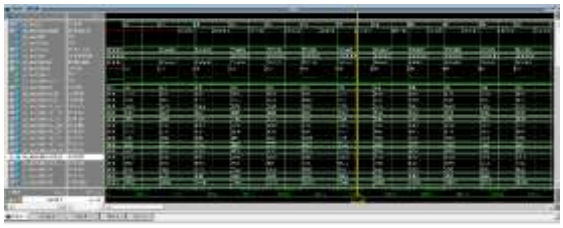

Figure 8: Systolic form for 13 tap FIR filter

From the Figure 8, the 13 tap FIR filter for the systolic method is designed and simulated using HDL language. The output of Conventional 13-tap FIR filter is 1baee0 for the given 13 inputs.

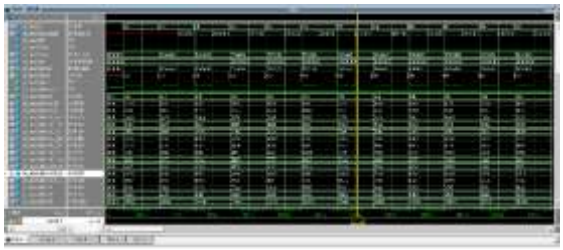

Figure 9: Folded form for 13 tap FIR filter

From the figure 9, the 13 tap FIR filter for folded method is designed and simulated using HDL language. The output of conventional 13 tap FIR filter is 1 baeee0 for the given 13 inputs.

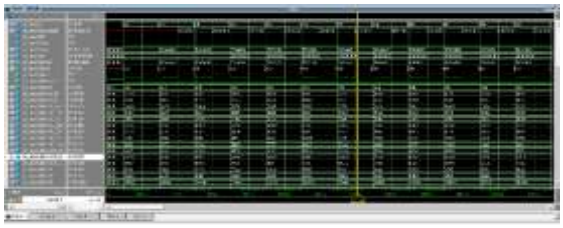

Figure 10: 13 tap FIR filter using systolic with associativity

From the figure 10, the 13 tap FIR filter for the systolic method with associativity is designed and simulated using HDL language. The outputs of conventional 13 tap FIR filter is 1baeee0 for the given 13 inputs.

**Table: Performance analysis of 13 tap FIR filter for different structure**

| Type of the Architecture/Parameter | Area | | Delay(ns) |
|---|---|---|---|
| | Slices | LUT | |
| **Direct Form** | 74 | 130 | 15.389 |
| **Transpose Form** | 72 | 126 | 14.091 |
| **Systolic Form** | 79 | 142 | 11.326 |
| **Folded Architecture** | 61 | 112 | **11.932** |
| **Associativity** | 58 | **105** | 15.389 |
| **Proposed Structure (Systolic with Associativity)** | 59 | 108 | 11.310 |

In the table, the LUT consumed by the proposed architecture is 16.92% less than the direct form structure and the delay obtained by the proposed architecture is 26.5% less than the direct form structure for 13-tap FIR filter.

## 4. CONCLUSION

The different architectural transformation is applied in FIR filter. The different transformation like Transpose form, Systolic architecture and Folding architecture is applied in the FIR filter. The functionality for the different structure is verified using modelsim and the parameter optimization is verified in XILINX ISE. The 8-tap and 13-tap FIR filter is designed under different architecture is verified and simulated and the parameter utilization is obtained. For 8-tap FIR filter the LUT consumed by the folded architecture is 27% less than the direct form structure and the delay obtained by the systolic architecture is 60.46% less than the direct form structure for 8-tap FIR filter. For 13-tap FIR filter the LUT consumed by the folded architecture is 43% less than the direct form structure and the delay obtained by the systolic architecture is 26.46% less than the direct form structure for 13-tap FIR filter. From the results the Folded architecture consumed less number of LUT while comparing to the other structures, so folded architecture can be used for the LUT optimization in different application and the systolic architecture consumes less delay than the other structures, so systolic architecture can be used for the delay optimization in different applications. In future the combined architecture of folded, transpose and systolic architecture can be designed to develop a optimized FIR filter in different applications.

## 5. REFERENCES

1. Lou X, Yu YJ, Meher PK. Fine-grained critical path analysis and optimization for area-time efficient realization of multiple constant multiplications. IEEE Transactions Circuits Systems. 2015 Mar; 62(3):863–72.
2. Ye WB, Yu YJ. Bit-level multiplier less FIR filter optimization incorporating sparse filter technique. IEEE Transactions Circuits Systems. 2014 Nov; 61(11):3206–15.

3. Peiro MM, Boemo EI, Wanhammar L. Design of highspeed multiplier less filters using a non-recursive signed common sub expression algorithm. IEEE Transactions Circuits Systems. 2002 Mar; 49(3):196–203.
4. Faust M, Kumm M, Chang CH, Zipf P. Efficient structural adder pipelining in transposed form FIR filters. IEEE International Conference on Digital Signal Processing (DSP); 2015. p. 740–3.

ISSN: 2005-4238 IJAST