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Realization of Analog circuits in Near Field Communication Process for better throughput Performance

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Abstract

In this paper a better throughput in Near Field Communication (NFC) is achieved using advanced modulation technique such as Ternary Quadrature Amplitude Modulation(TQAM) in 250nm CMOS process. Using Electromagnetic induction concepts, NFC makes a wireless communication with transmitter and receiver protocols. In this proposed work, transistor circuits for Transmitter and Receiver modules of NFC are designed using TQAM concepts. TQAM is highly efficient compared to other modulation techniques like ASK, PSK, QAM. TQAM utilizes both amplitude and phase variations. The Main reason to use the TQAM is to increase the data rate in the communication process. The Transmitter and receiver module are integrated in analog domain and synthesized using the Tanner tool software environment

Keywords: *NFC, Ternary logic, Transmitter, Receiver, Tanner Tool*

1. Introduction

NFC stands for "Near Field Communication". It enables short range communication between active and a passive device operates at a frequency of 13.56MHz. NFC devices are used in contactless payment systems. It is also used in social networking such as sharing videos, photos and contacts. Passive devices such as tags that transfer information to other NFC devices and do not require power supply of their own. They don't process any information that it was received by other devices and not able to connect to other passive devices. Active devices are capable of both transmit and receive the data and can communicate with each other. The communication between active and passive devices is established within only 4cm. Compared to other wireless technologies NFC doesn't require power and it is the big advantage. In the available NFC technology, digital modulation techniques like ASK with Manchester coding are used. In most of the cases a level of 10% modulation is used, with a Manchester coding format. In NFC, the supported data rates are 106 kbps to 424 kbps. Comparing to other modulation techniques ASK has poor noise immunity. The highly efficient NFC transmitter is designed and implemented using 0.18µm CMOS process. The ASK modulated output is generated by pulse width modulation (PWM) technique. The proposed NFC transmitter can provide 0-100% modulation depth [1]. The ASK demodulator circuit is designed by sample and hold method. The proposed ASK demodulator composed of switch capacitor filter, clock extractor, envelope detector, dynamic comparator and phase generator and it is implemented in TMSC 0.18µm CMOS technology[2].

The low power and area efficient passive tag used for medical application. In order to get high power conversion efficiency, the CMOS gate cross coupled rectifier with diode is used. The ASK demodulator has comparator circuit to detect the threshold levels.
The ISO/IEC 18092 standard uses 10%ASK modulation depth in NFC having the data rate from 106 to 824 Kbps[3]. In the existing technology, for ticketing and data exchange the NFC enabled smart phones either in peer to peer mode or card emulation mode. But in practical situation the manufacturer overcome obstacles such as interoperability and realization [4]. The NFC supporting data rate ranges from 106 to 848 Kbps and modulation depth varies from 8 to 100%. The proposed work is processed on 45nm CMOS

technology. The modulation techniques used are Manchester, NRZ and modified miller coding [5].TQAM is highly efficient and the data rate is improved by increasing the number of levels. By applying TQAM in NFC throughput is improved from 106Kbps to 8.46Mbps.Fig 1 shows the complete NFC block diagram.

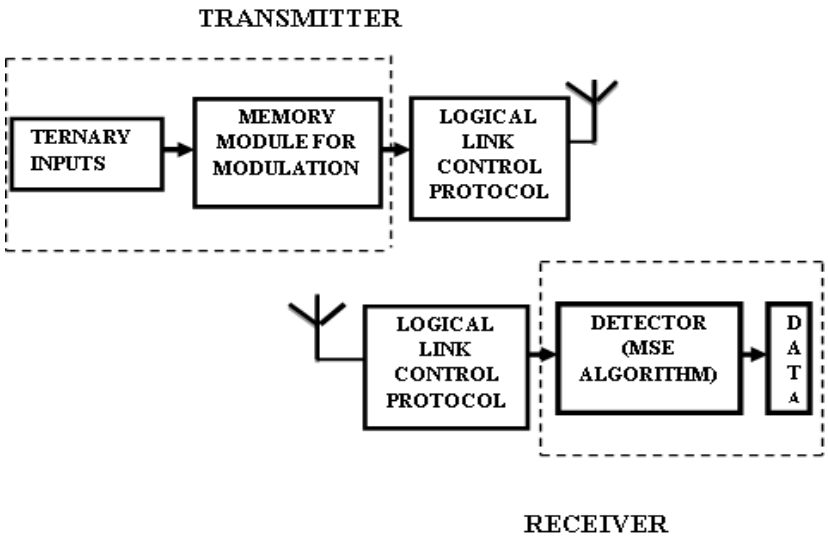

Fig 1. Block diagram for NFC

2. Proposed Methodology

Ternary Quadrature Amplitude Modulation technique is used in Near Field Communication. For ternary we have three states -1, 0, 1. Therefore 3^n combinations are possible, where n represents number of trit.

A. Transmitter Module

Fig 2 shows the transmitter module consists of de-multiplexer, 2 to 9 decoder and Read Only Memory. The data to be transmitted is given to the 1:4 de-multiplexer block. The output of the de-multiplexer block acts as a select lines for 2 to 9 decoder. For selecting any one of the row in ROM architecture decoder output is used. Finally TQAM modulated bits are transmitted.

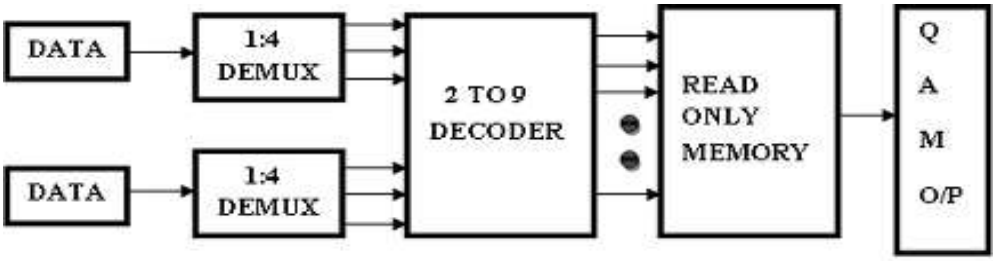

Fig 2. Block diagram for Transmitter

B. Ternary De-multiplexer

A De-multiplexer is also called as a data distributor.1:4 de-multiplexer has a single input line and routes to any one of the several output lines. A de-multiplexer has 2^n output lines where n represents the number of select lines. In De-multiplexer, depending upon the select lines A and B corresponding output will be

selected. The input to the 2to9 decoder is the output obtained from the de-multiplexer. Fig 3 shows the de-multiplexer. Whenever the select lines "A=B=0" means Y1 will be selected. If "A=0 and B=1" then Y2 will select. If "A=B=1" then Y3 will selected. There are four outputs from the de-multiplexer out of which we have used only three outputs. The select lines for first de-multiplexer are A and B and for second de-multiplexer C and D.

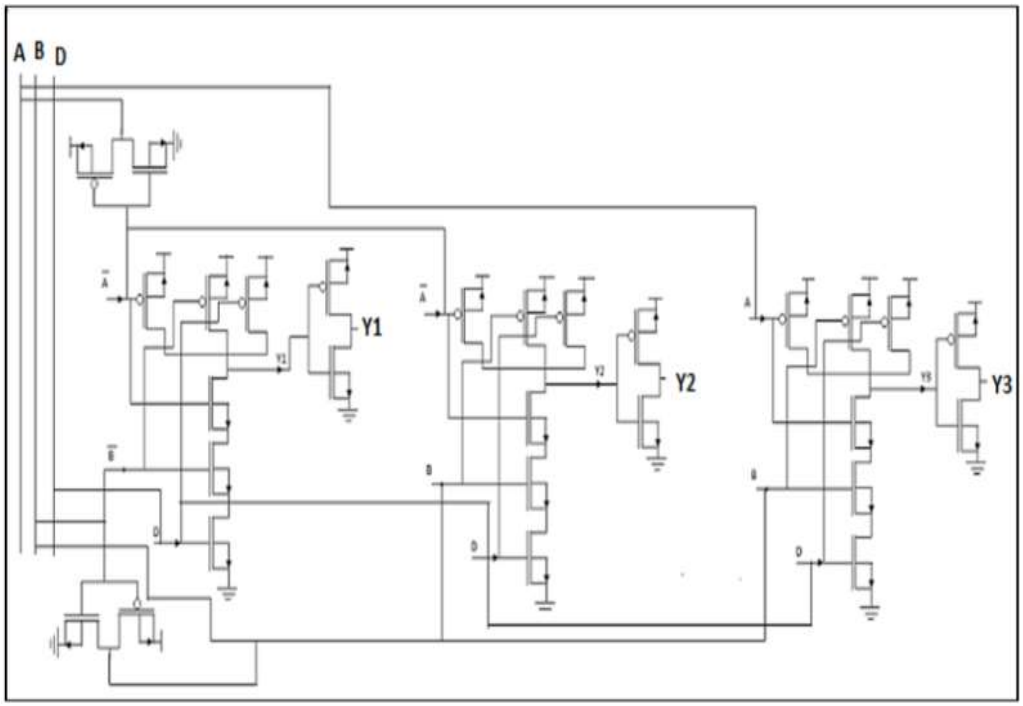

Fig 3. Transistor level diagram for 1:4Ternary De-multiplexer (BLOCK H)

De-multiplexer consists of two inverters, four 3input AND gates and data with two select lines. The three input AND gate is constructed with help of PMOS and NMOS. Since, it is a three input AND gate, three PMOS and NMOS transistors have used. Fig 3 shows the transistor level diagram for 2to9 Decoder.
The concept of de-multiplexer is that for a particular control signals, the corresponding output will be selected which is same as that of the data that given as an input. If "$\bar{A}$=$\bar{B}$=1", the PMOS will turn on and NMOS will turn off (because the source of the NMOS is driven to the ground) in the first three input AND gate.

C. 2 to 9 ternary decoders

The output of the ternary de-multiplexer is given as input to the decoder. As shown in Fig 4, the 2:9 Decoder consists of 2 inputs and 9 outputs. D1, D2 are the inputs and R1to R9are the outputs. PMOS are connected to the power supply (Vdd=5V). There are four select lines namely S0, S1, S2 and S3. So totally there are nine input combinations and nine outputs.
The select lines given to first de-multiplexer are S0 and S1, and the corresponding select lines are activated, a particular output will be obtained and it is same as that of the data. R1, T1 and W1 are the outputs obtained from first de-multiplexer and R2, T2 and W2 are from second de-multiplexer.

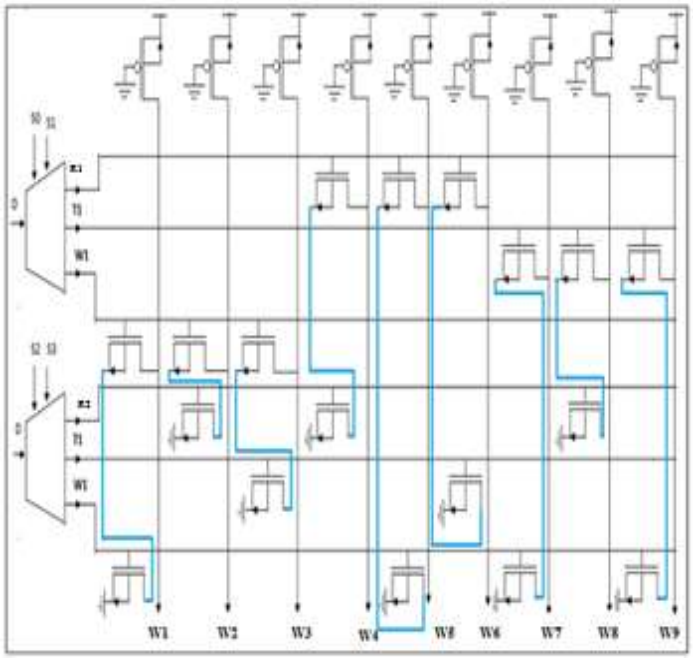

Fig4. Diagram for 2to9 Decoder

For example, when the control signals "S0=S1=S2=S3=1", the output W1and W2 from the first and second demultiplexer will be selected respectively as shown in Table 1. The output W1 and W2 gives as an input to the gate terminal of NMOS which is connected with the first PMOS`s drain terminal. Finally, the first row R1 will be selected.

For the remaining combinations also the particular rows will be selected as shown in Table 1.

I. Logic Table for 2to9 Decoder

Select Lines				Outputs
S0	S1	S2	S3	
1	1	1	1	W1
1	1	0	0	W2
1	1	0	1	W3
0	0	1	1	W4
0	0	0	0	W5
0	0	0	1	W6
0	1	1	1	W7
0	1	0	0	W8
0	1	0	1	W9

D. Nine-Quadrature Amplitude Modulation

For ternary QAM there are 3^n Output combinations are possible. Here n=2, therefore $3^2 = 9$ combinations are possible. The Energy per bit to the spectral noise density (E_b/N_0) for 9QAM is 4.963.

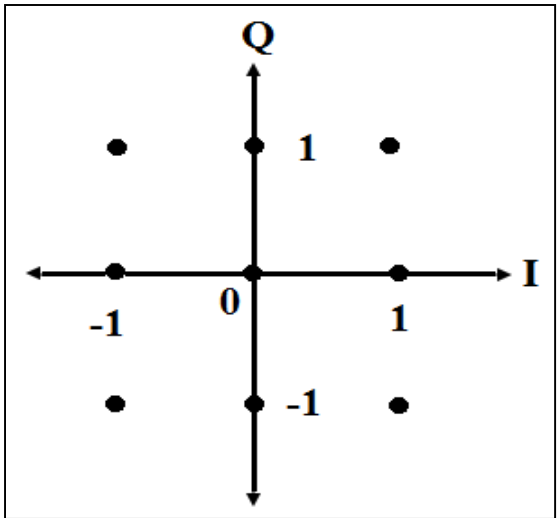

Fig 5. Nine QAM Square Constellation Diagram

For Nine Quadrature Amplitude Modulation the constellation points are shown in Fig 5. We are representing the In-phase component in x-axis and Quadrature phase component in y-axis. Since it is ternary we have three states 0, 1 and -1. The In-phase and Quadrature phase have measured for each constellation points as shown in Table 2.

II. 9 QAM Table for In-Phase and Quadrature Phase Component

Inputs	In-Phase	Quadrature
-1 -1	0	0
-1 0	0	1/√4.963
-1 1	1/√4.963	1/√4.963
0 -1	1/√4.963	0
0 0	1/√4.963	-1/√4.963
0 1	0	-1/√4.963
1 -1	-1/√4.963	-1/√4.963
1 0	-1/√4.963	0
1 1	-1/√4.963	1/√4.963

The In-phase and Quadrature phase components are measured and it is expressed in terms of binary values are shown in Table 3.

III. Logic table for 9QAM

Inputs		In-Phase	Quadrature
-1	-1	0000	0000
-1	0	0000	0011
-1	1	0011	0011
0	-1	0011	0000
0	0	0011	1011
0	1	0000	1011
1	-1	1011	1011

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1	0	1011	0000
1	1	1011	0011

E. Memory Module

For selecting the particular row in the Read Only Memory Architecture one among the nine decoder outputs are used. If W1 from the decoder is selected, the first row in ROM structure will be selected and the corresponding output will be shown. For the remaining combinations also the particular rows will be selected. The In-phase components are stored in the R1,R2,R3,R4and Quadrature phase components are stored in the R5,R6,R7,R8.

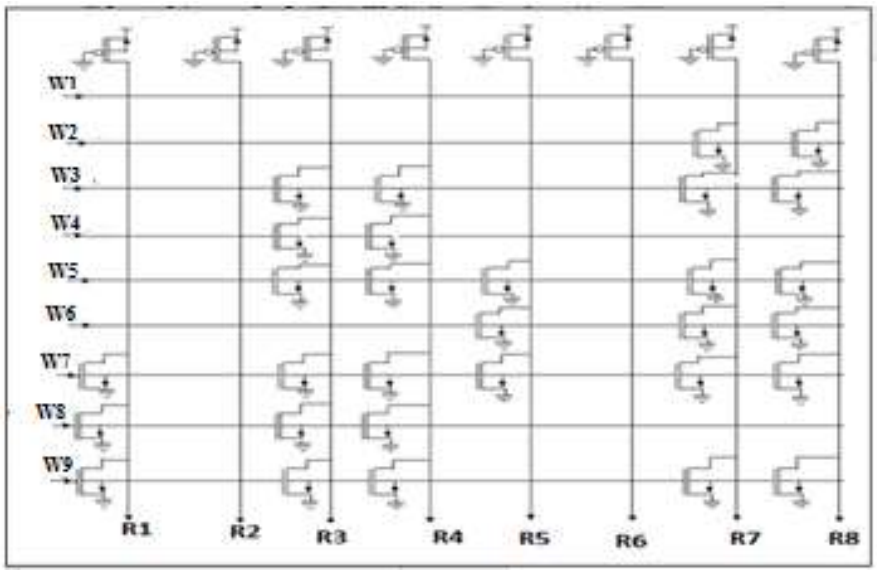

Fig 6. Memory module for 9 QAM

As shown in Fig 6, the inputs to the ROM architecture are R1to R9 which are the outputs obtained from the ternary decoder structure. The inphase and quadrature phase components are calculated by using the scaling factor. For the calculated decimal values corresponding binary values have been found and stored in the ROM architecture. The ROM structure consists of 9 rows and 8 columns.

The outputs obtained from the structure are R1 to R9. Since it is a 9-QAM, nine levels have used. R1 represents the first level similarly up to nine levels.

The NMOS transistor represents the bit that has been stored. The NMOS transistor is placed in order to store the bit 1. When the W1 is selected from decoder, the first level in the ROM architecture is selected. When W1 is given as an input to the first level, since no NMOS transistor is presented, the supply (Vdd=5V) given to the source of the PMOS is obtained as an output in each column as one.

All the sub block viz. Ternary demultiplexer, Ternary decoder, ROM structure of the transmitter are integrated. The two ternary de-multiplexers are used with two inputs and four control lines. The corresponding row in memory architecture will be selected based on the control lines enabled from the de-multiplexer. Fig 7 shows the whole transmitter integrated diagram.

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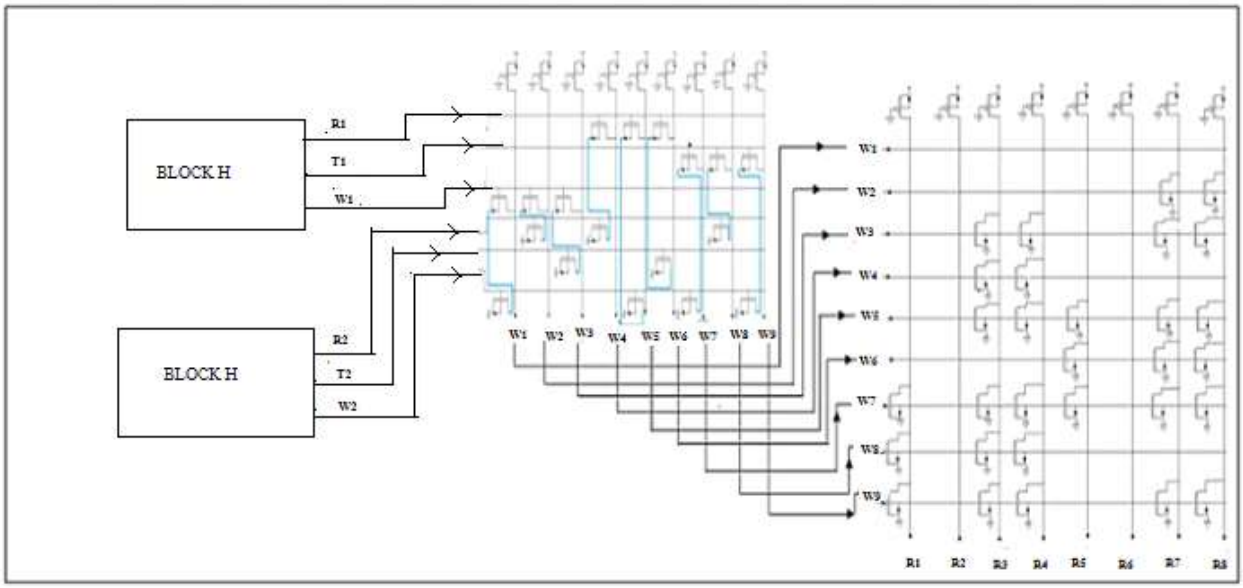

Fig 7. Integrated Transmitter Block

3. Calculation of data rate

The expression for calculating the Data Rate is given as follows,

$DataRate = 2 \times Blog_2[N]$ … (1)

where B represents the Bandwidth and N is number of levels.

In NFC, the Upper cutoff frequency(UF) and Lower cutoff frequency(LF) are 14.0475MHZ, 12.7125MHZ. Therefore, the bandwidth is calculated as upper cutoff frequency minus lower cutoff frequency (i.e. 14.0475MHz - 12.7125MHz =1.335MHz). The Bandwidth for NFC operation is 1.335MHz. The expression for $log_2(N)$ is given as follows,

$log_2(N) = 3.32\ log_{10}[N]$ … (2)

For ASK:

Data Rate =$2\times1.335\times10^6\times3.32\text{Log}_{10}[2]$ … (3)

Data Rate =264Kbps.

For Binary QAM:

Data Rate =$2\times1.335\times10^6\times3.32\text{Log}_{10}$ [4] … (4)

Data Rate = 5.34Mbps.

For Ternary QAM:

Compared to ASK and binary QAM, Ternary QAM has better data rate given by the expression(5)

Data Rate =$2\times1.335\times10^6\times3.32\text{Log}_{10}$ [9] … (5)

Data Rate =8.46Mbps.

4. Demodulation

The mean squared error (MSE) or mean squared deviation (MSD) estimates the average of the squares of the errors-that is the average squared differences between the estimated values and what has to be estimated.

$MSE = \frac{1}{n}\sum_{i=1}^{n}(y_i - \hat{y}_i)^2$ … (6)

Where, y_i= real data transmitted

$\hat{y}_i$is the obtained data and n is the no. of data points.

A. Receiver module

The receiver part is modelled by using mean square error algorithm. Fig 8 shows the general block of receiver. The receiver part is made up of Subtractor, Multiplier, full adder and divider are used to perform MSE algorithm for the first two levels of in-phase component and it is also for quadrature phase component.

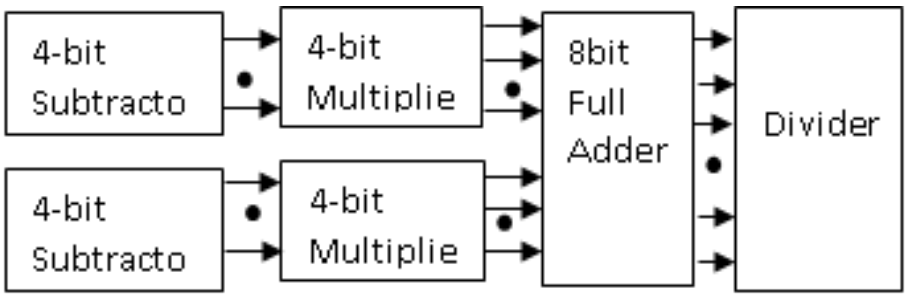

Fig8. General block diagram of receiver

Fig 9 shows the design of Full Subtractor. A, B, and Cin are the inputs to the full adder. The first full adder output is given as input to the next full adder and it continuously goes on. It occurs for the remaining full adder also. S0, S1, S2, S3 and Cout are the outputs respectively. The inputs area0, a1, a2, a3 and b0, b1, b2 and b3 and the outputs are Z0, Z1, Z2, Z3, Z4, Z5, Z6 and carry. The multiplier can also be viewed as a squarer.

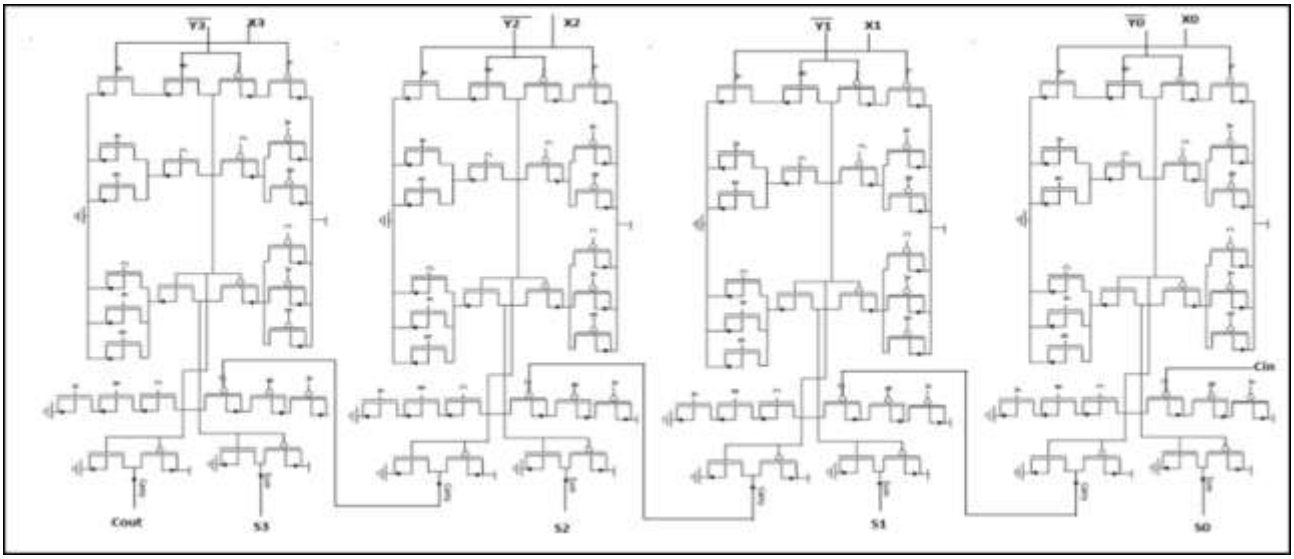

Fig 9. 4-Bit Full Subtractor(BLOCK G)

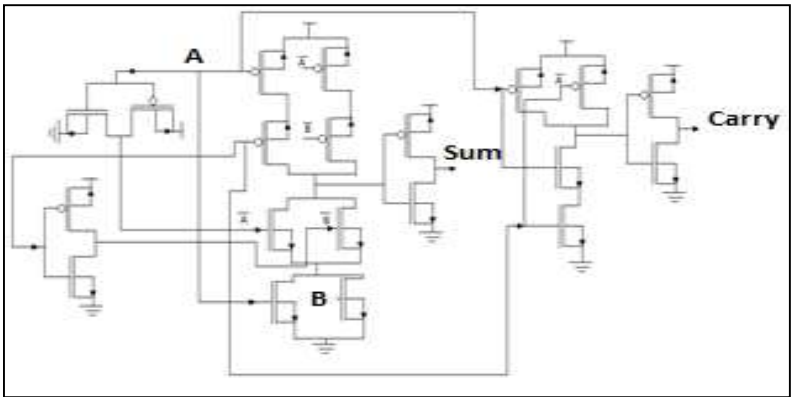

Fig10. Half Adder (BLOCK A)

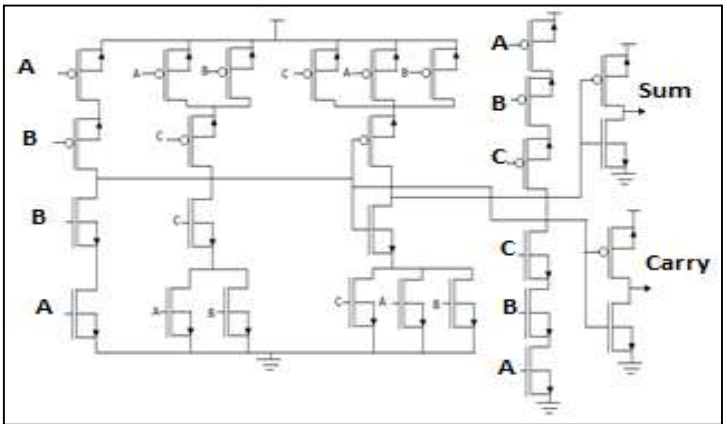

Fig11. Full Adder (BLOCK B)

Fig 10 and Fig 11shows the implementation of half adders (BLOCK A)and full adders(BLOCK B). The output of the Multiplier (BLOCK D) are a0b0, a1b0, a2b0, a3b0, a0b1, a1b1, a2b1, a3b1, a0b2, a1b2, a2b2, a3b2, a0b3, a1b3, a2b3 and a3b3.The first 4-Bit multiplier is shown in Fig 12. The output from the multipliers are added using 8 Bit binary adder(BLOCK E)as shown in Fig 13.For 9QAM we have nine levels. The above is stated for only one level and it is done for remaining eight levels also. The above procedure is repeated for quadrature phase component also. For performing division operation, shift register has used.

All the nine levels are summed up and average has been taken by using Serial in Serial Out shift right registers as shown in Fig 14. The divider (Mean)block (BLOCK F)is implement for two levels. It has to be implemented for nine levels. The result obtained from the full adder i.e. after the summation of all levels, shift right is enabled in order to execute division. Since, the output obtained from the summation of nine levels are in eight bits. It consists of eight delay flip-flops. So, single right shift is enough to obtain the data and the Shift right register is designed by using Delay flip flop. As shown in Fig 15 the receiver diagram was implemented by full subtractor, multiplier, eight-bit adder and divider which are designed by using PMOS and NMOS transistors. In order to obtain the data accurately Mean Square Error algorithm have used.

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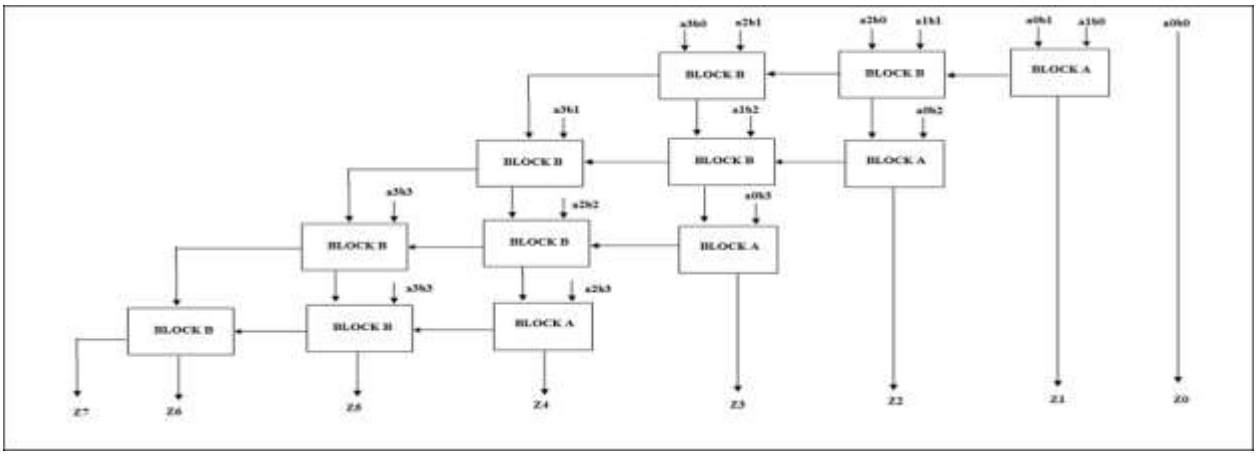

Fig 12. 4-Bit Multiplier(BLOCK D)

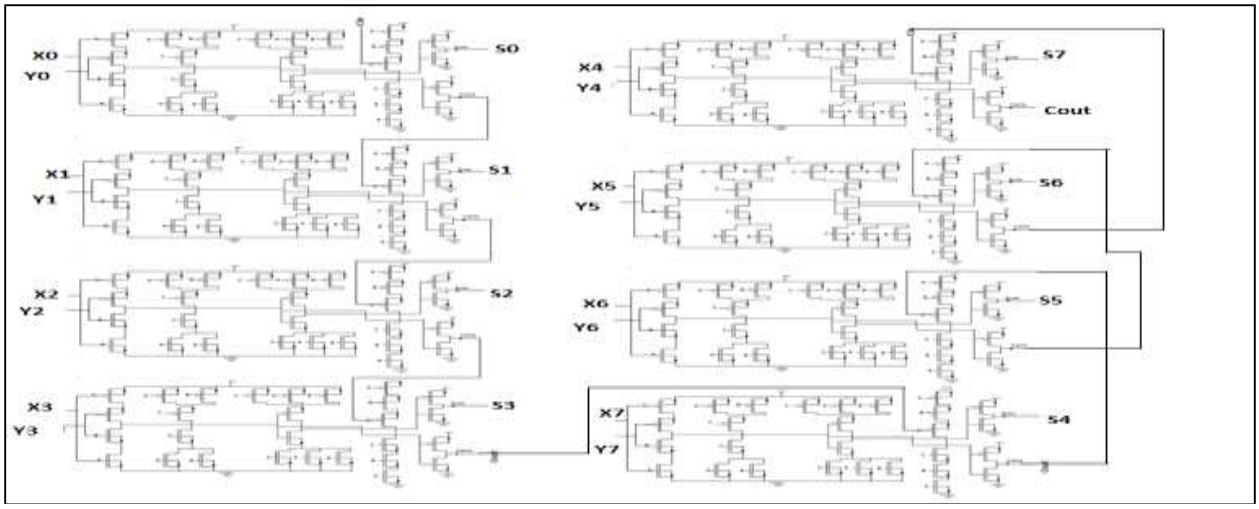

Fig 13. Transistor level diagram for8-Bit adder (BLOCK E)

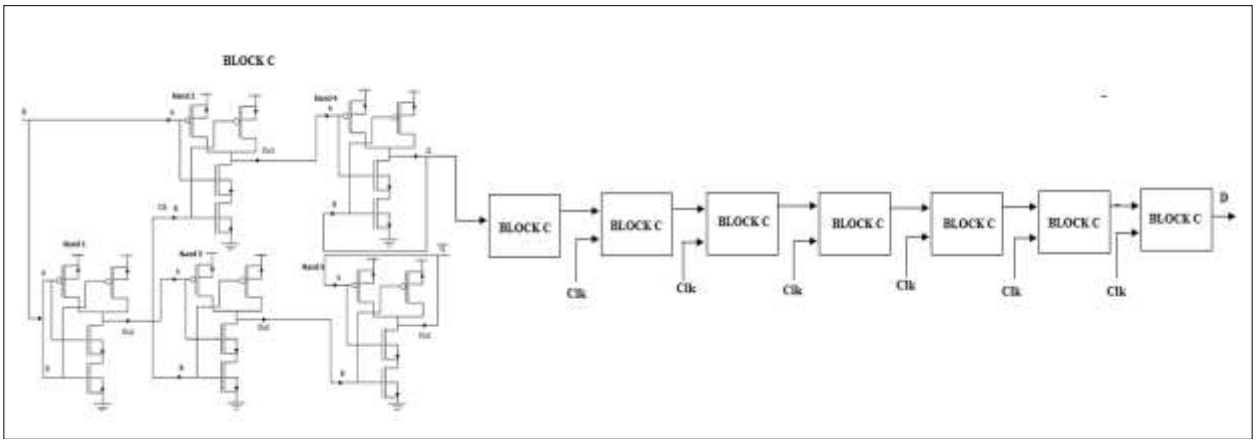

Fig 14. Transistor level diagram for Divider (BLOCK F)

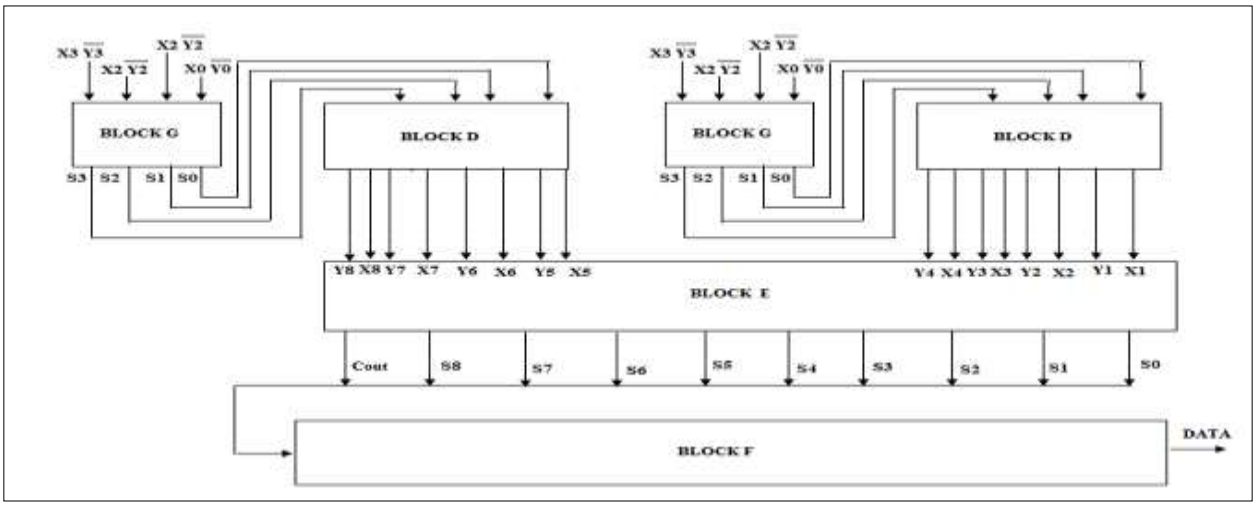

Fig 15.Integrated Receiver Block

5. Results and discussion

A. Transmitter module

The 2 to 9 Decoder is designed by using18 NMOS and 9 PMOS as shown in Fig 16.The input of the decoder is obtained by the de-multiplexer output. The decoder consists of 2 inputs and 9outputs that are represented by Out1to Out9. The number of 1:4 de-multiplexer have used is two. The control signals areA1, B1, A2, B2. Out1 to Out9 are the Outputs. For example"A1=B1=0;A2=B2=1", the output 9 will be selected as shown in Fig 17.The schematic for Ternary QAM is implemented by using ROM architecture with nine rows and eight columns analysis. As shown in Fig 18 the inputs to the architecture are Out1to Out9 and outputs are R1to R8. When Out1 is enabled in the decoder and given as an input to the first row among the nine levels. In eight columns the in-phase and quadrature phase values are stored and it will be obtained through the corresponding outputs R1to R8.

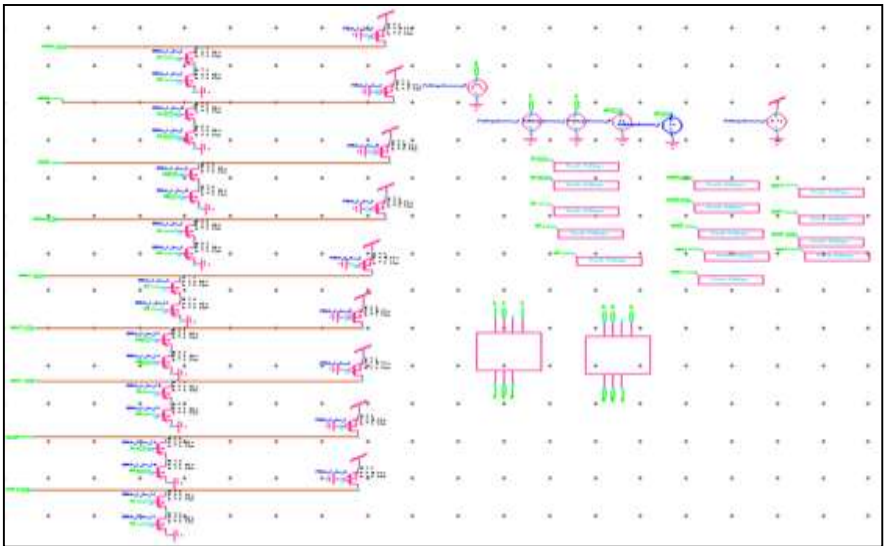

Fig 16. Schematic of 2 to 9 Decoder

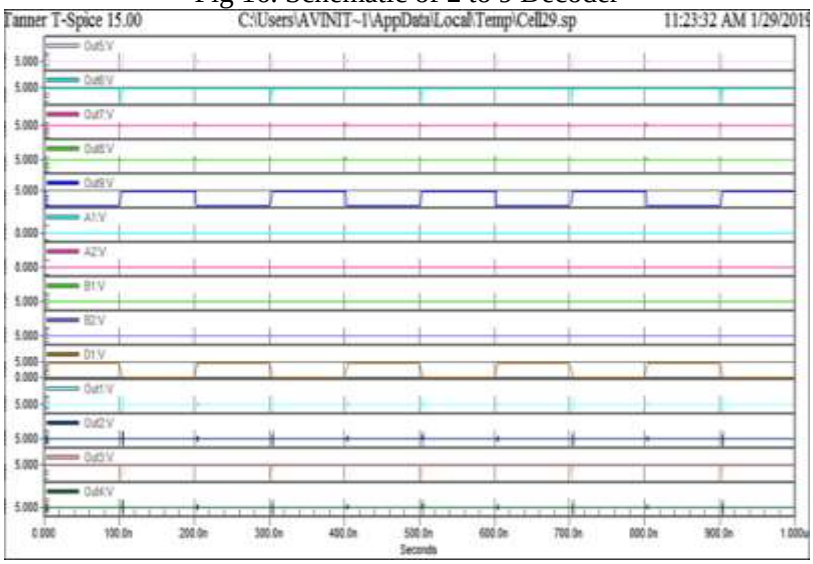

Fig 17. Simulation of 2 to 9 Decoder

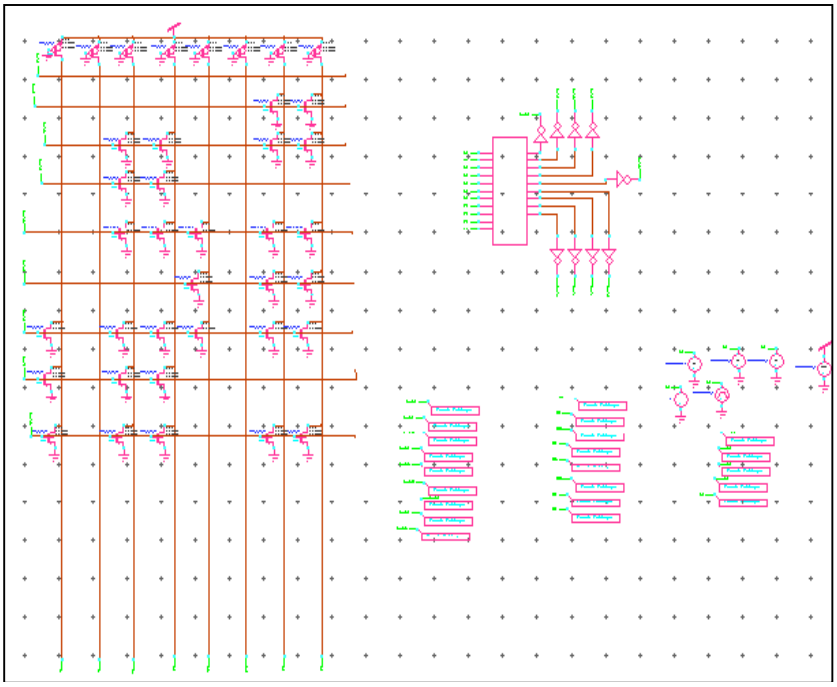

Fig 18. Schematic of Memory Structure

The ROM Architecture is shown in Fig 18.For example"A1=A2=0" and "B1=B2=1", fourth output will be selected. The fourth output of the decoder activates corresponding therow in the memory architecture and the outputs are represented as R1to R8 as shown in Fig 19.

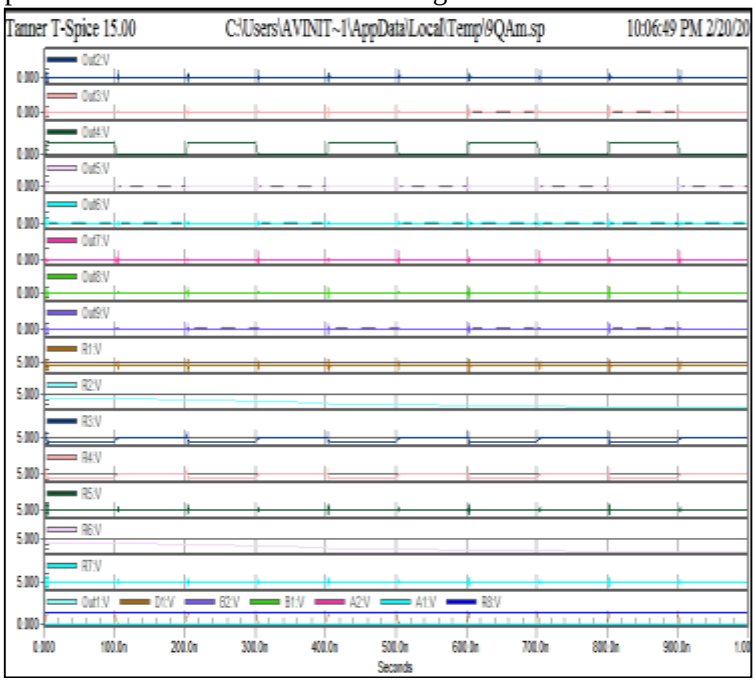

Fig 19. Simulation of ROM Architecture

B. Receiver module

The receiver module consists of the following schematics they are fullsubtractor, multiplier, full adder and divider. Full subtractor is used to take difference between the original bits and received bits.

Multiplier is used as squarer. Full adder is used for the summation of levels. Shift Right register (SISO) is used as a divider to calculate the mean. Fig 20 shows the schematic for full subtractor is implemented using full adder constructed with PMOS and NMOS transistors. Here the bits Y0, Y1, Y2 and Y3 represent the received bits and X0, X1, X2 and X3 represents the original bits transmitted.

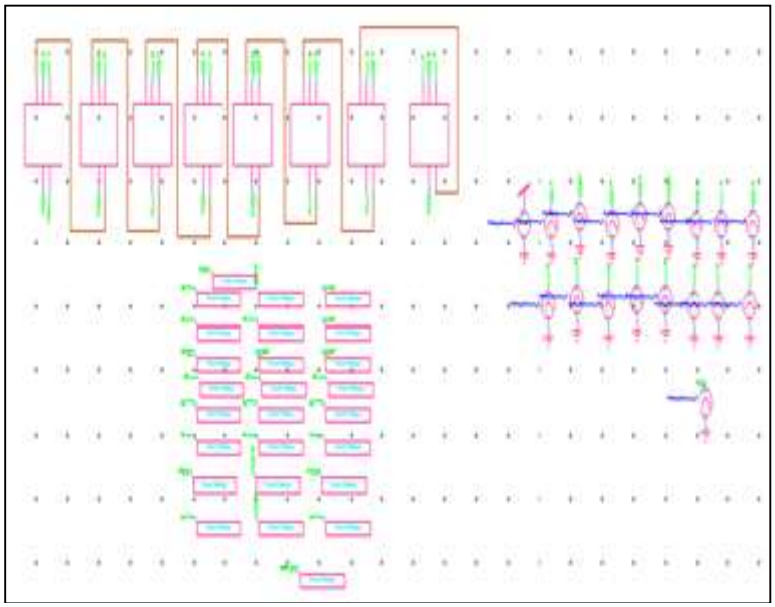

Fig 20. Schematic of Subtractor

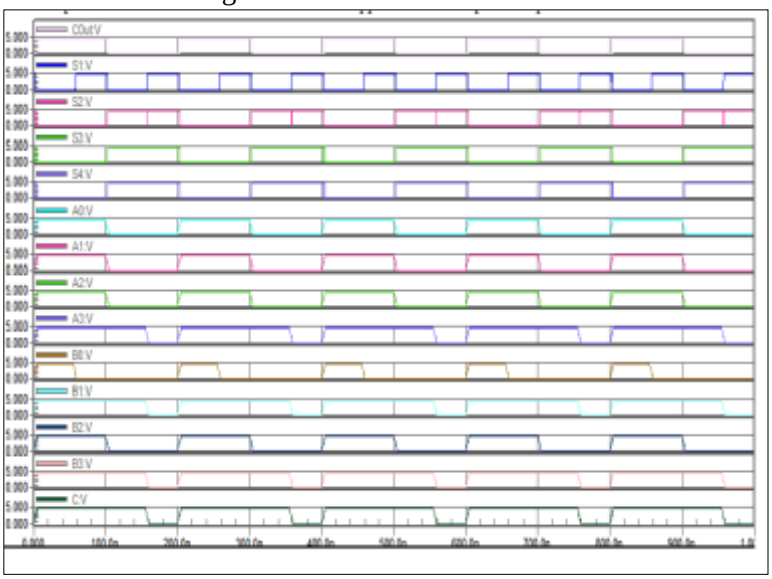

Fig 21. Simulation of Subtractor

As shown in Fig 21, A0, A1, A2, A3 are minuend and B0, B1, B2, B3 are subtrahend.The inputs are "A1=1, A2=1, A3=1, A4=1 and B1=0, B2=1, B3=1, B4=1".The results obtained are "S1=1, S2=0, S3=0 and S4=0". Fig 22 shows the inputs to the subtractor are A0, A1, A2 and A3. It is an implementation of 4-bit multiplier design which acts as a squarer. The results obtained from multiplier are in eight bits which are Z0 to Z7 and carry output obtained from the last full adder.The partial products obtained from AND logic and are added by using adders. Each stage consists of one-half adder and two full adders. The inputs areU0,U1,U2,U3and V0,V1,V2,V3.For example the inputs given are "U0=1,U1=1,U2=1,U3=1" and

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"V0=1,V1=1,V2=1,V3=1". The obtained results are "Z0=1,Z1=0,Z2=0,Z3=0,Z4=0,Z5=1,Z6=1 and z7=1" by performing multiplication of the U and V as shown in Fig 23.The 8-bit adder is used to perform addition operation obtained two multipliers. The inputs for first multiplier are A0, A1, A2, A3 and B0, B1, B2,B3. The inputs for second multiplier are A4, A5, A6, A7 and B4, B5, B6, B7.

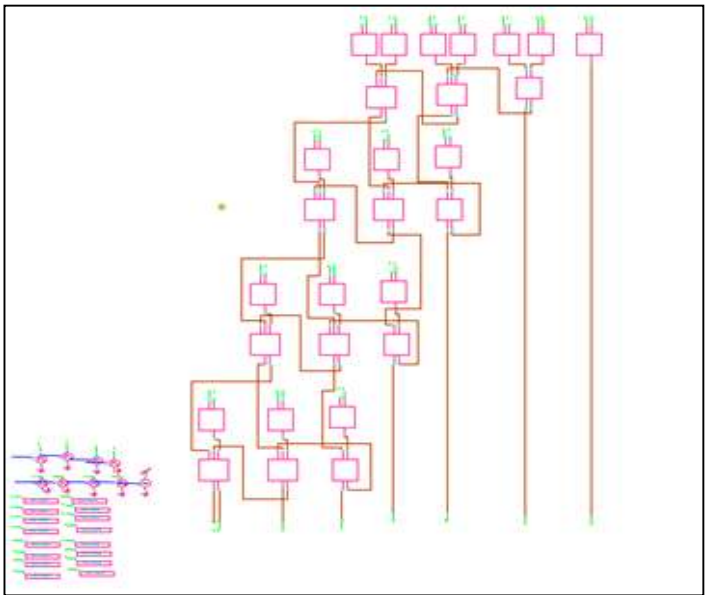

Fig 22. Schematic of Multiplier

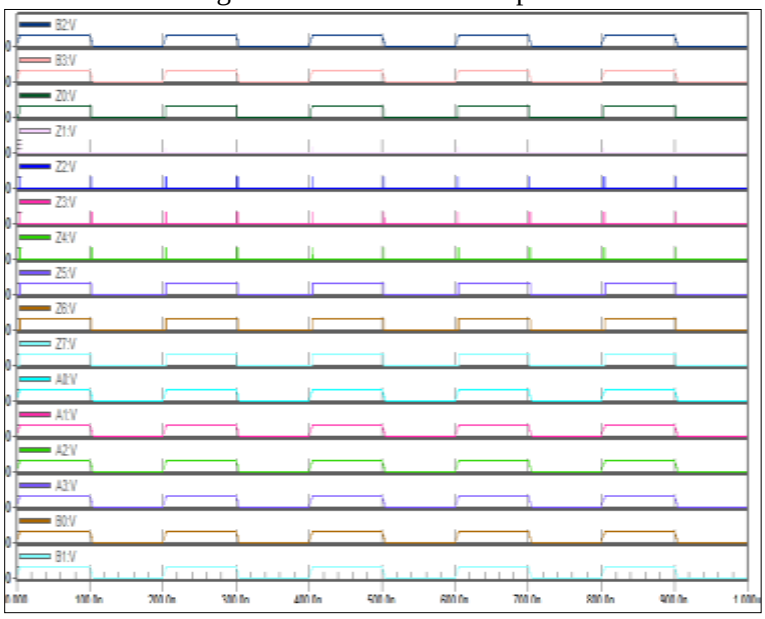

Fig 23. Simulation of Multiplier

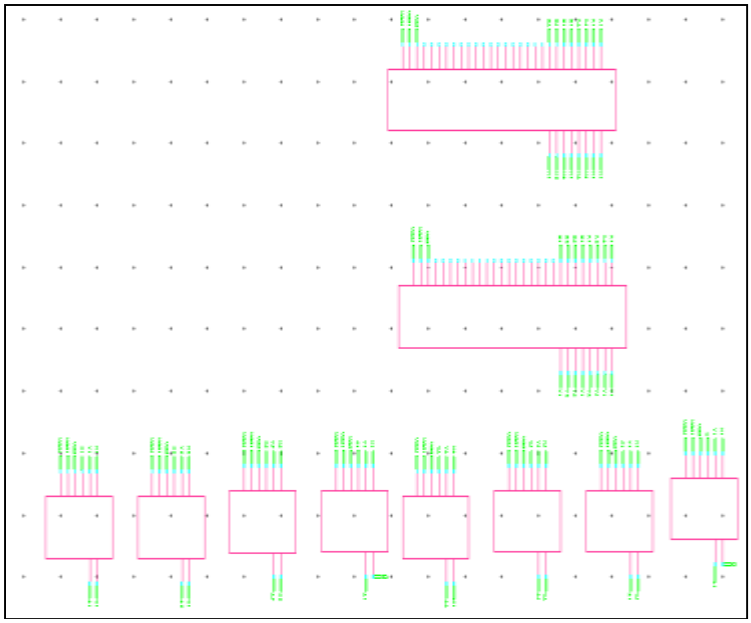

Fig 24. Schematic of Multiplier and Addition

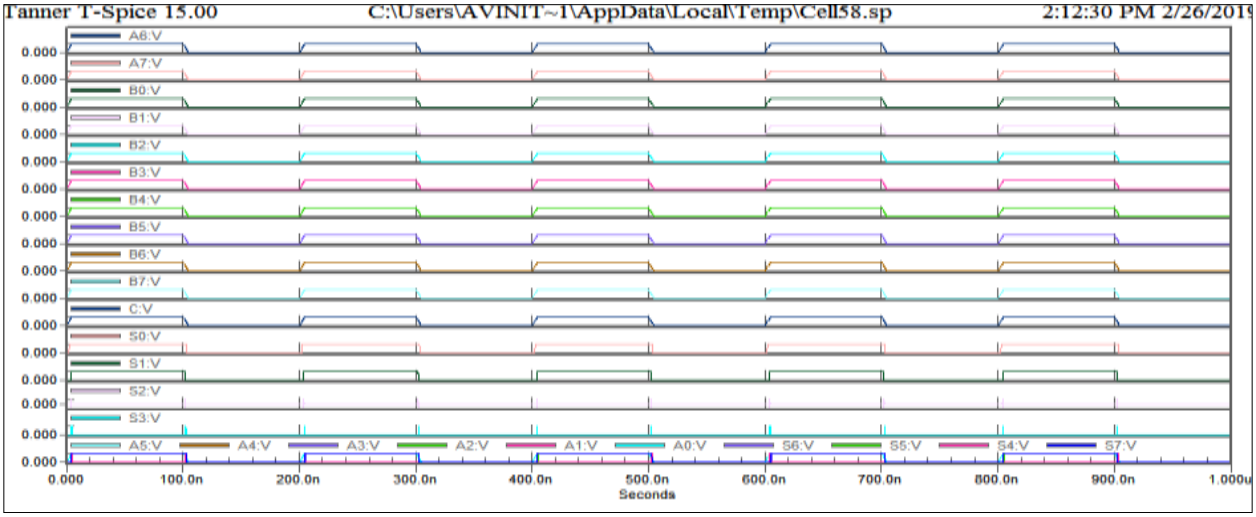

Fig 25. Simulation of Multiplier and Addition

The first Multiplier output is "P0=1, P1=0, P2=0, P3=0, P4=0, P5=1, P6=1, P7=1" and the second Multiplier output is "Q0=1, Q1=0, Q2=0, Q3=0, Q4=0, Q5=1, Q6=1, Q7=1" when all of the inputs are equal to one. The result of addition of two multipliers as shown in Fig 25 and the outputs obtained are "S0=1, S1=1, S2=0, S3=0, S4=0, S5=0, S6=1, S7=1 and carry=1"

Conclusion

The throughput for NFC is lower in the available technology that is in the range of Kilo Bits per Seconds (Kbps).But in this proposed methodology the number of bits per symbol are increased. There is a separate module for transmitter and receiver in NFC have synthesized in tanner EDA tool. By using advanced modulation technique like ternary Quadrature Amplitude Modulation technique in the

transmitter part the data rate or throughput is increases from Kbps to Mbps. The algorithm such as Mean Square Error (MSE) implemented in the receiver part. By using TQAM levels are increased. Therefore the data rate is also improved from 212Kbps to 8.46Mbps.Fig 26 shows the Data rate comparison of different modulation techniques in Near Field Communication.

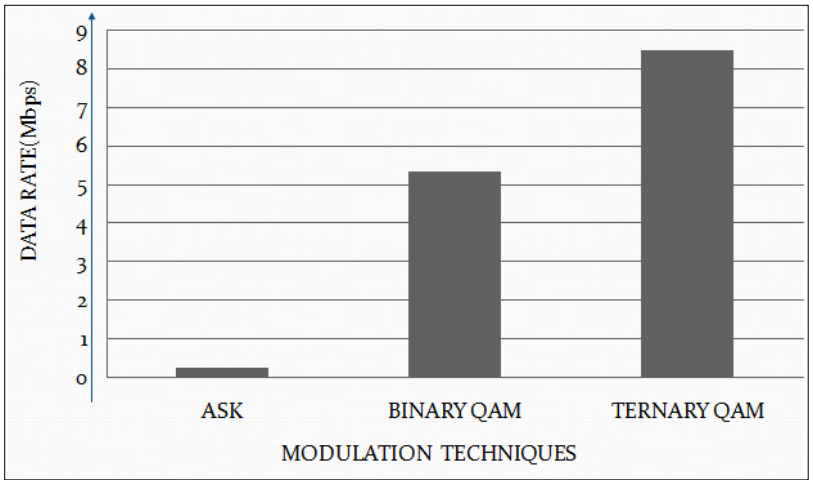

Fig 26. Comparison of data rate in NFC

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