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Embedded Run-time Reconfiguration Techniques in Wireless Sensor Network Applications using Field Programmable Gate Arrays(FPGA)

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Abstract

The Runtime Reconfigurable Techniques are used for efficient and reliable transmission of data across the Wireless Sensor networks. The industrial applications demands the efficiency of reconfigurable networks with respect to both power and size. The general reconfiguration scenarios can be Reconfiguration at network level, Reconfiguration at node level and Partial runtime reconfiguration. In this paper, the Field Processing Gate Array (FPGA) is used for reconfiguration of Industry applications which demands hardware and software reconfigurations during runtime, while retaining the I/0 devices active. The FPGAs provides high performance due to its flexibility towards Parallelism and reconfigurability. The concept is synthesized in different FPGA families like Viretx4 (XC4VFX12), Virtex5 (XC5VLX50) and Virtex7 (XC7VX485T). To analyze the various parameters like temperature and fire, the reconfiguration of FPGA is done during the runtime. The conditions are identified based on the thresh- hold values set as normal or danger. Basically to achieve the Partial Reconfiguration, the first part of the module the FPGA is configured through the static programming and in the next phase the FPGA is reconfigured and then the program is run. The simulation results of the modules before Reconfiguration and after the reconfiguration are demonstrated.

Index Terms *– Runtime Reconfiguration, Field Processing Gate Array (FPGA),Wireless Sensor Networks, Parallelism.*

I. INTRODUCTION TO RUNTIME RECONFIGURATION OF WSN

The Wireless Sensor networks is the most leading technology in the modern era. The advancement of micro-sensor technology has made the Wireless Sensor Networks to cater the needs of the end users with low cost and accuracy[1]. The Wireless sensor networks are also used in various applications such as Health Monitoring[2],Water Quality Measurement and Monitoring[3], Industrial Data Acquisition, Process and control[4], Vehicle Monitoring Systems[5]. Bao Liu et.al[6] has proposed and implemented the security Reconfiguration-Based VLSI Design has been proposed and implemented using SPARC V8 LEON2 processor, which would prevent the code attacks of either software or hardware. Norbert Abel et.al[7] have designed and demonstrated the Dynamic Partial reconfiguration (DPR)framework to for the better utilization of FPGA in data acquisition applications.

Yana Esteves Krasteva et.al[12], have designed a frame work for the Reconfigurable Node as shown in fig.2.1. The implementation of dynamic reconfiguration has changed the specific Wireless Sensor Networks to general purpose networks.. The general reconfiguration scenarios include Reconfiguration at network level, Partial runtime reconfiguration and Reconfiguration at node level. The Reconfiguration at the network level is going to define the updates of both hardware and software. The new configuration to the network can be sent to the Micro controller.

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<table>
<tr><td colspan="4">Application</td></tr>
<tr><td colspan="4">Reconfiguration Control</td></tr>
<tr><td colspan="4">Node Descriptors</td></tr>
<tr><td>Reconfigurable Hardware Abstraction Layer</td><td colspan="3">Hardware Abstraction Layout</td></tr>
<tr><td>Partial Run-time Reconfigurable System</td><td rowspan="2">Sensors</td><td rowspan="2">Radio</td><td rowspan="2">Microcontroller</td></tr>
<tr><td>Field Programmable Gate Arrays</td></tr>
</table>

Fig.2.1. Framework of Reconfigurable Node.

II. Related works of runtime reconfiguration techniques in wireless sensor network applications

Hanen Grichi et.al[8], have presented a new design methodology named RWiN for Reconfigurable Wireless Sensor Networks (RWSN) to execute the tasks related to software configuration.

J. Guevara, E. Vargas et.al[9], have proposed the Transducer Electronic Data Sheet (TEDS) architecture for monitoring of environmental wireless sensor networks.

S.Commuri et.al[11], have demonstrated a technique to reduce the overhead of implementing dynamic data aggregation in a network. They have used the reconfigurable cluster heads(RCHs) based on the Field Programmable Gate array.

Yibin Li et.al[13], demonstrated the usage of scheduling strategy in energy harvesting application. Based on the energy available the scheduling of task is done. The most required tasks are run on the hardware. This saves the maximum energy consumption.

Sani Abba [14] et.al, have proposed a efficient monitoring of real time applications and control the on-chip sensor networks for FPGA. The proposed system is self aware and reduces the power consumption.

S.Meena et.al[10], have demonstrated the Runtime Reconfigurations of Wireless Sensor node using the FPGA. The implementation of Runtime Reconfigurations using FPGA, reduces the constraints such as bandwidth and memory in WSN applications.

III. Implementation of Runtime Reconfiguration of WSN using FPGA

The FPGA is used for the Monitoring and controlling the Industrial Applications. During the emergency, the Wireless sensor network is reconfigured at the run time. The reconfigurable wireless sensor network is implemented in Xilinx ISE design suite 14.5. The programming language used is Verilog Hardware Description Language (VHDL). The concept of runtime reconfiguration is synthesized in different FPGA families Viretx4 (XC4VFX12), Virtex5 (XC5VLX50) and Virtex7 (XC7VX485T). The system model of this concept is shown as in fig 3.1:

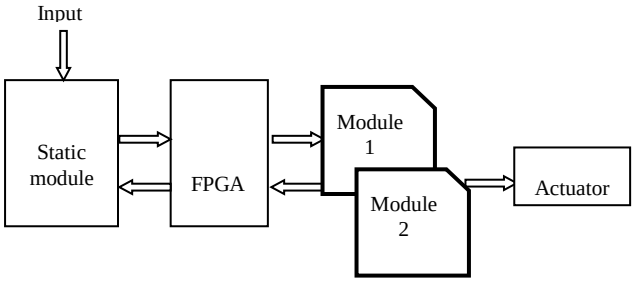

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Fig. 3.1. System Module of Reconfiguration.

The Entire System Module of Reconfiguration consists of two modules. The Module 1 consists of temperature sensor and Smoke sensor. The temperature is represented as the Low value and or High value depending on the standard temperature set. The thresh hold value of the temperature is set for the threshold value 50^{0}. The temperature is checked constantly and if the temperature value varies above or below the threshold value, then the smoke sensor is activated indicating the occurrences of Fire. The Module 2 controls and actuate the movement of motor in both clockwise and anticlockwise direction with the help of IR sensor and photo resistor. The node is programmed before the reconfiguration process and it is connected to the remote system. The reconfiguration can be controlled by the crossbar switch during the implementation part.

A. Result analysis for virtex4 FPGA:

The performance of runtime reconfiguration in WSN is analysed with two modules, before reconfiguration and after reconfiguration. The Fig . 3.2 shows result of the power analysis before Reconfiguration for Virttex4 FPGA.

Device	
Family	Virtex4
Part	xc4vfx12
Package	sf363
Temp Grade	Commercial
Process	Typical
Speed Grade	-12

Environment	
Ambient Temp (C)	50.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.012	1	---	---
Logic	0.000	21	10944	0
Signals	0.000	155	---	---
DCMs	0.000	0	4	0
IOs	0.159	131	240	55
Leakage	0.170			
Total	0.341			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	14.7	80.0	55.0

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.084	0.010	0.074
Vccaux	2.500	0.095	0.000	0.095
Vcco25	2.500	0.001	0.000	0.001

	Total	Dynamic	Quiescent
Supply Power (W)	0.341	0.012	0.329

Fig.3.2 Power Analysis before Reconfiguration

The Fig.3.3 shows the Power Analysis after Reconfiguration. The before reconfigurable design consumes 0.341W whereas the design after reconfiguration consumes 0.180W. Likewise, the maximum operating frequency of design consumes 199.56MHz and 205.497 MHz for both before and after reconfiguration respectively.

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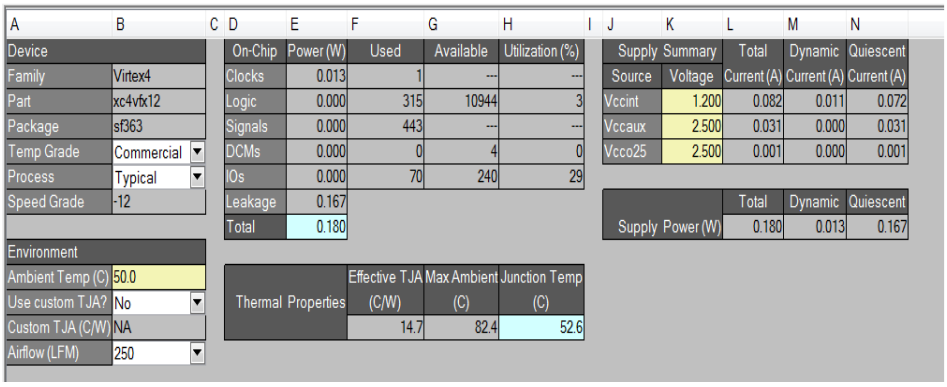


Device	
Family	Virtex4
Part	xc4vfx12
Package	sf363
Temp Grade	Commercial
Process	Typical
Speed Grade	-12

Environment	
Ambient Temp (C)	50.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.013	1	---	---
Logic	0.000	315	10944	3
Signals	0.000	443	---	---
DCMs	0.000	0	4	0
IOs	0.000	70	240	29
Leakage	0.167			
Total	0.180			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	14.7	82.4	52.6

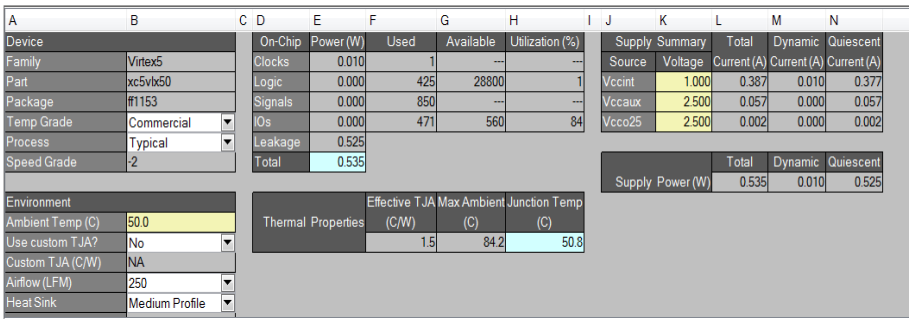
Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.082	0.011	0.072
Vccaux	2.500	0.031	0.000	0.031
Vcco25	2.500	0.001	0.000	0.001

	Total	Dynamic	Quiescent
Supply Power (W)	0.180	0.013	0.167

Fig:3.3 Power Analysis after Reconfiguration

B. Result Analysis for Virtex5 FPGA:

The power analysis of Virtex5 FPGA families before the Runtime Reconfiguration is 0.535W and after reconfiguration is 0.528W, with a maximum operating frequency of 217.361 and 221.293MHz respectively. The.Fig.3.4 shows the power Analysis before Reconfiguration and the fig.3.5 shows the Power analysis after Reconfiguration.



Device	
Family	Virtex5
Part	xc5vlx50
Package	ff1153
Temp Grade	Commercial
Process	Typical
Speed Grade	-2

Environment	
Ambient Temp (C)	50.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile

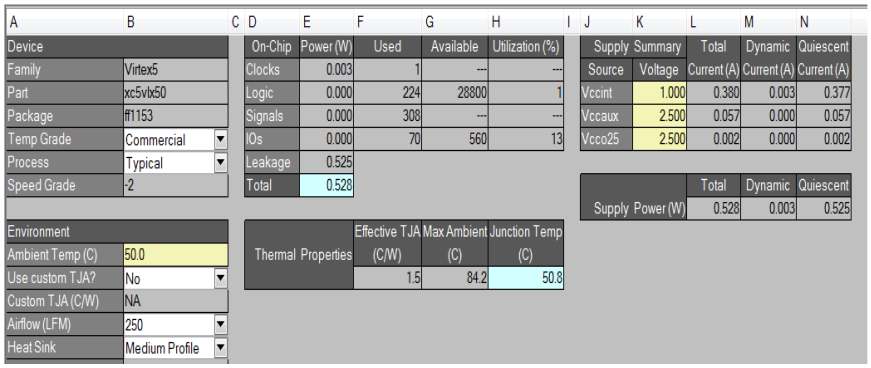
On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.010	1	---	---
Logic	0.000	425	28800	1
Signals	0.000	850	---	---
IOs	0.000	471	560	84
Leakage	0.525			
Total	0.535			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	1.5	84.2	50.8

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.387	0.010	0.377
Vccaux	2.500	0.057	0.000	0.057
Vcco25	2.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.535	0.010	0.525

Fig.3.4.Power Analysis Before Reconfiguration



Device	
Family	Virtex5
Part	xc5vlx50
Package	ff1153
Temp Grade	Commercial
Process	Typical
Speed Grade	-2

Environment	
Ambient Temp (C)	50.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.003	1	---	---
Logic	0.000	224	28800	1
Signals	0.000	308	---	---
IOs	0.000	70	560	13
Leakage	0.525			
Total	0.528			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	1.5	84.2	50.8

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.380	0.003	0.377
Vccaux	2.500	0.057	0.000	0.057
Vcco25	2.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.528	0.003	0.525

Fig.3.5. Power analysis after Reconfiguration

C. Result Analysis for Virtex7 FPGA:

The power analysis of Virtex 7 families before the Runtime Reconfiguration is 0.216W and after reconfiguration is 0.143W with the maximum operating frequency of 187.03MHz and 191.077MHz after the reconfigurable design. The Fig.3.6 shows the Power Analysis Before Reconfiguration and Fig.3.7 after reconfiguration respectively.

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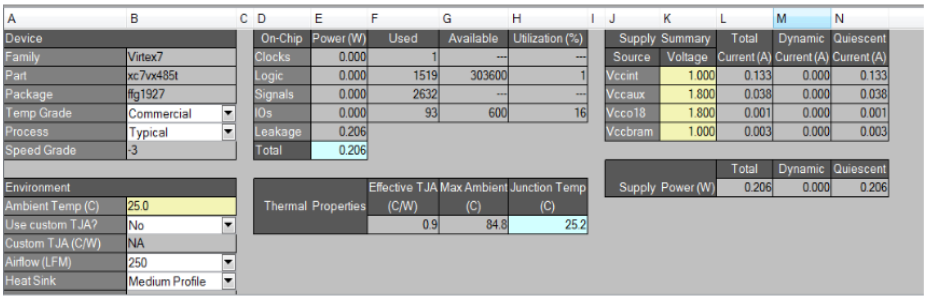


Device	
Family	Virtex7
Part	xc7vx485t
Package	ffg1927
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	1519	303600	1
Signals	0.000	2632	---	---
IOs	0.000	93	600	16
Leakage	0.206			
Total	0.206			

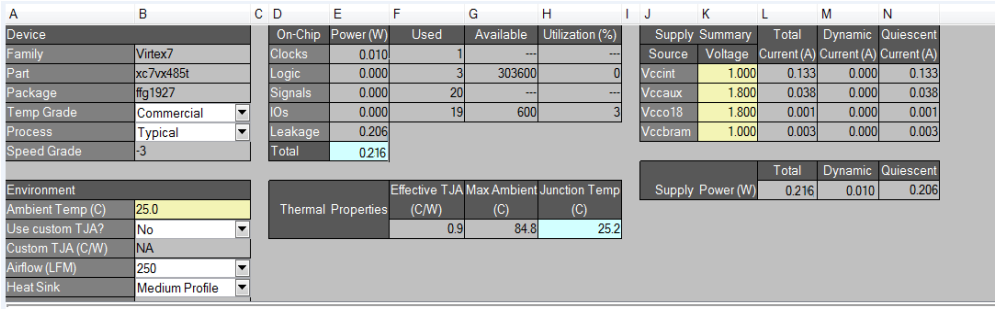
Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.133	0.000	0.133
Vccaux	1.800	0.038	0.000	0.038
Vcco18	1.800	0.001	0.000	0.001
Vccbram	1.000	0.003	0.000	0.003

	Total	Dynamic	Quiescent
Supply Power (W)	0.206	0.000	0.206

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	0.9	84.8	25.2

Fig.3.6 Power Analysis Before Reconfiguration



Device	
Family	Virtex7
Part	xc7vx485t
Package	ffg1927
Temp Grade	Commercial
Process	Typical
Speed Grade	-3

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.010	1	---	---
Logic	0.000	3	303600	0
Signals	0.000	20	---	---
IOs	0.000	19	600	3
Leakage	0.206			
Total	0.216			

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.133	0.000	0.133
Vccaux	1.800	0.038	0.000	0.038
Vcco18	1.800	0.001	0.000	0.001
Vccbram	1.000	0.003	0.000	0.003

	Total	Dynamic	Quiescent
Supply Power (W)	0.216	0.010	0.206

Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	0.9	84.8	25.2

Fig. 3.7. Power Analysis after Reconfiguration

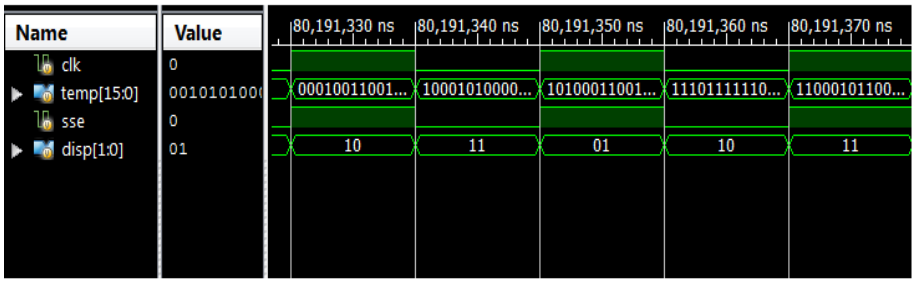


Fig.3.8 Timing Diagram Before Reconfiguration

Fig.3.8 shows the Timing Diagram before Reconfiguration. The Fig.3.9 shows the RTL schematic diagram of RTL inner block Before Reconfiguration.Fig.3.10. shows the inner block after Reconfiguration.

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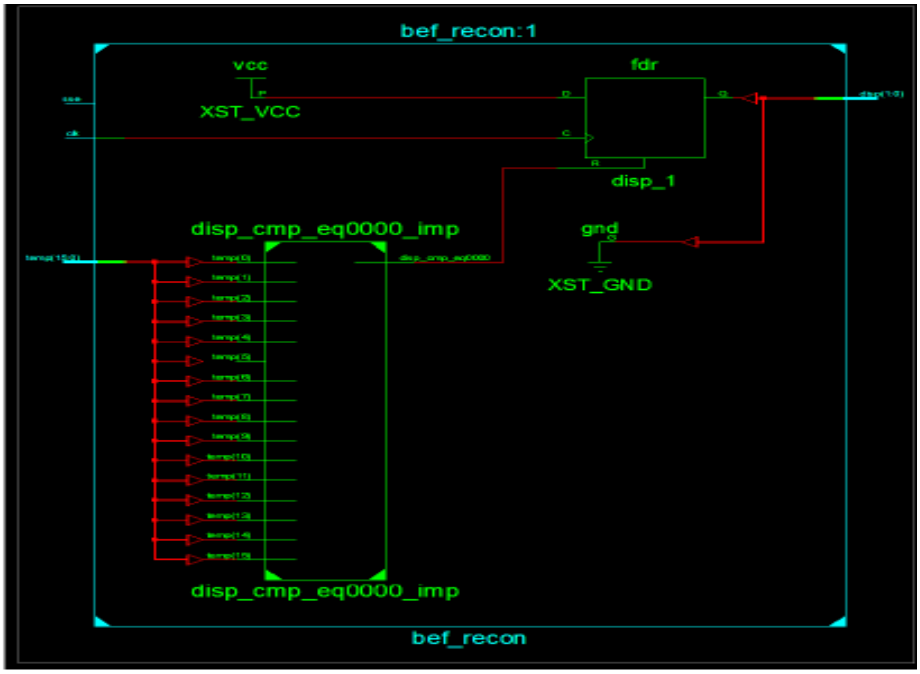

Fig.3.9 RTL innerblock Before Reconfiguration

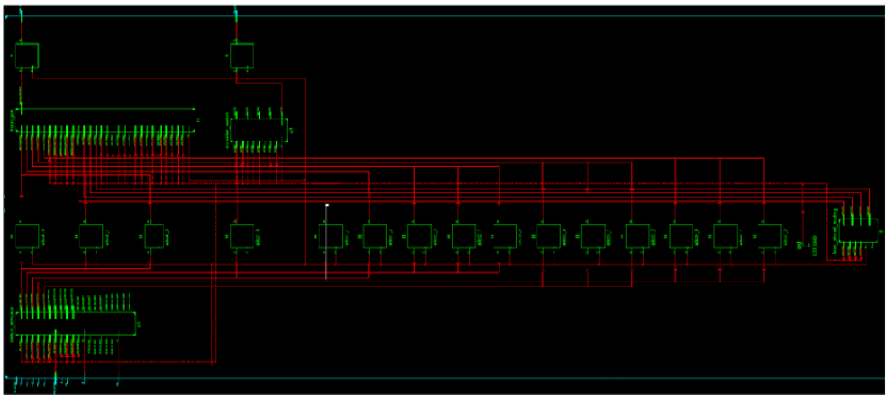

Fig.3.10. RTL inner block After Reconfiguration

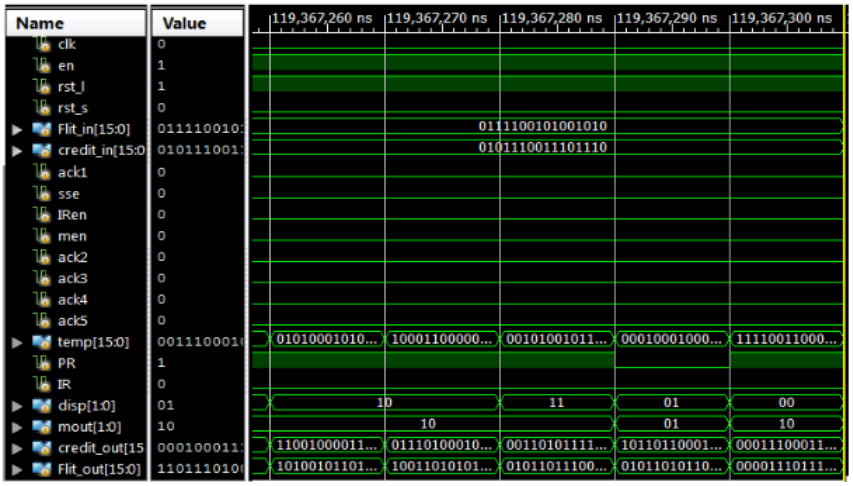

Fig : 3.11.Timing Diagram Results after Reconfiguration

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IV CONCLUSION

The FPGA's provides the flexibility for the designer to tailor the application for runtime reconfigurations by selecting the appropriate flip flops, storage units and logic gates. The performance of runtime reconfiguration in WSN is analysed with two modules before and after reconfiguration. The Module 1 and Module 2 are experimented on the different FPGA families namely Viretx4 , Virtex5 (XC5VLX50) and Virtex7 (XC7VX485T). The use of FPGA during the runtime reconfigurations in various industrial applications provides an optimum solution with better utilization of power , time and memory.

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