

SUMULTI CODES- A Binary Forward Error Correcting Scheme

Dr.P.Sri Hari.*

Department of Electronics and Communication Engineering
GEETHANJALI COLLEGE OF ENGINEERING & TECHNOLOGY, Hyderabad, India
Email: mail2pshari@yahoo.com

Abstract

Forward Error correction, also referred to as Channel Encoding plays a vital role in providing error free or reliable information transmission/reception. A linear Block Code specified as (n, k) code encodes 'k' bit data into 'n' bit code word, by appending $r = n - k$ redundant bits, which are also referred to as parity bits.. The (n, k) Block Code is with a code efficiency or code rate of $R = \frac{k}{n}$, expressed as percentage. The provision of parity bits enables the code to address the influence of the additive noise in the channel on the message transmitted. The errors occurred in the data received can be Random errors, Burst Errors, and Random-Burst-type errors. The present discussion proposes two Channel encoding schemes namely "DATA INVERTING CODES" and "SUMULTI CODES", which are capable of correcting the channel errors.

Key words: Code efficiency, Parity word, Data Inverting Code, Sumulti code, Random and Burst errors, Constituent code, Error Vector

1.Introduction:

In a linear Block code represented as (n, k) code, each data word represented by a k-tuple as $D = [d_1 \ d_2 \ \dots \ d_k]$ is transformed independently into a code word represented as an n-tuple $C = [c_1 \ c_2 \ \dots \ c_n]$. In a Binary Block Code, the code elements are selected from binary alphabets 0 and 1, and hence the code is Binary Code.

In a systematic block code, each code word contains the original 'k' symbol(bit) data block unaltered, and the redundant bits are expressed in terms of data bits. These expressions are code specific. In the present paper, "SUMULTI CODES", with the ability of correcting various types of channel errors are proposed and each code word of SUMULTI code is 2- Dimensional, which is constructed using a 1-Dimensional (n, k) Data Inverting code (Weight Based Code) which is the constituent code for the specified SUMULTI code. In this 1-Dimensional code, in some of the code words, the inverted data word is the parity word and hence the name. The encoding of a data word is depending on the number of Non-Zero elements that are present in it i.e. its Weight. Hence, is the name Weight Based Code. All these constituent codes are 50% efficient. The code word of A SUMULTI code is a two dimensional $(8, k)$ code array and thus contains $8 \times k$ elements.

2. (n, k) Data Inverting Codes:

These codes can also be named as "Codes with Unequal Parity Bit Structure", since all the data words are not of the same weight. All the proposed Data Inverting codes (which are the constituent codes for SUMULTI codes) are systematic codes and are capable of correcting single error.

Dr.P.Srihari
mail2pshari@yahoo.com

2.1.Code word generation:

The code word of a Data Inverting code is expressed as $C = [d_1 \ d_2 \ \dots \ d_k \ p_1 \ p_2 \ \dots \ p_k]$ where $D = [d_1 \ d_2 \ \dots \ d_k]$ is the 'k' bit data word and $P = [p_1 \ p_2 \ \dots \ p_k]$ is the parity word of length $(n - k)$ with $n = 2k$.

In the code word C

- ❖ For the data word with zero/even weight → parity word is same as data word .
- ❖ For the data word with odd weight → parity word is the negated data word.

2.2.Decoding:

Let the code word at the receiver be $R = [d_1 \ d_2 \ \dots \ d_k \ p_1 \ p_2 \ \dots \ p_k]$

(R may not be equal to C)

Under the reception with no error, each R satisfies the following conditions:

In the received code word,

Condition1:

- If parity word is same as the data word, $\sum_i(d_i + p_i) = 0$, i bounded from 1 to k
- If the parity word is the negated data word, $\sum_i(d_i + p_i) = 1$, i bounded from 1 to k

Condition2:

- If the parity bits are same as the data bits, there will be $2k$ summations, where all result in a 0.
- Each sum consists of k terms.
- In each sum, the difference between number of data bits and parity bits will have a value form the set of integers $\{0,1,2,\dots,k\}$.

For Ex., in a (6, 3) Data inverting code, the summations are,

$$d_1 + d_2 + d_3 = 0; d_2 + d_3 + p_1 = 0; d_3 + p_1 + p_2 = 0; p_1 + p_2 + p_3 = 0;$$

$$p_2 + p_3 + d_1 = 0; p_3 + d_1 + d_2 = 0;$$

- If the parity bits are the inverted data bits, the above $2k$ summations result in alternate 1/0

For the received code word, if Condition-1 and condition-2 deviate from the results under error free communication, it indicates the reception is not error free.

2.2.1. Error Detection and Correction:

The difference between the received(R) and the transmitted (C) code vectors is referred to as Error Vector E. This is expressed as $E = R + C$. Under error free reception, $E = [0 \ 0 \ 0 \ \dots \ 0]_{1 \times n}$. If the reception is with error/s, E is a non zero vector.

For a given R, computation of E depends on the structure of the parity word and error location in R.

2.2.1.1. Identifying the structure of the parity word :

The structure of the parity word in R can be identified based on the Modulo-2 sum (length k) of D and P of R i.e. $D + P$.

In R,

- if the parity word is same as the data word,
 - ✓ $D + P = [0 \ 0 \ \dots \ 0]_{1 \times k}$, under error free R

- ✓ $D + P$ consists of $(k - 1)$ number of 0s, under R with error
- If the parity word is the negated data word,
 - ✓ $D + P = [1\ 1\ \dots\ 1]_{1 \times k}$ under error free R
 - ✓ If the reception is with error, $D + P$ consists of $(k - 1)$ number of 1s , under R with error

2.2.1.2. Estimating the Error Location:

Error location in R can be estimated using Condition-1. Deviation of any of the ' k ' summations of R with reference to the error free condition is an indication of either d_i or p_i of that summation is in error.

3.2.1.2.1. Locating the Error :

Error in R can be located using the **Condition-2**. The ' $2k$ ' summations of Condition-2 are partitioned into two equal halves, such that if k summations in one of the partitions contain d_i , then the summations of other partitions contain p_i or vice versa. The k summations of which partition differ from the error free conditions is considered to contain the error and the error will be either d_i or p_i that is available in all the k summations of that partition.

2.2.1.2.2. Error Correction:

The corresponding E consists of $(n - 1)$ zeros and a single 1. The position of 1 in E corresponds to the position of the located error in R. The corrected Code word is $C = R + E$.

3. SUMULTI CODES:

Using the proposed single error correcting Data Inverting code as the constituent code, the code word of the SUMULTI code can be generated. SUMULTI code stands for SUM-MULTIPLICATION code. The code word of the code is 2-dimensional. There are two stages of encoding. In the first stage, the 2-Dimensional code array is constructed using the specific Data Inverting code being the constituent code. In the final stage, all the columns of the array are encoded using an (8,4) Data Inverting code, column wise. The total number of elements in the code word of the SUMULTI code is $8Xk$.

3.1. Code word Generation:

In the first stage of encoding, the k bit data word is encoded using the respective Data inverting code. The k bit data word and the k bit parity word of the above data inverting code form the first and second rows respectively in the code array of the code word of a SUMULTI code. The third row and fourth rows of the array are respectively the Modulo-2 sum and the AND product (element wise) of the first and second rows.

In the second stage of encoding, each of the ' k ' columns of the code array will be encoded using (8, 4) Data Inverting Code, there by forming an $(8, k)$ code word of the SUMULTI Code.

3.2. Locating and correcting the Error/s:

The code word will be sent through Block interleaving, i.e. row wise with $(8Xk)^{th}$ element in the last row of the array as the first and first element of the first row as the last.

At the receiver, is arranged back in the same order as an array.

The process of locating and correcting the error/s is implemented on the received on column by column basis.

4. Illustration:

Let the received code array be

$$\begin{matrix} 1 & 0 & 1 \\ 0 & 0 & 1 \\ 1 & 1 & 1 \\ 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \\ 0 & 0 & 0 \end{matrix}$$

(6,3) Data Inverting code is the constituent code, as the first row of the array which is the actual data word is of length 3.

Column-1 of the received code array is

$$\begin{matrix} a & b & c & d & e & f & g & h \\ 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \end{matrix}$$

** a, b, c, \dots , represent the bit positions.

The Modulo-2 sum of bits in the positions e, f, g, h and the bits in the positions a, b, c, d is 0000 , indicating that the column-1 of the received array is encoded using the Data Inverting code $(8, 4)$, where the parity bits of this code word are same as the first four bits, **and is received without error. The corresponding Error Vector is $E=00000000$.**

Similar Modulo-2 additions for column-2 of the code array results in 0100 indicating that column-2 is also encoded similar to column-1, and there is a single error in the received. It's location can be estimated as either the position b or f of the 2nd column.

To locate the error, the summations of Condition-2 are partitioned into two halves such that summations in Partition-1 contains the bit in position b and summations in Partition-2 contains the bit in position f .

Under Error Free reception, this partitioning will be

Table1. Partitioning under error free reception

Partition-1	Partition-2
$a + b + c + d = 0$	$c + d + e + f = 0$
$b + c + d + e = 0$	$d + e + f + g = 0$
$g + h + a + b = 0$	$e + f + g + h = 0$
$h + a + b + c = 0$	$f + g + h + a = 0$

The summations are for the bits in the positions indicated.

These summations for column-2 of the received result in

Table2. Partitioning in the case of received

Partition-1	Partition-2
$a + b + c + d = 1$	$c + d + e + f = 0$
$b + c + d + e = 1$	$d + e + f + g = 0$
$g + h + a + b = 1$	$e + f + g + h = 0$
$h + a + b + c = 1$	$f + g + h + a = 0$

Since, the summations in Partition-1 are differing from the results under error free conditions, and all the summations are having b in common, it can be decided that the bit in that position of column-2 of the array is in error. The respective Error Vector is $E = 0 1 0 0 0 0 0 0$. Thus, the error free column -2 of the received array will be $E + \text{Column-2 of the received}$, which results in $0 1 1 0 0 1 1 0$.

Similar process for column-3 of the received array indicates the presence of error in position a of the column-3. The respective Error Vector is $E = 1 0 0 0 0 0 0 0$. Thus, the error free column -3 of the received array will be $E + \text{Column-3 of the received}$, which results in $0 1 1 0 0 1 1 0$

Thus, the error free code array is

$$\begin{matrix}
 1 & 0 & 0 \\
 0 & 1 & 1 \\
 1 & 1 & 1 \\
 0 & 0 & 0 \\
 1 & 0 & 0 \\
 0 & 1 & 1 \\
 1 & 1 & 1 \\
 0 & 0 & 0
 \end{matrix}$$

5. Probability of Undetected Error:

If the presence of the error is not detected, such error becomes an Undetected error. With reference to a Binary Symmetric Channel, if the code used for only error detection, the probability with which the detector misses the error i.e. probability with which the error is undetected is $p(e)$.

The probability for the receiver for not detecting the error $p(e) =$

$(1 - p)^L \cdot [W\left(\frac{p}{1-p}\right) - 1]$, where, $W\left(\frac{p}{1-p}\right) = W(\alpha)|_{\alpha=\frac{p}{1-p}}$, where $W(\alpha) = \sum_{i=0}^n W_i \cdot \alpha^i$ is the weight enumerator of the code, and W_i gives the number of code words of the SUMULTI codes having weight ' i '. ' p ' is the transition probability i.e. $p(0/1)$ or $p(1/0)$ and ' L ' is the length of the code word. .

The set of weight distributions of the SUMULTI code, with (6,3) Data Inverting constituent code is $\{W_0, W_{12}\} = \{1, 7\}$, i.e. the code is having 1 code word with a zero weight and 7 code words with weight Twelve. Thus, the corresponding (24,3) SUMULTI code has a weight enumerator $W(\alpha) = 1 + 7\alpha^{12}$.

The Probability of for the receiver for missing the error detection is $p(e) =$

$$(1 - p)^{24} \left[1 + 7 \left(\frac{p}{1-p} \right)^{12} - 1 \right].$$

For a transition probability of 10^{-1} , $p(e)$ is found to be 1.97×10^{-12} . This can be interpreted as: if there are 10^{12} code digits present at the detector, on average 2 incorrect digits will be undetected.

6. Conclusion:

The Proposed Data Inverting Code corrects single error present in the code word. SUMULTI code is a Two dimensional code used to correct multiple number of errors, both random and Burst errors. The proposed SUMULTI code words will be obtained from the corresponding Data Inverting Code as a constituent code.

The proposed SUMULTI codes has the capacity of correcting burst errors of burst length ' k ' (appearing along a row of the code array), in addition to having the capacity of correcting random errors.

7. References:

1. Abraham Lempel, & Shmuel Winograd (July 1977). - "A New Approach to Error Correcting Codes" - IEEE Trans. Inform. Theory, vol. IT-23, No. 4, pp. 505-508.
2. Andrew J. Viterbi, & Jim K. Omura (1979). - "Principles of Digital Communication and Coding" - McGraw-Hill International Edition
3. F. J. MacWilliams & N. J. A. Sloane (1977). - "The Theory of Error-Correcting Codes" - North Holland Publishing Company
4. Richard E. Blahut (Nov. 1977). - "Composition Bounds for Channel Block Codes", IEEE Trans. Inform. Theory, Vol. IT-23, No. 6, pp. 656-674.
5. Shu Lin, Daniel & J. Costello, JR (1983). - "Error Control Coding - Fundamentals and Applications" Prentice-Hall, Inc. Englewood Cliffs, New Jersey 07632
6. P. Sri Hari & Dr. B. C. Jinaga (2007). - "DATA INVERTING CODES" - Ph.D Thesis, Jawaharlal Nehru Technological University, Hyderabad, India.
7. N. SHRIBALA, Dr. P. SRIHARI and Dr. B. C. JINAGA. - "Data Negation Codes - A Binary Channel Coding Scheme" - 2013 IEEE INDICON held at Indian Institute of Technology, Bombay, India, during 13-15 Dec, 2013
8. Dr. P. SRIHARI. - "Multiple Error Correcting Binary Channel Coding Schemes and their error Performance" - International Journal of Innovative Research in Computer and Communication Engg. - Vol. 2 Issue 2, February, 2014.
9. Dr. P. SRIHARI. - "Sum Codes - A Binary Channel Coding Scheme" - International Journal of Computer Science and Technology - Vol. 5 Issue Spl 1, January - March, 2014, p. No. 60-64.
10. Dr. P. SRIHARI. - "Multiplication Codes - A Multiple Error correcting Binary Channel Coding Scheme" - International Journal of Applied Engineering Research, Vol. No. 9, Pg. Nos. 8857-8873 August 2014

Authors



Name: Dr. P. Srihari

Profile:

Dr. P. Srihari obtained his Ph.D from Jawaharlal Nehru Technological University, Hyderabad, India. He is having 30 years of Teaching experience. His areas of interest are Communication Engineering and Signal processing. He is the author of Text Books in the area of Digital Communication, Random Variables and Random Processes.