International Journal of Future Generation Communication and Networking
Vol. 13, No. 1, (2020), pp. 612 - 617

Array Multiplier Using Multiplexer based Pass Transistor Logic Style Full Adders

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Abstract

For designing the high speed and low power multiplier are normal in layout of extensive research significance. An arithmetic logic unit is the combinational logic electronic circuit that performs the arithmetic and logical operation by using binary numbers, ALU is the heart of the CPU, It performs the addition, multiplication and all compression operations. The all ALU operations multiplication is a complex operation which can be done by full adders. In digital circuits the multiplication process consumes the large power compare to other operations. In multiplier concept, there are many ways to moderate the partial products in multiplication procedure among that one of the important method is array multiplier. The hybrid logic style full adder design is based on the new 14 transistor structure. The proposed full adder circuit design is based on the multiplexer, which reduce the number of transistors in the design, less capacitance effect and high driving capacity. In array multiplier major role is full adder functions, which determines the multiplier function In this paper new multiplexer based logic style full adder functions are analyzed and used in the array multiplier.

Keywords: *Full adder, Multiplier, Hybrid logic style, Delay, HPSC, TFA.*

1. Introduction

In computer system the arithmetic building blocks play the major role of the simplest controller to the complex processor in last several years. The full adder is the main concentration in the arithmetic logic operation, based on the full design the circuit speed and are estimated. The full adder circuit designs in multiple logic styles. The conservative CMOS type adder circuits contain the Pull Up and Pull Down networks, where all logic style consists the some merits and de-merits. The popular logic design style in VLSI is conventional, complementary metal oxide semiconductor, it consist the pull up and pull down in PMOS and nMOS network connections [4].

The pull up network consists only the PMOS transistor, which connection differs from the logic, for OR operation the in pull up network the PMOS transistor in series connection and similarly AND operation PMOS transistor in parallel connection. In the pull down network OR operation the in pull up network the NMOS transistor is connected to the parallel and similarly AND operation NMOS transistors are connected in series. In comparison with conventional, complementary metal oxide semiconductor the mixture structure circuits have minimum connection supply and ground. The conventional, complementary metal oxide semiconductor consists the high input capacitance due large number of connections with MOS transistors which reduce the operation speed.

The mixture logical design uses the distinctiveness of the separate logical circuit of design to increase the efficiency. At gate level modeling XOR and XNOR (Fig1

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and Fig 2) circuits which plays a major role for design the full adder circuit [3].The transistor level structure for XOR and XNOR are used to solve the clock arriving issues in global and internal clocks gating technique is used in the adaptive clock gating technique in flip flops 978-1-4799-6818-3/15/$31.00 © 2015 IEEE, which consumes the least power and the simple structure for clock gating technique, and also which overcomes the internal global clock issues in their structure. It is efficient and suitable method for avoiding clock timing issues. [9]

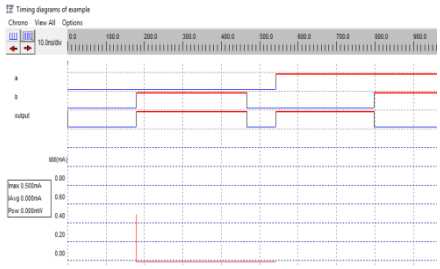

Figure. 1. XOR Gate Timing Analysis

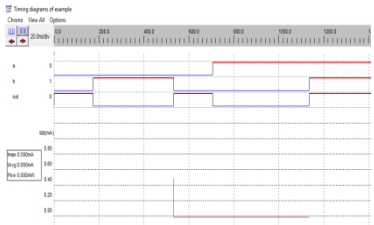

Figure. 2. XNOR Gate Timing Analysis

2. Hybrid Logic Style Full Adders

The full adder circuit in multistage structure the driving capacity and input capacitance are important parameters along with the integral form of our timing analysis behavior. The new HPSC [1] Adder circuit produces better performance compared to the normal conventional full adder circuit. The new HPSC adder circuit consists of XOR and XNOR gate structure. The new HPSC adder circuit switching timing and driving capacity is good and the capacitance value, low but the connections to the gate, capacitance value is high compare to C-CMOS, TFA, TGA and NEW 14T (Fig 3) structure [3].

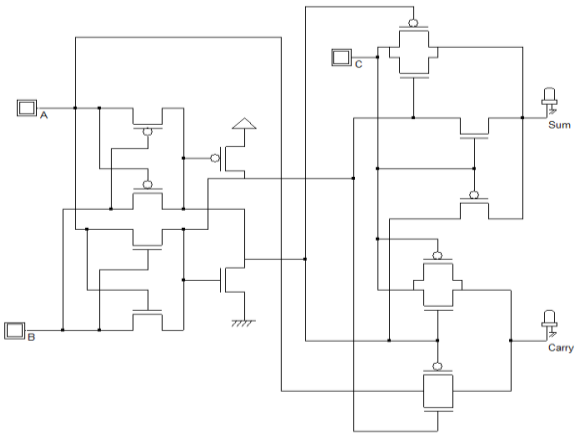

Figure. 3. 14T adder

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The incidence of the intrinsic inverter in response in conservative CMOS and HPSC adder circuit offers equal and better driving capacity The hybrid structure design and modification of the circuits are proposed by the simple exact algorithm which is a good sizing algorithms and flexible for covering both desirable characteristics and structural difficulties in single object optimizations and multi object optimization but the same technique does not suitable for behavioral analysis and delay measurements.

The Sutherland et al [2] was first presented the idea of logical effort. Multiplexer based, full adder design contains the two multiplexer circuits and logical xor gate circuit; the response or gate signal acts the control lines of the multiplexer circuits. In this method the proposed adder adder circuit consists the less are comparable to the conventional method the synchronized response shows that the usual power drop in 8 bit circuit is 29.94% and 19 bit circuit 44.97% and also the average delay is reduced 11.8 % [4].

3. Proposed Design

One of the significant constraints in VLSI Design is the area reduction, which plays the major role in recent technology. The proposed design is multiplexer based, full adder circuit; the analysis has been presented against the complexity and easy to understand the structure and working principle. The designer has clear initiative about, the circuit design has high efficient to run faster in multiplier circuit in multi-stage model. The main significant parameter in this method is considered by the designer to achieve a better response of the circuit with a modified mixture design before the simulation analysis.

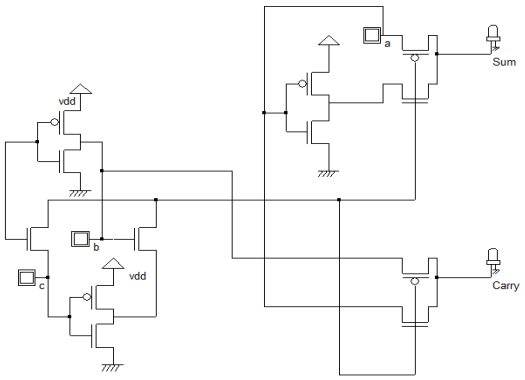

Figure. 4. MUX based FA

The proposed design consists the multiplexer and xor gate circuit in structural model, the xor gate design is made up of pass transistor concept which increases the response of the operation and reduces the circuit difficulty. The Compare to the Conservative-CMOS and Proposed circuit (Fig 4) design consist the less number of transistor and speed also high. . It can be predictable for Conservative -CMOS and proposed full adder circuit design, tender the less capacitance value and speed of the operation also much better. In the conservative logic endeavor, the gate delay (D) of CMOS circuit is

$$D=G.H.P+P$$

The number of transistors and capacitance value in multiplexer based, full adder is less compared to the other design method. The Table 1 and figure 5 clearly demonstrate the comparative of transistor count in multiplexer based, full adder design and other design method. Similarly, Table 2 and figure 6 clearly

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demonstrate the comparisons of capacitance value of multiplexer based full adder design and other design method

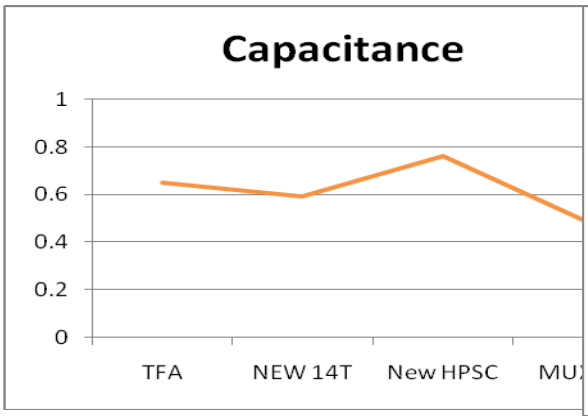

Figure. 5. Comparison of Capacitance Value

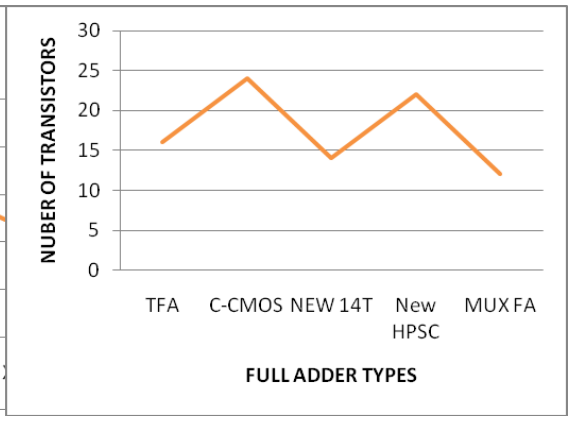

Figure. 6. Comparison of Transistor count

Parameter	TFA	C-CMOS	NEW 14T	New HPSC	MUX based FA
Area	16	24	14	22	12

Table 1. Transistor Comparisons

Parameter	TFA	NEW 14T	New HPSC	MUX FA
Capacitance(fF)	0.653	0.594	0.7633	0.495

Table 2. Capacitance Comparisons

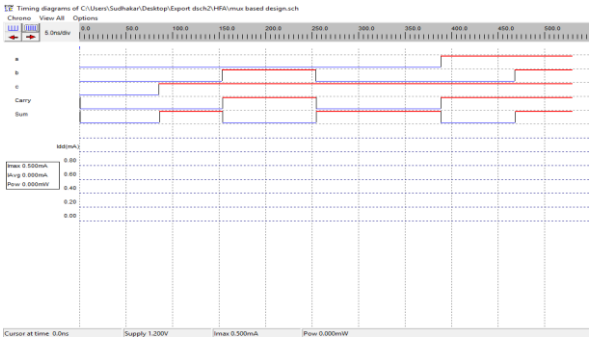

Figure. 7 Proposed design wave form analysis

4. Simulation Results

The below mentioned simulation results are taken by the micro wind expert tool for better analysis about multiplexer based full adder design The simulation results carried out by waveform analysis (fig 7), Layout design (Fig 7) Capacitance value (Fig 9), Id v's Vd (Fig 10), Id v's VG (Fig 11), Log (Id) vs VG (Fig 12) and Threshold voltage (13)

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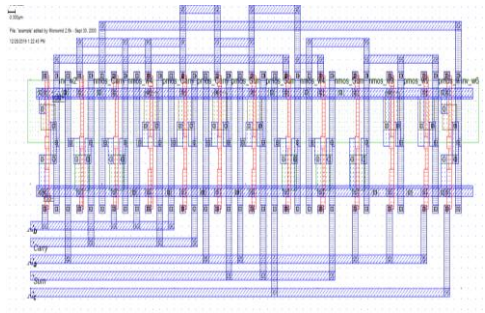

Figure. 8 Layout design

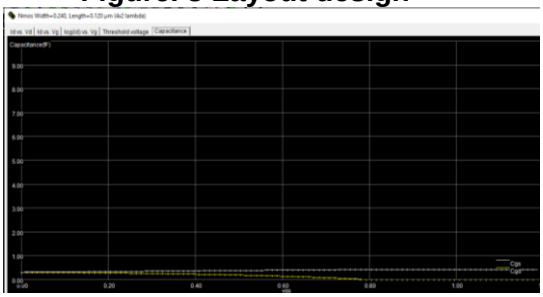

Figure. 9 Capacitance value

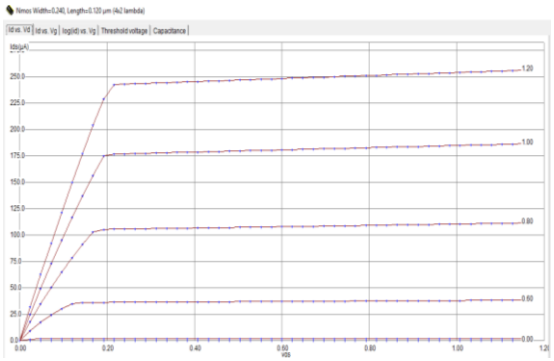

Figure. 10 Id vs Vd

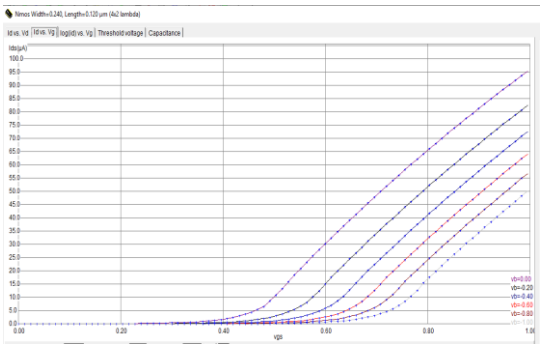

Figure. 11 Id vs Vg

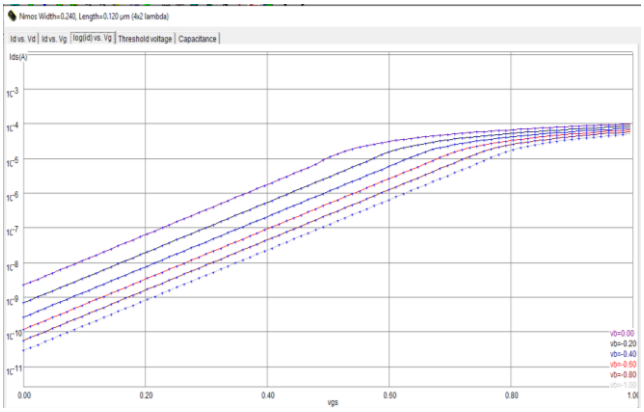

Figure. 12 Log (Id) vs Vg

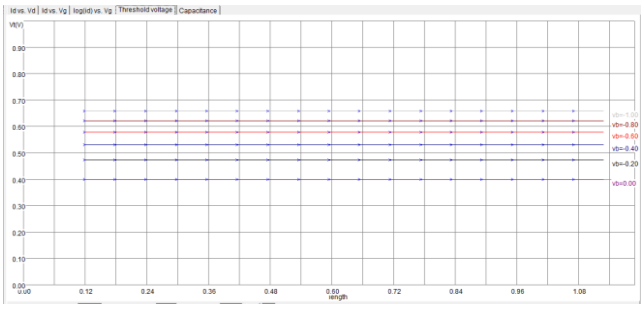

Figure. 13 Threshold voltage

5. Array Multiplier Concept

The array multiplier is well recognized in the standard method, the array multiplier design structure depends on the add and shift algorithm. The every result is obtained by multiplication of the multiplicand with single multiplier bit, the partial product is shifted according to the bit order and the summed. The sum is able to carry out by a carry spread adder. In worst case delay of multiplier is

$$D(\text{delay}) = (2n+1)\, t_d$$

The multiplication in step by step process Fig 14

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$$
\begin{array}{cccccccc}
 & & & a_3 & a_2 & a_1 & a_0 & \\
 & & \times & b_3 & b_2 & b_1 & b_0 & \\
\hline
 & & & p_{30} & p_{20} & p_{10} & p_{00} & \\
 & & p_{31} & p_{21} & p_{11} & p_{01} & \times & \\
 & p_{32} & p_{22} & p_{12} & p_{02} & \times & \times & \\
p_{33} & p_{23} & p_{13} & p_{03} & \times & \times & \times & \\
\hline
s_7 & s_6 & s_5 & s_4 & s_3 & s_2 & s_1 & s_0
\end{array}
$$

Figure. 14 Array multiplier concept

6. Conclusion

In this proposed pass transistor logic style mixture adder circuit which or gate design is based on the pass transistor logic, which increases the speed of calculation, less area and minimum capacitance value compared to the C-CMOS and other circuits. The proposed design is a simple method for the multistage structure with reliable blocks. The responses are significant to estimate the performance of the adder such as different types of adder structure and capacitance and area analysis etc. Also, graphical analysis, which helpful understand the circuit behavior and layout design which makes circuit design in back end process.

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11.1. Journal Article

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