International Journal of Future Generation Communication and Networking
Vol. 13, No. 1, (2020), pp. 330 - 340

HIGH-EFFICIENCYACTIVE CLAMP FLYBACKCONVERTER DESIGN

[1]S.Arunprathap, [2]K.Aiyappan, [2]S.T.Dharanish, [2]K.B.Jananee, [2]D.Kanimozhi
[1]Assistant Professor, [2]UG Student
Department of Electronics and Communication Engineering,
M.Kumarasamy College of Engineering, Karur, Tamilnadu

Abstract

The reference design is developed for evaluating 13-W isolated active clamp flyback Powered Devices converter using the IEEE802.3 at Power Over Ethernet interface and DC/DC controller TPS23756. The converter is capable of supporting the 13-W permitted IEEE802.3 at power requirements. It presents good efficiency, load regulation and associated electrical performance. It supports IEEE802.3 at compliant power devices. This combines PowerOver Ethernet Poawered Device and DC/DC controller simplifies the model. It provides high efficiency and better EMI performance with soft-switching technology. All the measurements were done using the DC source to stimulate Power Over Ethernet Power Supply Equipment. A isolated active clamp flyback converter with hiccup protection reference design is implemented in Printed Circuit Board.

Keywords: : *Power over Ethernet, Powered Devices, Power Supply Equipment,Flyback Converter,DC/DC controller,Soft-Switching Technology.*

INTRODUCTION

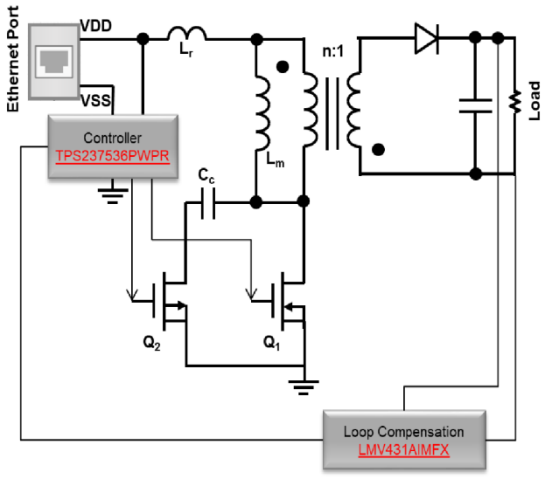
Power-over-Ethernet (PoE) applications preferred high efficiency due to restricted input power. The IEEE 802.3at specification limits the input power of a powered device to 13 W for low-power systems and 25.5 W for high-power systems. Telecommunication applications, which can have battery backup or exigent thermal requirements, additionally requires high efficiency. For several reasons, employing an active reset is an excellent choice for optimizing efficiency in these and many other low-power applications.

First, the transformer currents soften the switching losses of the primary MOSFETs. Second, the clamp provides near lossless snubbing on the primary. In the forward converter, the transformer is always driven into the first and third quadrants, providing better core utilization. There is no 50% duty-cycle limitation, allowing for wide input ranges and lowering the stresses on the switching components. Third and most significant, the secondary's voltage waveforms are ideal for implementing self-driven synchronous rectifiers.

The DC-DC controller attributes two complementary gate drivers with programmable dead time. This simplifies the model of active-clamp forward converters or optimized gate drive for highly-efficient flyback topologies. The second gate driver is also disabled if desired for single MOSFET topologies. The controller additional attributes internal soft start, bootstrap start-up source, current-mode compensation, and a 78% maximum duty cycle.

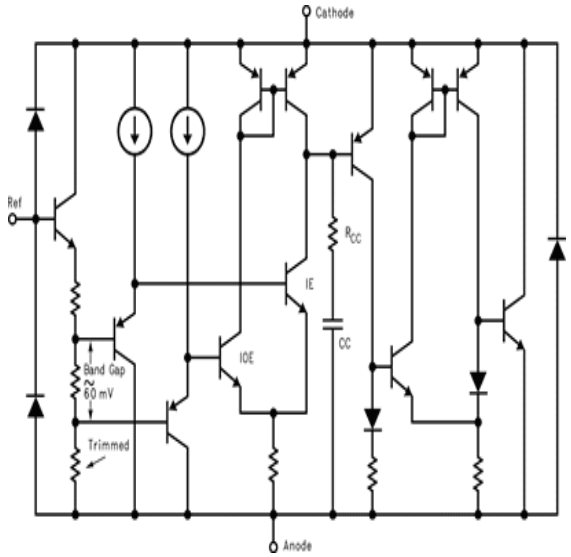
ISSN: 2233-7857 IJFGCN

PROPOSED SYSTEM
BLOCK DIAGRAM



LMV431A-Low-Voltage(1.24V) Adjustable Precision Shunt Regulators

The LMV431, LMV431A and LMV431B are exactitude1.24 V shunt regulators capable of adjustment to 30 V. Negative feedback from the cathode to the adjust pin controls the cathode voltage, very similar to a non-inverting op amp configuration . A two-resistor potential divider terminated at the regulate pin controls the gain of a 1.24 V band-gap reference. Shorting the cathode to the alter pin (voltage follower) provides a cathode voltage of a 1.24 V.



The LMV431, LMV431A and LMV431B have relavent initial tolerances of 1.5%, 1%, and 0.5%, and functionally lend themselves to several applications that prefers zener diode category performance at low voltages. Applications incorporate a 3 V to 2.7 V low drop-out regulator, an error amplifier in a 3 V off-line switching regulator and at the same time as a voltage detector. These parts are typically stable with capacitive loads greater than 10 nF and less than 50 pF.

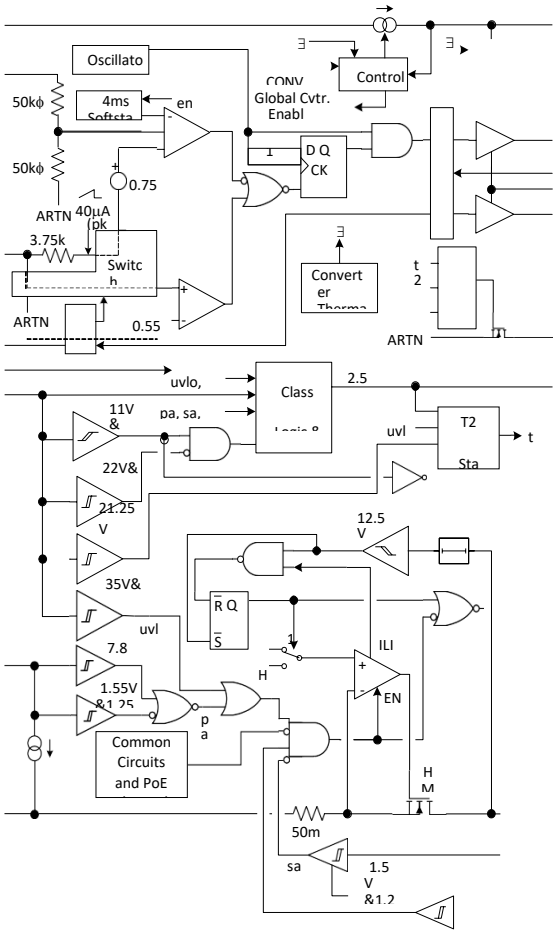
The LMV431, LMV431A and LMV431B offers performance at a competitive price.

TPS23756-High Power/High Efficiency PoE Interface and DC/DC Controller

ISSN: 2233-7857 IJFGCN

The TPS23756 devices has a combined power-over-ethernet (PoE), powered-device (PD) interface, and current-mode DC-DC controller optimized specifically for isolated converters. The IEEE 802.3 is supported by the power-over-ethernet interface.

The TPS23754 and TPS23756 support a range of input voltage ORing alternativesincluding maximum voltage, external adapter preference, and power-over-ethernet preference. These attributes allow the designer to work out that power supply can carry the load below all conditions.



The Power over Ethernet interface attributes the new extended hardware classification necessary for compatibility with high-power midspan power sourcing equipment (PSE) per IEEE 802.3at. The detection signature pin may also be used to force power from the Power over Ethernet source off. Classification can be programmed to any of the outlined types with a single resistor.

A programmable and synchronizable generatorpermits design optimization for efficiency and eases use of the controller to upgrade existing power supply designs. Exact programmable blanking, with a default period, simplifies the typical current-sense filter design trade-offs.

The TPS23754 device has a 15-V converter start-up whereas the TPS23756 device has a 9-V converter start-up. The TPS23754-1 replaces the PPD pin with a no-connect for enhanced pin spacing.

ISSN: 2233-7857 IJFGCN

Flyback Converter

When cost is a major concern, the flyback topology is usually the preferred choice. In its basic outline, it utilizes a single primary FET and a single secondary rectifier. The latter will be either a diode or a synchronous FET. Many design references exist for the flyback converter. Adding synchronous rectification and active clamp to the flyback converter can provide significant gains in efficiency.

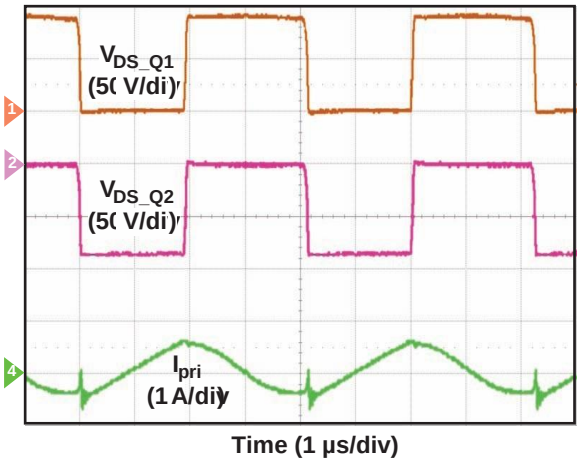


Figure shows the simplified power stage for a flyback converter with an active clamp and a synchronous-FET rectifier. A diode-rectified flyback converter allows the secondary current to flow in only one direction and can operate in discontinuous-conduction mode (DCM) at light loads. Interestingly, a flyback converter with synchronous rectifiers allows the secondary current to flow in both directions and forces a continuous conduction mode (CCM) to occur over the entire load range. At light loads, this AC circulating current will reduce the efficiency (compared to a diode-rectified flyback) as it flows though the primary FET, secondary FET, and transformer. Choosing the correct primary inductance for the power transformer willscale back the losses by reducing the AC circulating currents.

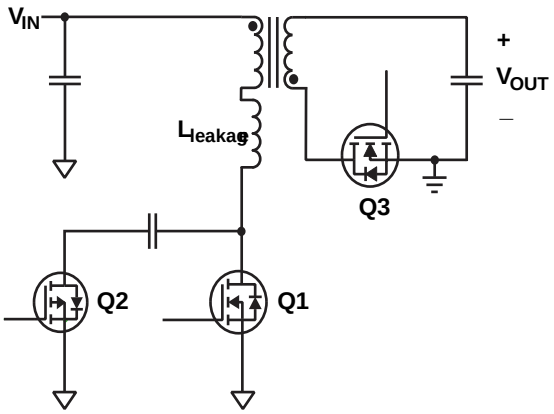
Transformer Design

When the primary inductance for the flyback transformer is selected, trade-offs need to be made. With lower inductance, losses at light loads will be ligher due to the higher peak-topeak AC circulating current. Higher inductance will improve light-load efficiency by reducing the peak-to-peak ripple current. But higher inductance will require more primary turns and larger core. This will increase the winding losses and reduce the efficiency at higher loads. Also, the right-half-plane zero (RHPZ) in the control loop is inversely proportional to the primary inductance.

$$\text{RHPZ}=\frac{\text{Rload}\times(1-\text{D})^2}{2\pi LD}$$

As the inductance increases, the RHPZ moves lower in frequency. To achieve acceptable phase and gain margins, the loop crossover frequency should be at least one decade below the RHPZ frequency. A primary inductance that results in a peak-to-peak ripple current of 25 to 50% of the maximum load current is usually a good compromise between peak-to-peak current, transformer size, and RHPZ frequency.

ISSN: 2233-7857 IJFGCN



For a flyback converter operating in CCM, the transformer turns ratio and input-voltage range determine the duty-cycle range:

$$D = \frac{V_{OUT} \times \frac{N_{pri}}{N_{sec}}}{V_{IN} + V_{OUT} \times \frac{N_{pri}}{N_{sec}}}$$

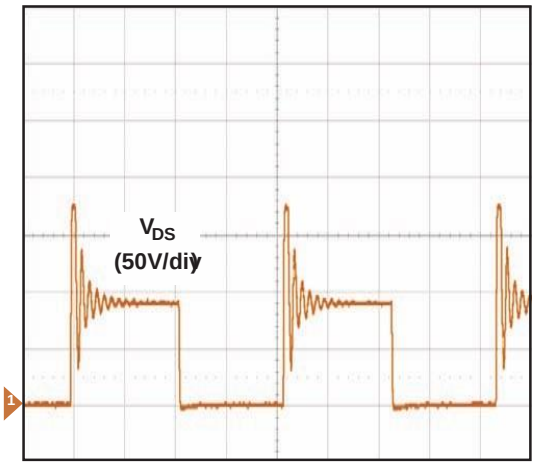
An input range of 36 to 75 V covers most PoE An input range of 36 to 75 V covers most PoEand telecom applications. For this input range,the transformer turns ratio is usually selected toachieve a maximum duty cycle of 60% at theminimum input voltage of 36 V. This results ina minimum duty cycle of approximately 42% atthe maximum input voltage of 75 V. One of thebenefits of the flyback topology is that it canaccommodate a wide input range without severechanges in duty cycle. Fig. 7 shows how thechoice of transformer turns ratio affects the VDSratings of the primary FETs (Q1 and Q2). The sum of the input voltage and reflectedoutput voltage is plotted versus the input voltage,where the duty cycle was set to 60% for a 36-Vinput. This neglects the effects of any peakingfrom the clamp resonance, which must also beconsidered before the VDS rating of the primaryFETs is determined.

Active-Clamp Circuit

Because of the large voltage spike that occurs when Q1 turns off, a primary FET with a ligher voltage rating is often required. FETs with higher voltage ratings generally have higher RDS(on) and slower switching times, both of which reduce efficiency. Resistor R1 in the lamp must also dissipate part of the energy in the leakage inductance, which can be significant. In addition, the voltage overshoot and ringing that occur when the primary FET's drain is turned off may create an EMI issue.

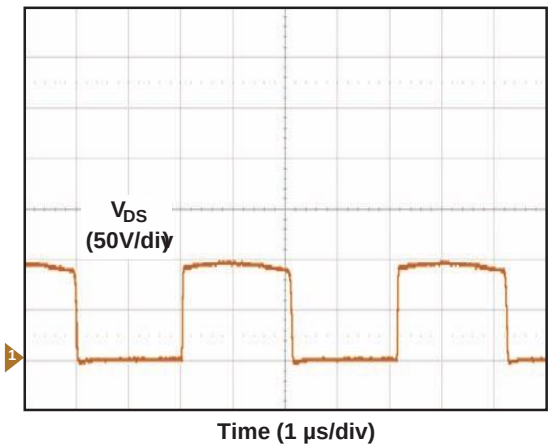
Because of the large voltage spike that occurs when Q1 turns off, a primary FET with a ligher voltage rating is often required. FETs with higher voltage ratings generally have higher RDS(on) and slower switching times, both of which reduce efficiency. Resistor R1 in the lamp must also dissipate part of the energy in the leakage inductance, which can be significant. In addition, the voltage overshoot and ringing that occur when the primary FET's drain is turned off may create an EMI issue.

ISSN: 2233-7857 IJFGCN



The active-clamp circuit, provides significant benefits versus an RCD clamp the drain-to-source voltage of the primary FET no longer has the large voltage spike when it is turned off. Instead of being dissipated in a resistor, the leakage energy is mostly recovered and returned to the input capacitors. Eliminating the leakage spike permits a primary FET with a lower VDS rating to be used, improving efficiency. Potential EMI issues are also significantly reduced.

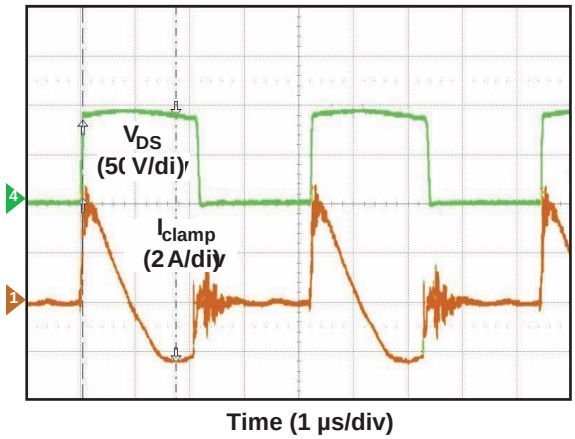
In the operation of an active-clamp flybackconverter, the transformer's primary leakage inductance plays a crucial role. A simplified schematic of the flyback converter's activeclamp power stage, including the leakage inductance.



When Q1 is on, operation is the same as with a standard flyback converter. The current flows into the transformer's primary, storing energy in the primary's magnetizing and leakage inductances.

During this time, Q2 and Q3 are off, while the output capacitor supplies current to the load.

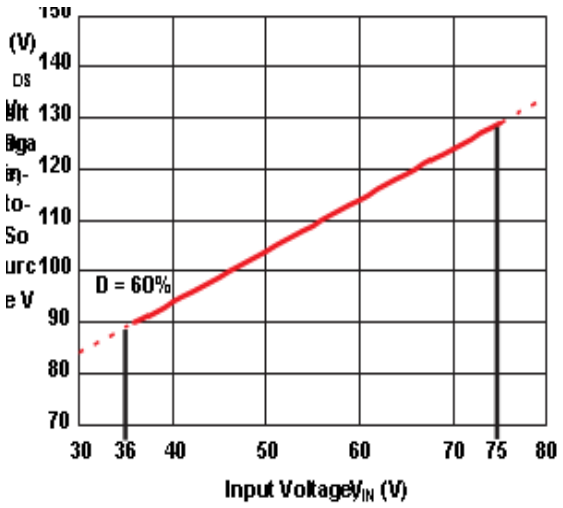
ISSN: 2233-7857 IJFGCN



When Q1 turns off, Q2 and Q3 turn on. The stored energy in the magnetizing inductance is diverted by Q3, supplying current to the load and charging the output capacitor. The output capacitor is connected across the secondary winding and gets reflected through the transformer to the primary, essentially shorting the primary winding. With the voltage on the primary's magnetizing inductance held to the reflected output voltage, the current flowing in the clamp will resonate with Lleakage and Cclamp at a frequency of

$$f_{clamp} = \frac{1}{2 \times \sqrt{\text{Lleakage} \times \text{Cclamp}}}$$

The instantaneous current flowing in the clamp circuit at the moment when Q2 turns on is equal to the peak primary current. Neglecting circuit losses, the clamp current will resonate fclamp while Q1 is off.



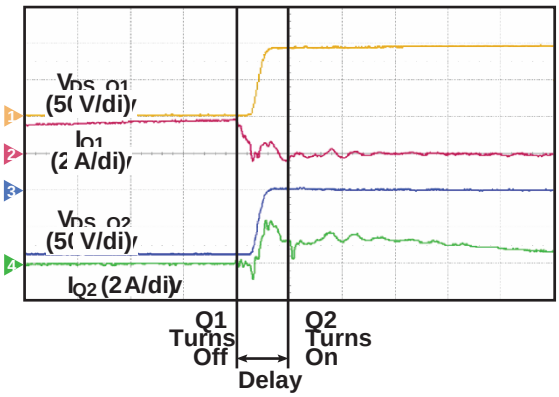
As can be seen from the clamp current's waveform, the current will flow in both directions through Q2. The magnitude and direction of the clamp current when Q2 turns off depends on the duty cycle. If the clamp current is flowing from drain to source when Q2 turns off, the clamp current continues to flow through the body diode of Q2. In this scenario, when Q1 turns on, Cclamp dispenses until the body diode of Q2 completes reverse recovery and turns off. This results in significantly increased power dissipation in Q1. To prevent this condition, it is required for fclamp to be selected such that the clamp current is flowing from source to drain through Q2 when Q1 turns on. If fclamp is set equal to the switching frequency, the current will be flowing in the correct direction for duty cycles between

ISSN: 2233-7857 IJFGCN

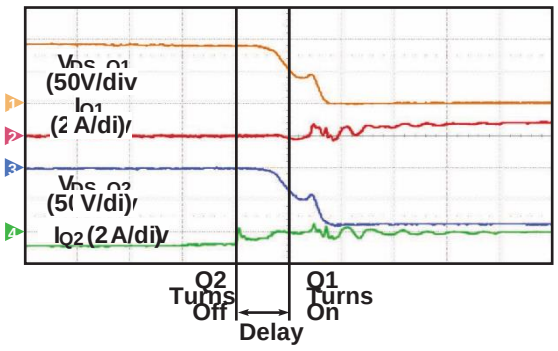
25% and 75%. (The cosine waveform crosses 0 at p and 3p/2.) Cclamp is typically selected to obtain an acceptable value for fclamp, per Equation (6). The leakage inductance can be measured or taken from the transformer specification. The measured leakage inductance can be much lower than the maximum rated leakage from the transformer specification. To account for variations in the leakage inductance, fclamp should be about 20% lower than the switching frequency.

Soft Switching

Before Q1 turns off, the peak primary current is flowing through the transformer's agnetizing inductance, leakage inductance, and Q1 to ground. When the gate of Q1 is pulled low, the current stored in the magnetizing inductance (gap) begins to transfer to the secondary winding, but only after the voltage on the secondary transitions up to the point where theinternal diode of Q3 is forward-biased.

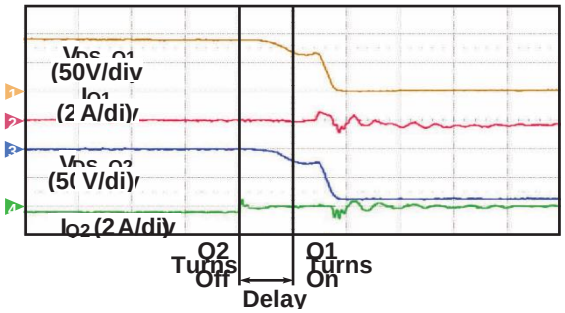


When Q1 is completely off, the current flowing in the leakage inductance is commuted from Q1 through the clamp capacitor and body diode of Q2 before Q2 actually turns on. After a delay time, Q2 is turned on with 0 V across it. The load and duty cycle have no effect, because the peak current is always flowing in the same direction during this transition.



Assuming that the clamp frequency was properly chosen, the clamp current will flow from source to drain through Q2 before Q1 turns on. When Q2 is switched off, the clamp current will continue to flow through the body capacitance of Q2, resonating with the leakage inductance. The clamp current also commutates to the body capacitance of Q1, again resonating with the leakage inductance. It can be seen that Q2 switches off with 0 V across it.

ISSN: 2233-7857 IJFGCN



After a delay,the gate of Q1 transitions high, and Q1 begins to turn on. As may be seen from the waveforms, this transition does not take place with the voltage fully at zero. At maximum load, the drain of Q1 resonates down toward ground before Q1 is switched on, achieving partial zero-voltage switching. At lighter loads), Q1's drain voltage does not resonate as far down because there is less energy stored in the leakage before this transition occurs. Since the resonant frequency of the falling drain voltage depends on various parasitic capacitances and the leakage inductance of the transformer, it is difficult to precisely calculate the required delay time. The best way to select a delay time is to measure these waveforms on an actual converter with maximum load. The delay time should be set such that Q1 turns on just before Q1's drain voltage reaches the resonant valley.

CONCLUSION AND FUTURE WORK

The project represents an example of systematic approach to the assessment of High-Efficiency Active Clamp Flyback Converter Design. This article provides an introduction to PoE and the higher-power Power over Ethernet, outlining the standards, explaining the components parts, Powered Devices, Power Supplying Equipment, "midspan" and "endspan" Ethernet switches and splitters and describing a simple system. When developing or upgrading an Ethernet-based communication systems, investing on PoE architecture is a cost effective upgrade for industrial based Ethernet switches systems, as it reduces the need to maintain numerous separate remote interruptible power source units to guard against data loss during power outage situations.

REFERENCE

1. The Fly buck Converter - Lecture notes - ECEN4517 - Department of Electrical And Computer Engineering - University of Colorado, Boulder.
2. S.Palanivel Rajan, et.al., "Performance Evaluation of Mobile Phone Radiation Minimization through Characteristic Impedance Measurement for Health-Care Applications", IEEE Digital Library Xplore, ISBN : 978-1-4673-2047-4, IEEE Catalog Number: CFP1221T-CDR, 2012.
3. M.Paranthaman, S.Palanivel Rajan, "Design of Implantable Antenna for Biomedical Applications", International Journal of Advanced Science and Technology, P-ISSN: 2005-4238, E-ISSN: 2207-6360, Vol. No.: 28, Issue No. 17, pp. 85-90, 2019.
4. S.Palanivel Rajan, et.al., "Experimental Explorations on EOG Signal Processing for Real Time Applications in LabVIEW", IEEE Digital Library Xplore, ISBN : 978-1-4673-2047-4, IEEE Catalog Number: CFP1221T-CDR, 2012.
5. Dr.S.Palanivel Rajan, Dr.C.Vivek, "Performance Analysis of Human Brain Stroke Detection System Using Ultra Wide Band Pentagon Antenna", Sylwan Journal, ISSN No.: 0039-7660, Vol. No.: 164, Issue : 1, pp. 333–339, 2020.
6. Dr.S.Palanivel Rajan, Dr.C.Vivek, "Analysis and Design of Microstrip Patch Antenna for Radar Communication", Journal of Electrical Engineering & Technology, Online ISSN No.: 2093-7423, Print ISSN No.: 1975-0102, Vol. No.: 14, Issue : 2, DOI: 10.1007/s42835-018-00072-y, pp. 923–929, 2019.

ISSN: 2233-7857 IJFGCN

7. Hennessy, John L.; Patterson, David A. (2002). Computer Architecture: A Quantitative Approach. The Morgan Kaufmann Series in Computer Architecture and Design. Morgan Kaufmann. p. 707. ISBN 9780080502526.
8. Rajan, S., & Paranthaman, M. (2019). Characterization of compact and efficient patch antenna with single inset feeding technique for wireless applications. Journal of Applied Research and Technology, 17(4).
9. Dr.S.Palanivel Rajan, L.Kavitha, "Automated retinal imaging system for detecting cardiac abnormalities using cup to disc ratio", Indian Journal of Public Health Research & Development, Print ISSN: 0976-0245, Online ISSN: 0976-5506, Vol. No.: 10, Issue : 2, pp.1019-1024, DOI : 10.5958/0976-5506.2019.00430.3, 2019.
10. T.Abirami, S.Palanivel Rajan, "Cataloguing and Diagnosis of WBC'S in Microscopic Blood SMEAR", International Journal of Advanced Science and Technology, P-ISSN: 2005-4238, E-ISSN: 2207-6360, Vol. 28, Issue No. 17, pp. 69-76, 2019.
11. Rajan S. P, Paranthaman M. Novel Method for the Segregation of Heart Sounds from Lung Sounds to Extrapolate the Breathing Syndrome. Biosc.Biotech.Res.Comm. 2019;12(4).DOI: 10.21786/bbrc/12.4/1, 2019.
12. Dr.S.Palanivel Rajan, "Design of Microstrip Patch Antenna for Wireless Application using High Performance FR4 Substrate", Advances and Applications in Mathematical Sciences, ISSN No.: 0974-6803, Vol. No.: 18, Issue : 9, pp. 819-837, 2019
13. Fingas, Jon (25 February 2014). "Freescale makes the world's smallest ARM controller chip even tinier". Retrieved 2 October 2014.
14. Sadasivan, Shyam. "An Introduction to the ARM Cortex-M3 Processor"Arm Holdings on July 26, 2014.
15. T.Abirami, Dr.S.Palanivel Rajan, "Detection of poly cystic ovarian syndrome (PCOS) using follicle recognition techniques", Bioscience Biotechnology Research Communications, ISSN: 0974-6455, Vol. 12, Issue : 01, pp. 1-4, DOI: 10.21786/bbrc/12.1/19, 2019.
16. Dr.S.Palanivel Rajan, "Enrichment of ECG Quality using Independent Component Analysis for Dynamic Scenario by Eliminating EMG Artifacts", Advances and Applications in Mathematical Sciences, ISSN No.: 0974-6803, Vol. No.: 18, Issue : 2, pp. 219-237, 2018.
17. Dr.S.Palanivel Rajan, S.Suganya, "Design of Loop Antenna for the Human Brain Signal Analysis", Indian Journal of Science and Technology, Online ISSN No.: 0974-5645, Print ISSN No.: 0974-6846, Vol. No.: 11, Issue: 10, pp. 1-6, DOI: 10.17485/ijst/2018/v11i10/120829, 2018.
18. M.Paranthaman, Dr.S.Palanivel Rajan, "Design of E and U Shaped Slot for ISM Band Application", Indian Journal of Science and Technology, Online ISSN No.: 0974-5645, Print ISSN No.: 0974-6846, Vol.: 11, Issue: 18, pp. 1-3, DOI: 10.17485/ijst/2018/v11i18/123042 2018.
19. C.Vivek, S.Palanivel Rajan, "Z-TCAM : An Efficient Memory Architecture Based TCAM", Asian Journal of Information Technology, ISSN No.: 1682-3915, Vol. No.: 15, Issue : 3, pp. 448-454, DOI: 10.3923/ajit.2016.448.454, 2016.
20. AN-2040 Output Voltage Clamping Using the LM5069 Hot Swap Controller.
21. Vosough and Vosough (November 2011). "PLC and its Applications"
22. Erickson, Kelvin T. (1996). "Programmable logic controllers" Institute of Electrical and Electronics Engineers.

ISSN: 2233-7857 IJFGCN

23. S.Vijayprasath, R.Sukanesh, S.Palanivel Rajan, “Assessment of relationship between heart rate variability and drowsiness of post operative patients in driving conditions”, JoKULL Journal, ISSN No.: 0449-0576, Vol. 63, Issue 11, pp. 107 – 121, 2013.
24. Paranthaman, M., and S. Palanivel Rajan. "Design of Triple C shaped Slot Antenna for Implantable Gadgets." Current Trends In Biomedical Communication And Tele–Medicine (2018): 40. DOI: 10.21786/bbrc/11.2/6
25. S.Palanivel Rajan, R.Sukanesh, S.Vijayprasath, “Design and Development of Mobile Based Smart Tele-Health Care System for Remote Patients”, European Journal of Scientific Research, ISSN No.: 1450-216X/1450-202X, Vol. No. 70, Issue 1, pp. 148-158, 2012.
26. M. Paranthaman, "T-shape polarization reconfigurable patch antenna for cognitive radio," 2017 Third International Conference on Science Technology Engineering & Management (ICONSTEM), Chennai, 2017, pp. 927-929. doi: 10.1109/ICONSTEM.2017.8261338
27. S.Palanivel Rajan, R.Sukanesh, S.Vijayprasath, “Analysis and Effective Implementation of Mobile Based Tele-Alert System for Enhancing Remote Health-Care Scenario”, HealthMED Journal, ISSN No. : 1840-2291, Vol. No. 6, Issue No. 7, pp. 2370–2377, 2012.
28. Jim Williams (March 1, 1989) "High Efficiency Linear Regulators". Linear Technology retrieved 2014-03-29.
29. Pithadia, Sanjay. "LDO PSRR Measurement Simplified" Texas Instruments on 2012-10-22.
30. Specific Absorption Rate (SAR) For Cell Phones"Federal Communications Commission retrieved 2013-12-22.
31. M.Annakamatchi, V.Keralshalini," Design of Spiral Shaped Patch Antenna for Bio-Medical Applications", International Journal of Pure and Applied Mathematics , Online ISSN No.: 1314-3395,Print ISSN No.:1311-8080 ,Vol. No.:118, Issue No.:11,pp.131-135,2018.
32. S.Palanivel Rajan, “A Significant and Vital Glance on “Stress and Fitness Monitoring Embedded on a Modern Telematics Platform”, Telemedicine and e-Health Journal, Vol.20, Issue 8, pp.757-758, 2014.
33. S.Palanivel Rajan, T.Dinesh, “Systematic Review on Wearable Driver Vigilance System with Future Research Directions”, International Journal of Applied Engineering Research, Vol. 2, Issue 2, pp.627-632, 2015.
34. S.Palanivel Rajan, S.Vijayprasath, “Performance Investigation of an Implicit Instrumentation Tool for Deadened Patients Using Common Eye Developments as a Paradigm”, International Journal of Applied Engineering Research, Vol.10, Issue 1, pp.925-929, 2015.
35. M.Manikandan,N.V.Andrews, V.Kavitha, “Investigation On Micro Calification Of Breast Cancer From Mammogram Image Sequence” International Journal of Pure and Applied Mathematics, Online ISSN No.: 1314-3395, Print ISSN No.: 1311-8080, Vol. No.: 118, Issue No.: 20, pp. 645-649,2018.
36. Analog Devices (2009). "Op Amp Input Bias Current" Analog Devices tutorial MT-038.
37. Op Amp Output Phase-Reversal and Input Over-Voltage Protection" . Analog Devices 2009 retrieved 2012-12-27.

ISSN: 2233-7857 IJFGCN