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Design of Novel PMOS and NMOS for High Speed Applications

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Abstract: This paper sews Novel PMOS and NMOS for high-speed applications, standard PMOS and NMOS combined called CMOS have been the dominant technology for the past decade, using the concept of pre-existing bias threshold voltage can be reduced when speed can be reached there. improvement and delays are reduced. The product of the power delay is a statistical value of any digital design .in this paper novel PMOS and NMOS novel are combined together it is called a novel inverter is designed and the transmitted components are researched by 180nm technology
Keywords: Power Delay Product, Threshold Voltage, Forward Body Biasing, Reverse Body Biasing, Body Coefficient.

1. Introduction

Normal PMOS and NMOS are widely used as they take up less space and lower power dissipation .Large PMOS and NMOS limitations are the result of low speed and short channel, these two limitations can be resolved using Novel PMOS [1] and Novel. NMOS. The threshold voltage of the device can be changed (changed) by the following techniques a) Gate protection equipment b) doping station c) Gate conductor object d) voltage difference between source and body, would be advantageous if the threshold voltage was an independent machine. [2] and the flexible design parameter, the active bias used to control the threshold voltage by changing the bulk power of the transistor, the negative bulk to source voltage (VBS) of the NMOS transistor increases the width of the bulk reduction layer and increases the threshold voltage [3] and the positive mass at the source voltage reduces the width of the reduction layer and lowers the threshold voltage. The first case is known as reverse bias and the latter case is progressive bias. The threshold voltage change of NMOS due to the mass change in the source voltage is given by $\Delta vth = \gamma (x)$ due to the dependence of the square root. it is clear that the threshold voltage is more sensitive to more FBB power than the RBB with the same change in multiple power, thus the decrease [v] of vth due to further bias is greater than the increase in vth due to distorted body bias. , usually from libraries to meet the time we use vth cells lower and higher and more expensive, but in this process from the same libraries we can get vth cells lower and higher.

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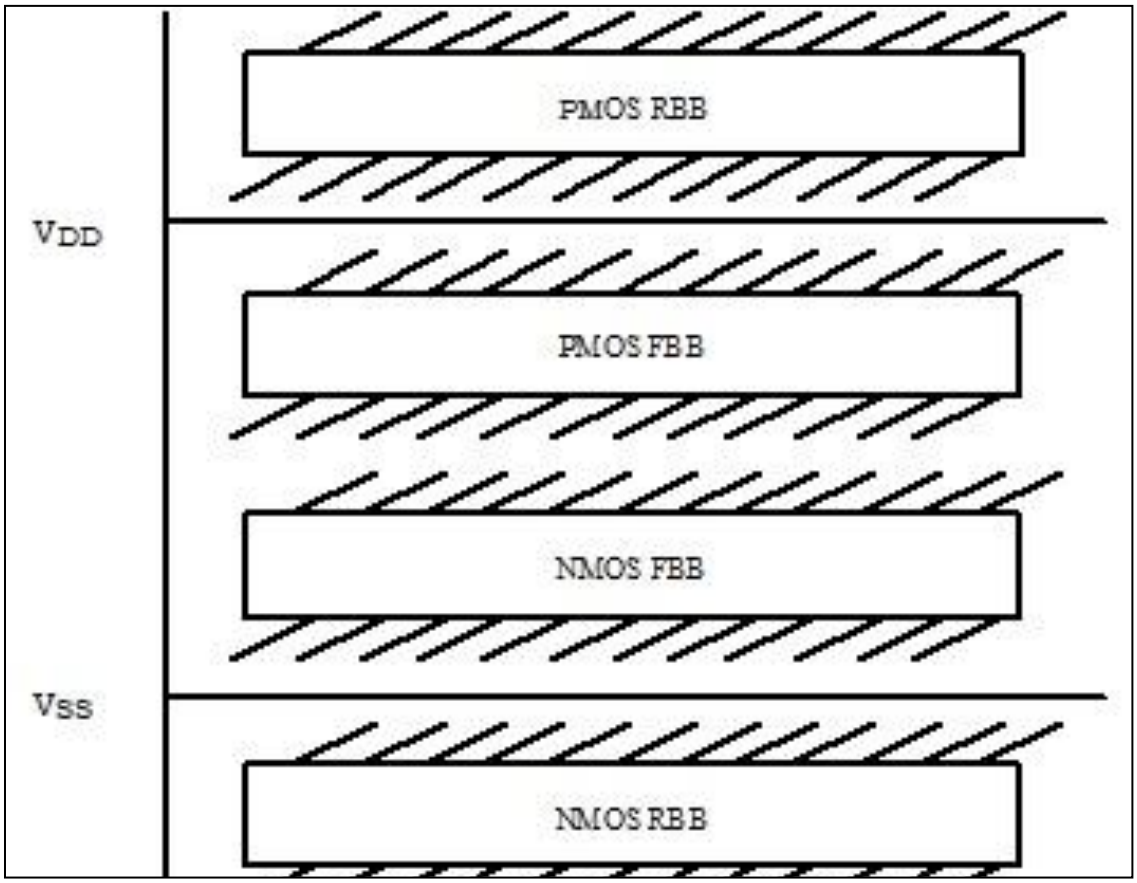


Figure.1. Forward body biasing and reverse body biasing for PMOS and NMOS

In Fig.1 of PMOS when the substrate / body voltage is greater than V_{dd} it is called reverse body biasing where the threshold voltage can be increased, if the substrate or body voltage is below V_{dd} it is called bias [5] body where the threshold voltage can be. slow down and speed can be increased. In NMOS if the substrate / body voltage is greater than V_{ss} it is called forward bias where the threshold voltage can be reduced and the speed can be increased, if the substrate or body voltage is below V_{SS} the body is biased and Vth goes up.

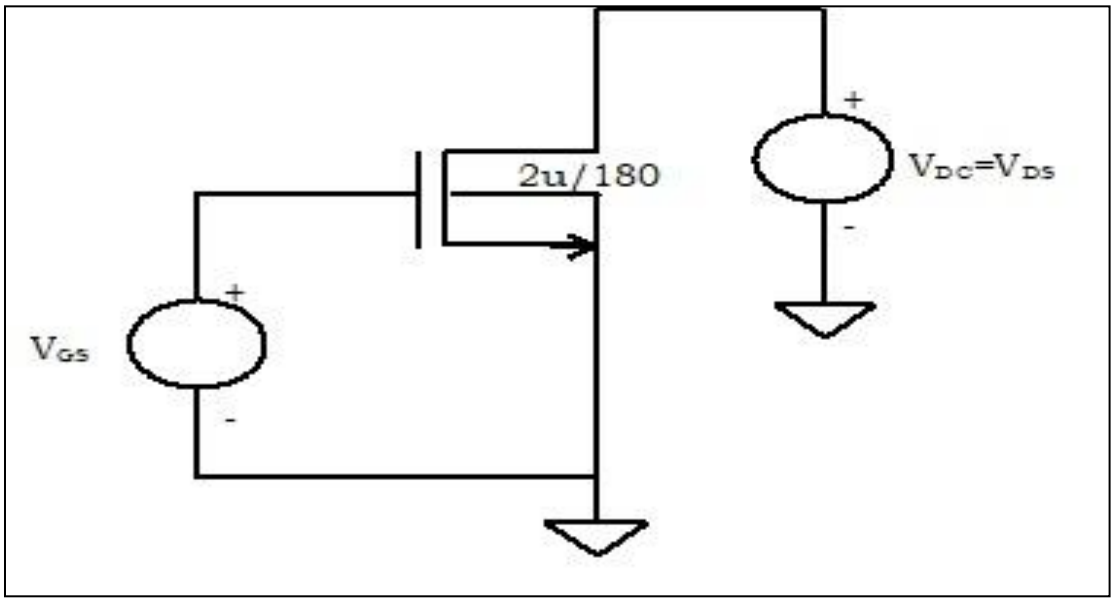
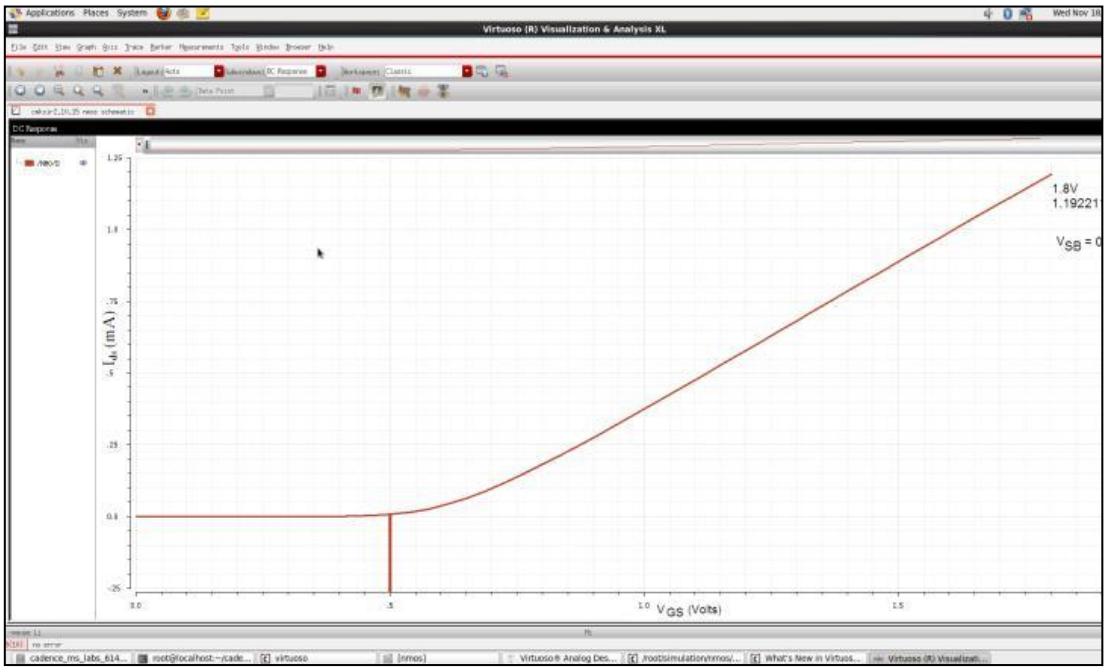


Figure.2. Conventional NMOS

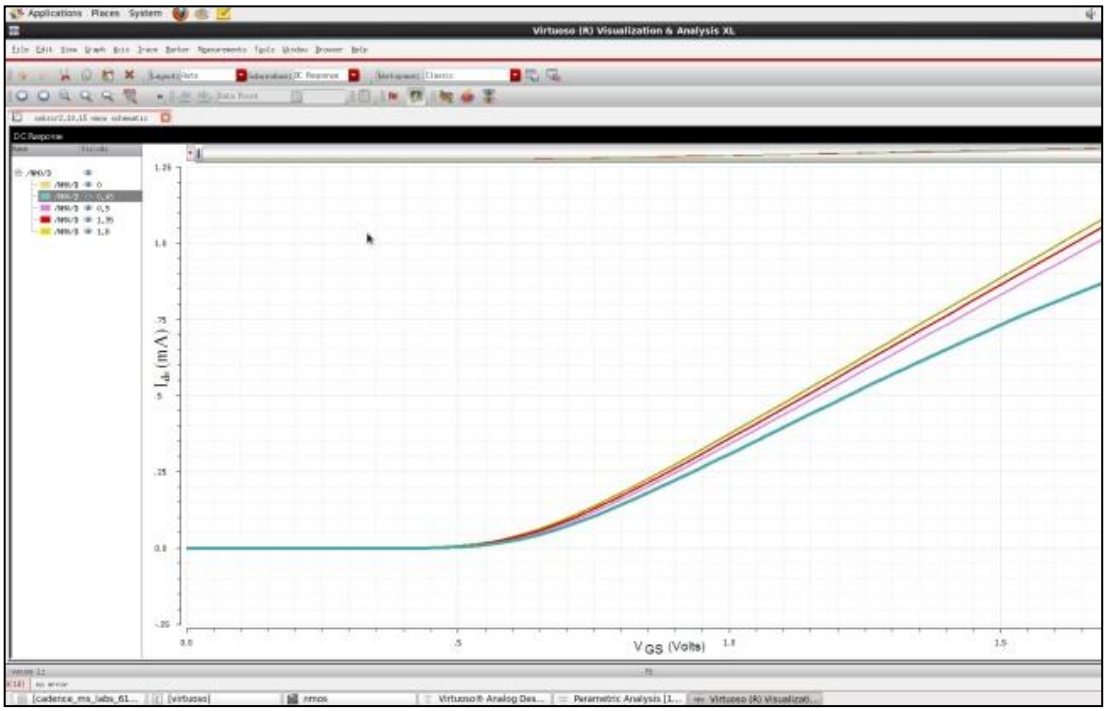
In Fig.2 the source and body tied together and there is no body effect, Fig.3 below shows VGS verses I_{ds} characteristics where $V_{SB} = 0$ and its observed that threshold voltage is 0.5 Volts.



$V_t = 0.5V$ $V_{SB} = 0$

Figure.3. Conventional NMOS V_{gs} verses I_{ds} characteristics

Below Fig.4 conventional NMOS V_{GS}versus I_{ds} characteristics for different V_{DS} Values



$V_t = 0.5V$ $V_{SB} = 0$

Figure.4. Conventional NMOS V_{GS} verses I_{ds} characteristics

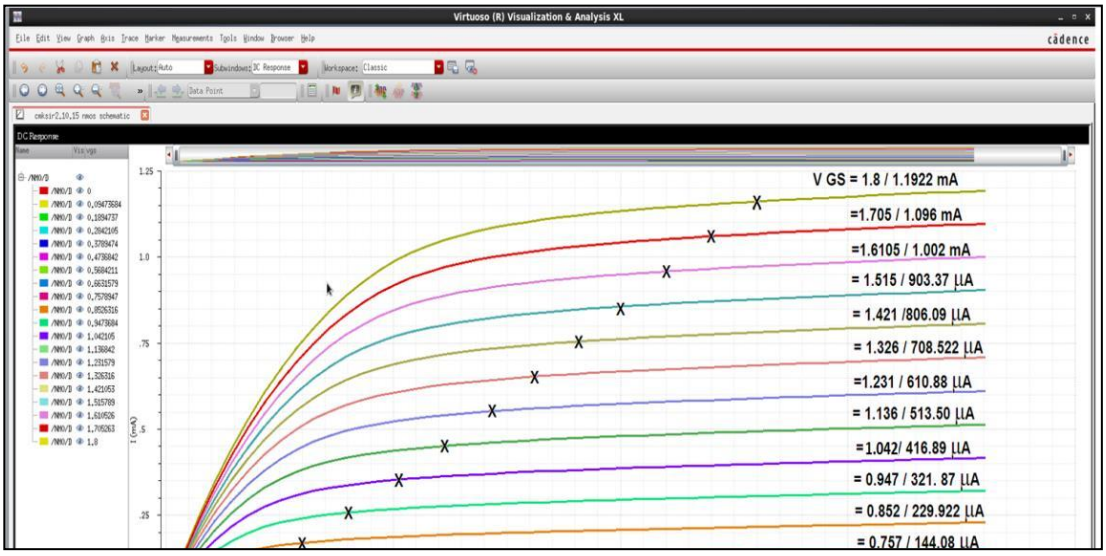


Figure.5. Conventional NMOS V_{DS} verses I_{ds}

Fig.5 shows a conventional NMOS Vds versus I_{DS} for different values of V_{gs} and region[6] of operations are shown $V_{gs} \leq V_T$ where I_{DS} is zero is called cut-off region, $V_{gs} \geq V_T$ and $V_{DS} \leq V_{gs} - V_T$ is called ohmic region or triod region.

2. Propoed NMOS

Fig. 6 shows the proposed NMOS. NMOS VGS novel against I_{ds} ¬in Fig. 7 and Fig.8, from these factors it is found that the threshold voltage of the device is 0.4 volts. At VSB 0.22 volts, due to pre-body bias the threshold voltage decreases from 0.5 volts to 0.4 volts, where the speed can be improved. Fig.9 shows the novel NMOS VDS when compared to I_{ds} features and operating region [8] such as ohmic circuit, area fullness and cut-off regions are shown.

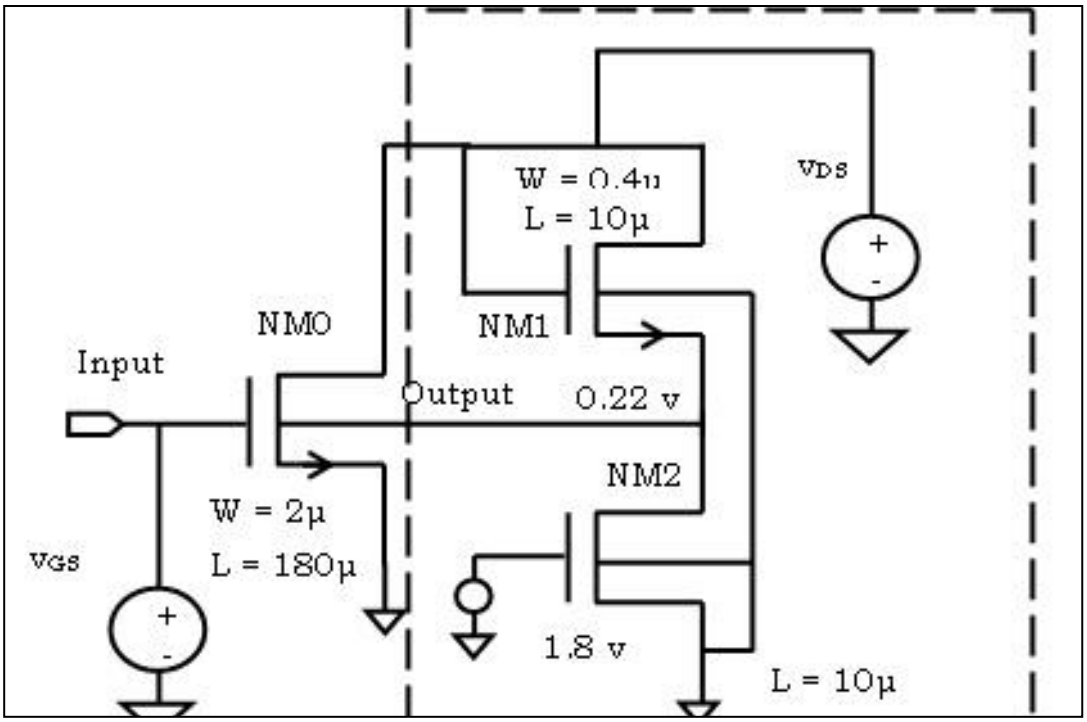
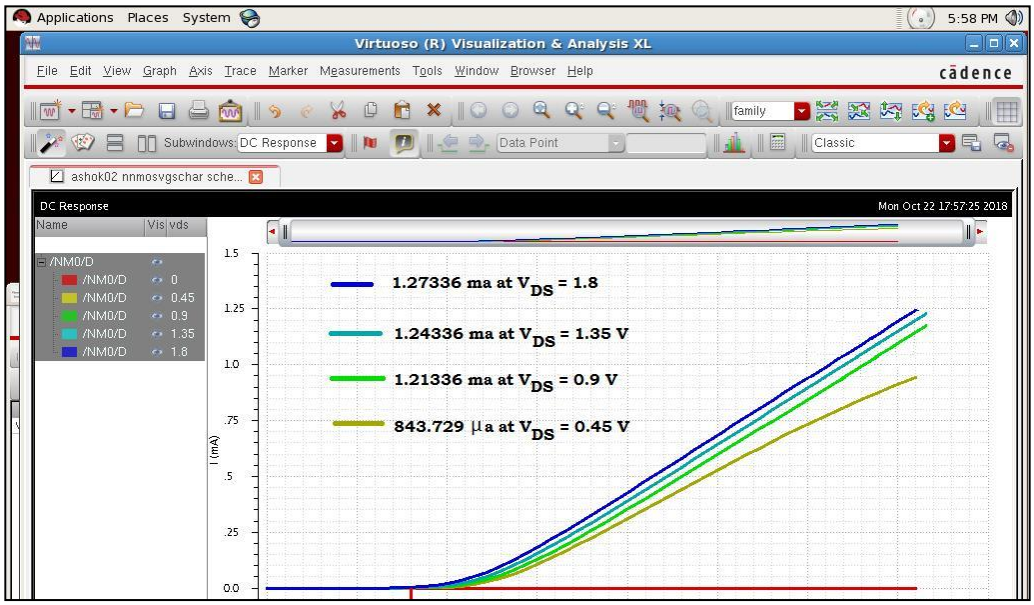


Figure.6. Proposed NMOS

Fig. 6 shows the proposed NMOS. NMOS VGS novel against I_{ds} ¬in Fig. 7 and Fig.8, from these factors it is found that the threshold voltage of the device is 0.4 volts. At VSB 0.22 volts, due to pre-body bias the threshold voltage decreases from 0.5 volts to 0.4 volts, where the speed can be improved. Fig.9 shows the novel NMOS VDS when compared to I_{ds} features and operating region [8] such as ohmic circuit, area fullness and cut-off regions are shown.



Vt = 0.4V V_{SB} = 0.22v

Figure.7. Novel NMOS V_{GS} verses I_{ds} characteristics

Figure.8. Novel NMOS V_{DS} verses I_{ds} characteristics

Fig.8 above shows the proposed NMOS V_{GS} compared to the I_{ds} features of different V_{DS} values. The current percentage increase due to a decrease in threshold voltage from 0.5 volts to 0.4 volts from VSB = 0.2 volts.

((1.27336 – 1.192211)/1.192211) x 100 = 6.80%

Percentage Decrease in Threshold voltage from 0.5v to 0.4v is

$$\%V_{TH} = \frac{0.4 - 0.5}{0.5} \times 100$$

$$\%V_{TH} = -20\ \%$$

20% decrease in threshold voltage raised 6.80% in current

3.Propoed PMOS

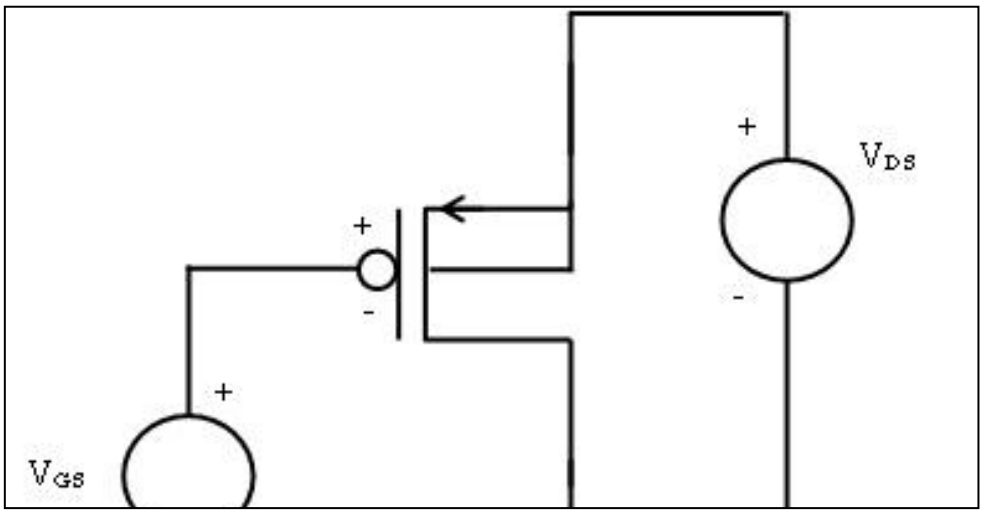


Figure.9. Conventional PMOS

Fig.9 shows normal PMOS where the source and body are connected [9] and there is no body bias. Fig.10 shows the common features of PMOS V_{gs} against I_{ds}. From the features it is noted that the threshold voltage of the device is 0.5 volts, and Fig.11 shows V_{DS} compared to I_{ds} features of different V_{GS} values.

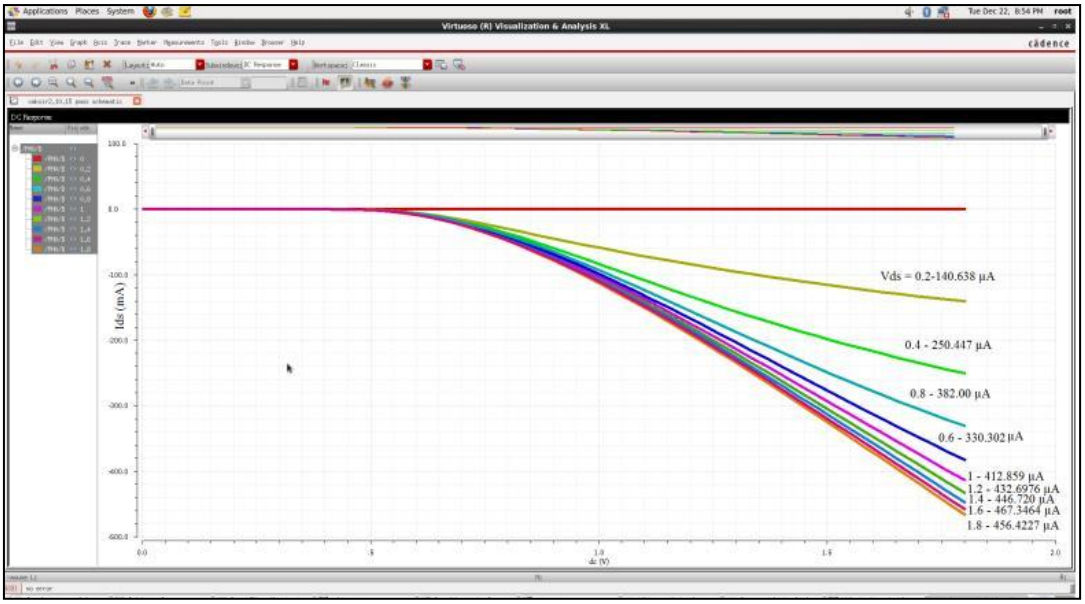


Figure.10. Conventional PMOS V_{GS} verses I_{ds}

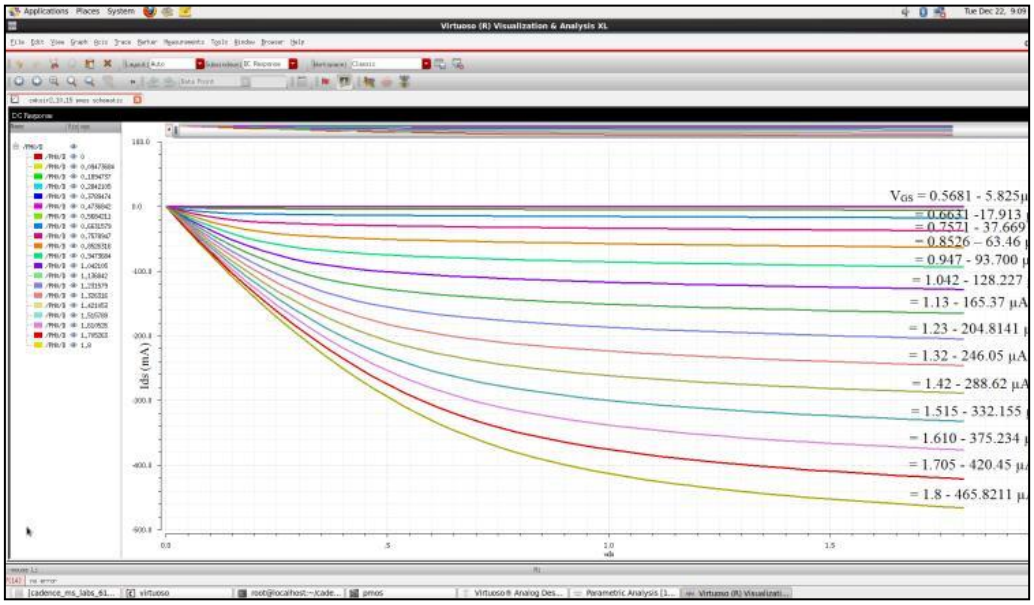


Figure.11. Conventional PMOS V_{DS} verses I_{ds}

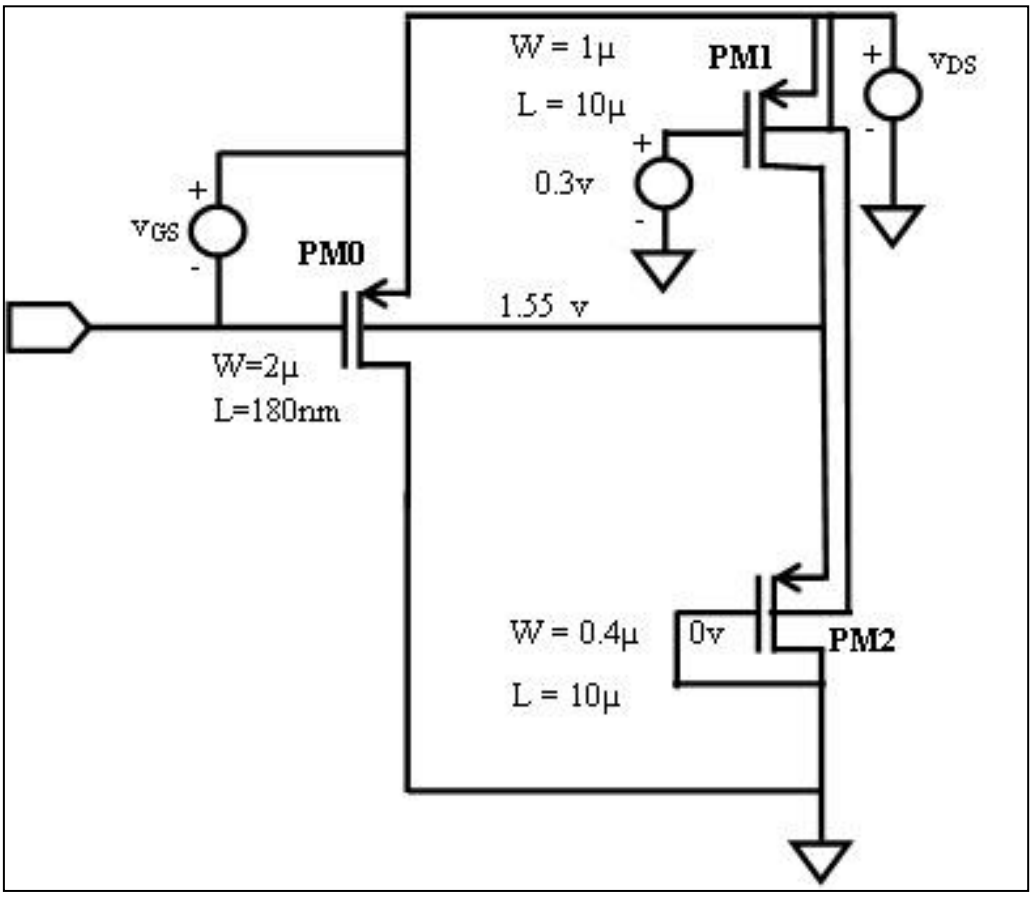


Figure.12. Novel PMOS

Fig.12 shows the PMOS novel when using the previous bias, Fig.13 shows the PMOS V_{GS} novel versus I_{ds} features, from features that detect threshold voltage reduced [10] from 0.5 volts to 0.4 volts. Delays can be reduced and speed can be increased. Fig.14 shows V_{DS} compared to I_{ds} features of different V_{GS} values.

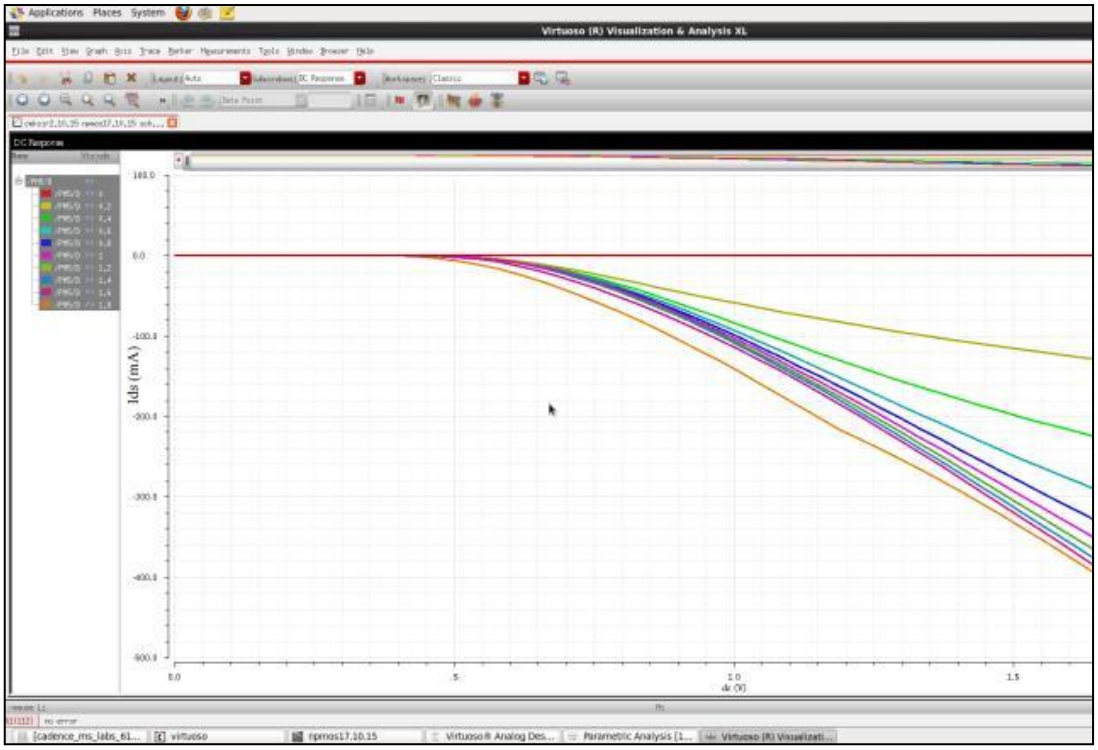


Figure.13. Novel PMOS V_{GS} verses I_{ds}

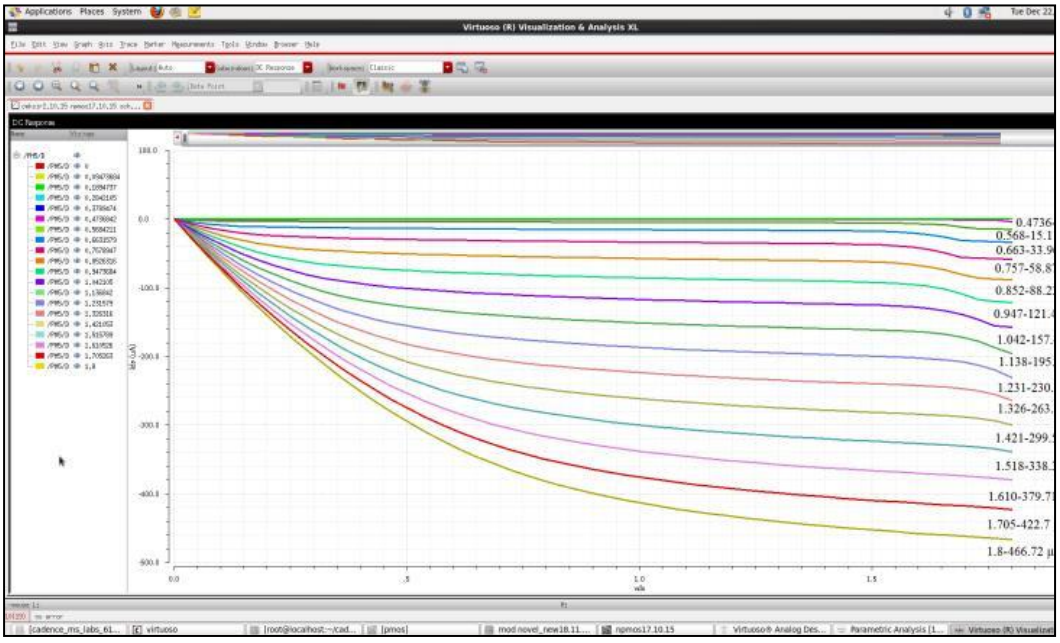


Figure.14. Novel PMOS V_{DS} verses I_{ds}

3. Propoed CMOS Inverter

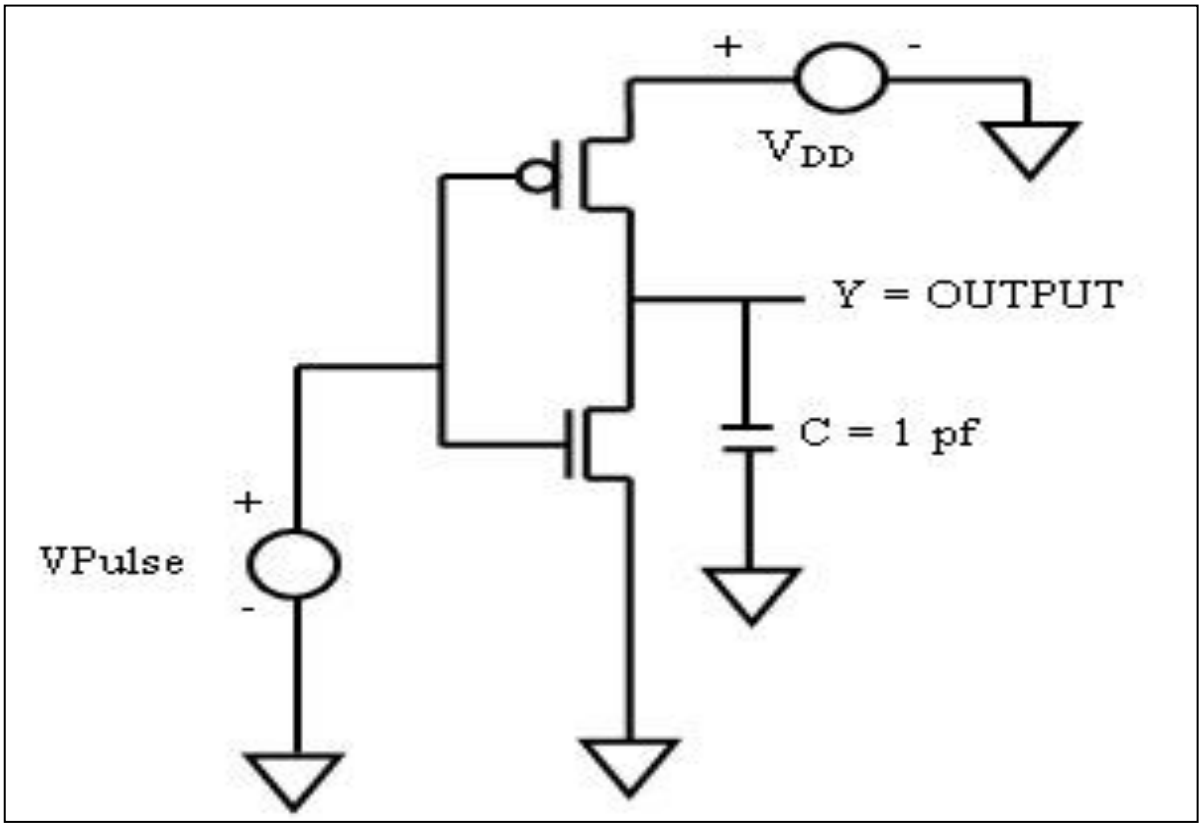


Figure.15. Conventional CMOS İnverter

Fig.16 below shows a conventional CMOS inverter Input verses Output characteristics

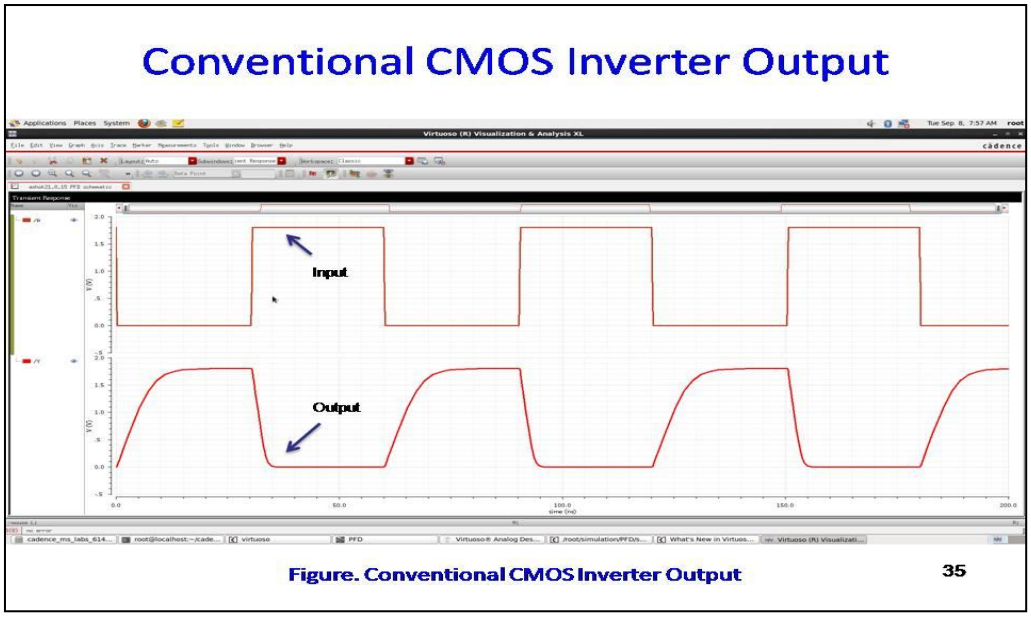


Figure.16. Conventional CMOS inverter input versus output

Fig. 17 shows the novel CMOS inverter and the input features compared to the output shown in Fig.19 and Fig.20 shows the transmission characteristics of the novel inverter [12] and the audio genes are calculated at 0.45, since both the common converter and the novel converter it is noted that the novel converter will have better audio genes compared to the standard CMOS converter [13].

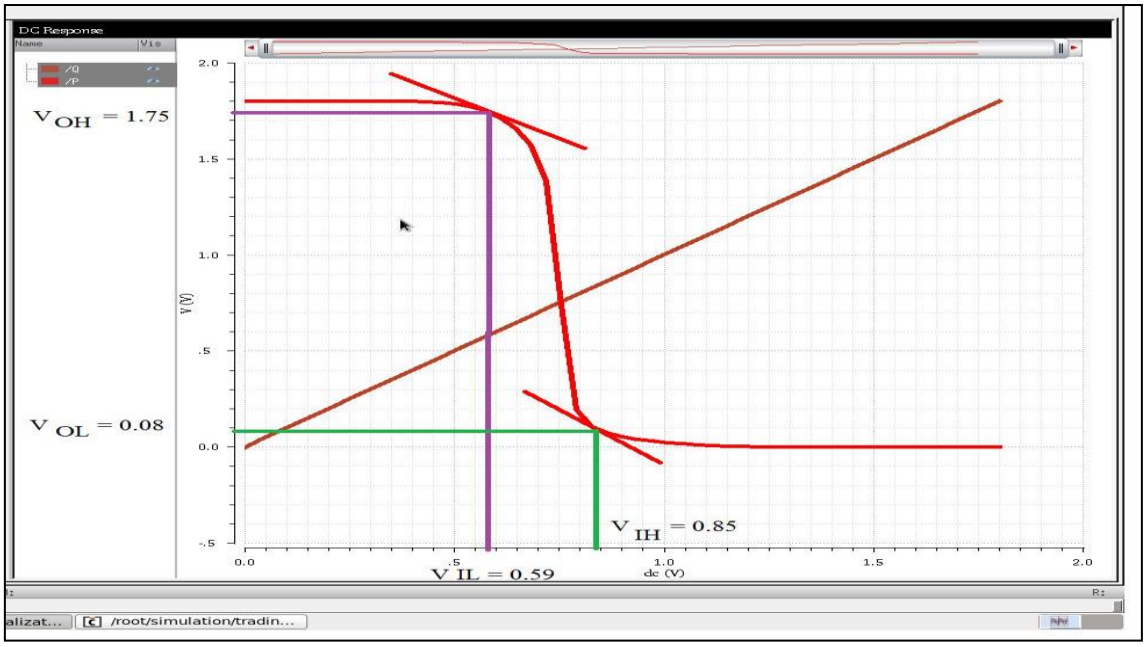


Figure.17. Conventional inverter transfer characteristic**s**

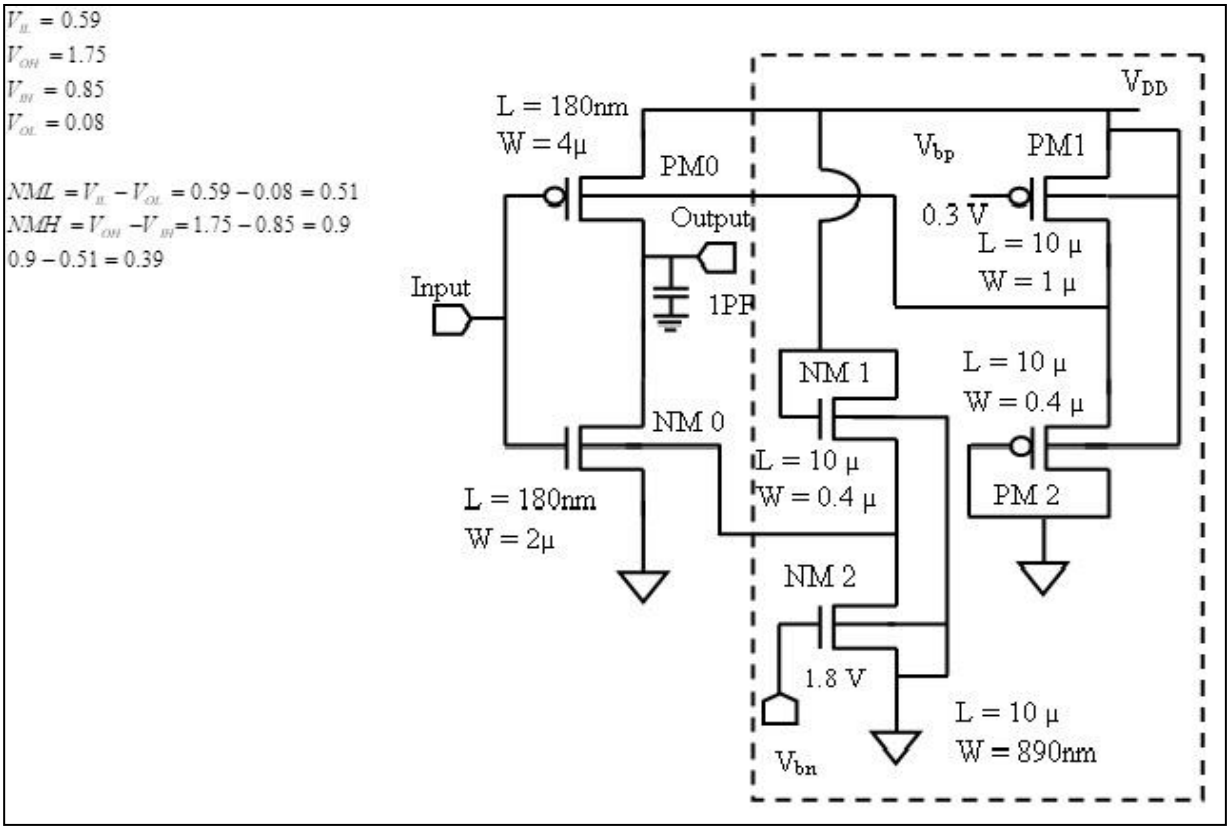


Figure.18. Proposed CMOS inverter

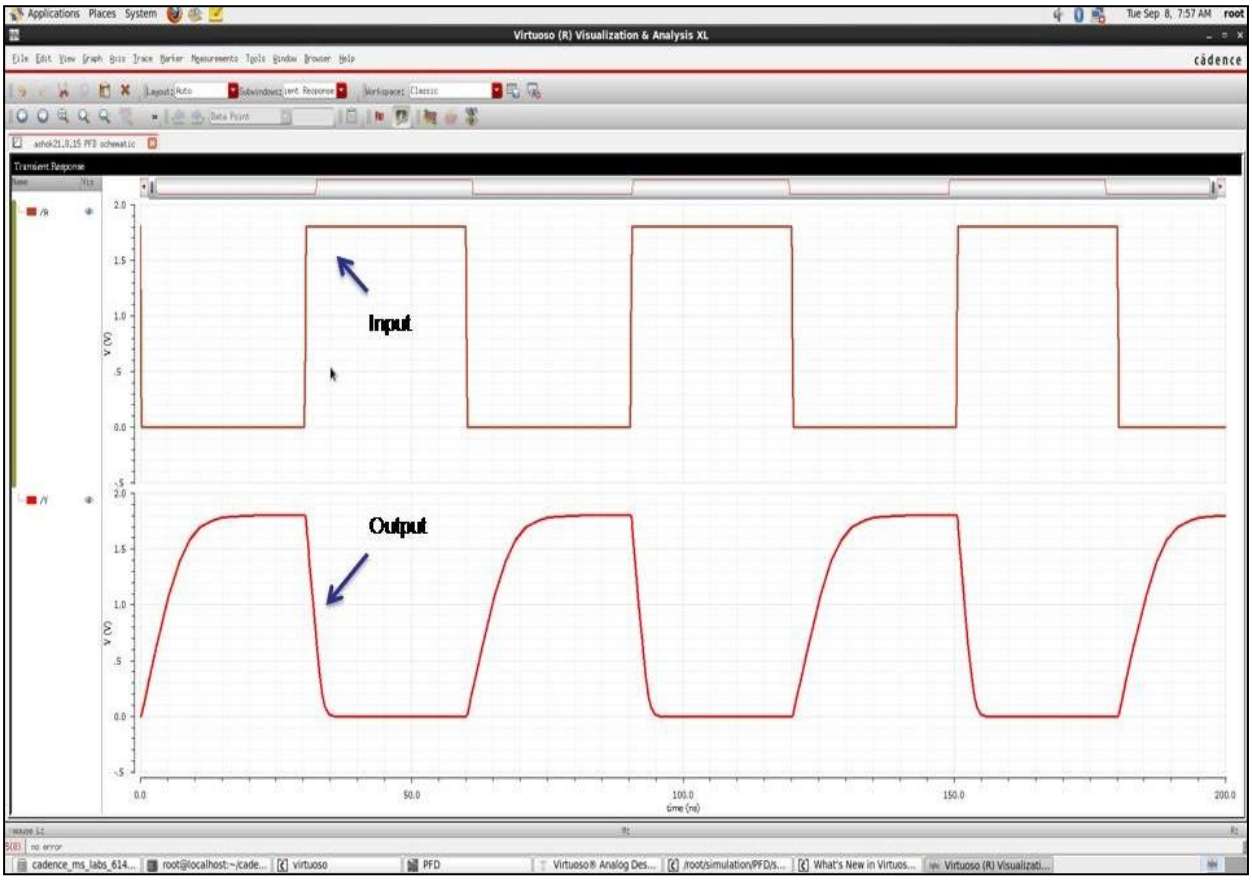


Figure.19. Proposed CMOS inverter input versus output

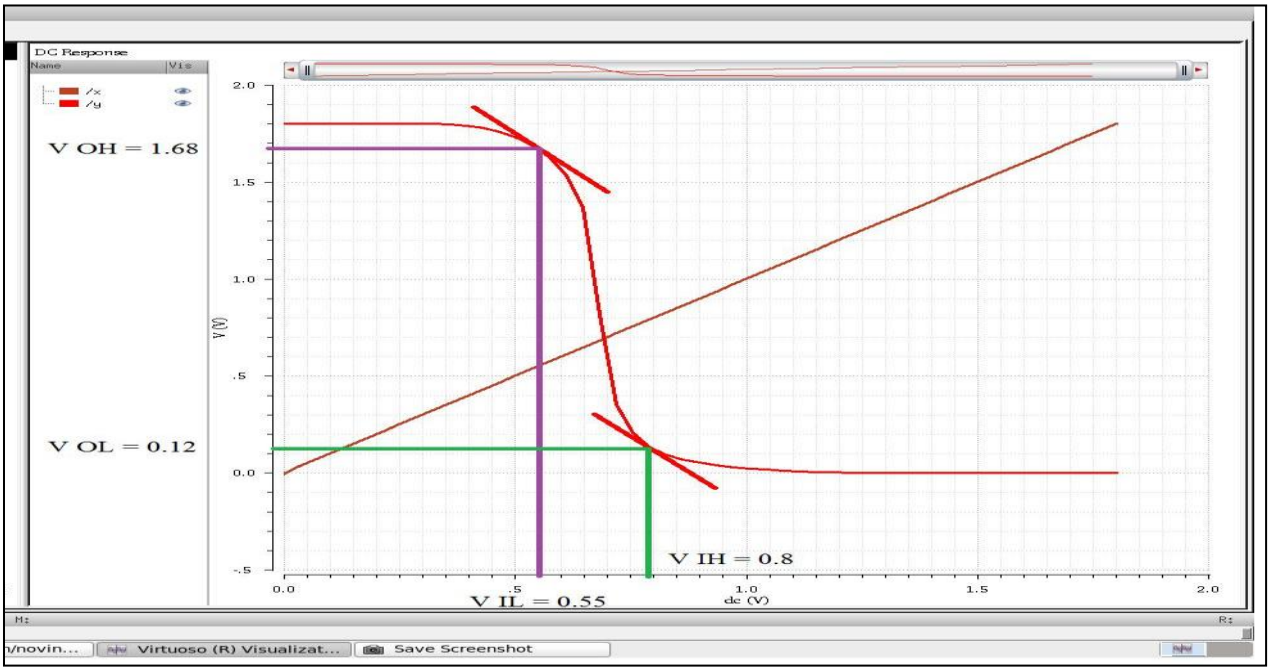


Figure.20. Novel İnverter Transfer Characteristics

$V_{IL} = 0.55$

$V_{OH} = 1.68$

$V_{IH} = 0.8$

$V_{OL} = 0.12$

$NML = V_{IL} - V_{OL} = 0.55 - 0.12 = 0.43$

$NMH = V_{OH} - V_{IH} = 1.68 - 0.8 = .88$

$0.88 - 0.43 = 0.45$

The improvement in the noise margin of proposed inverter is

$$\frac{0.45 - 0.39}{0.39} \times 100 = 15.38\ \%$$

4. Conclusıon

This paper examines the features of the proposed PMOS and NMOS and discusses the benefits of pre-existing Bias and its effects, using advanced Bias the device limit voltage decreases from 0.5v to 0.4v , speed improves and improved noise margin of proposed inverter is 15.38% , the benefits of the novel PMOS and NMOS come from the same library we can find low v^{th} cells and high v^{th} cells where costs can be saved, the concept of Novel PMOS and NMOS is applied to the inverter and the novel inverter is built and their audio parameters learned.

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