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Vedic Multiplier

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Abstract- *The principle reason for the venture is to improve the speed of the computerized circuits like multiplier since adder and multiplier are one of the key equipment parts in superior frameworks like microchips, advanced sign processors and FIR filters and so forth Consequently we generally go after great multiplier design to expand the productivity and execution of a framework. Vedic multiplier is one such fast multiplier architecture. This 'Vedic Mathematics' name is based on the techniques used for calculations which are depended on some of principles and rules, by using these any of problems can be solved in arithmetic, algebra, geometry or trigonometry. Vedic Multiplier plays a significant role in the processors. The Vedic mathematic requires more processing time as compared to other mathematic operations on system. Vedic mathematic is the old Indian arrangement of mathematic. It has a novel strategy of calculations dependent on 16 Sutras. UrdhvaTiryagbhyam is the increase sutra between these 16 sutras, which implies vertical and crosswise.*

Keywords- Multiplier, Vedic,*Urdhva Tiryagbhyam****,Calculations, Adder***

I. INTRODUCTION

Multiplication is the main math activity in signal processing applications and inside the Processor. As speed is consistently a significant prerequisite in the augmentation activity, speed up can be accomplished by diminishing the quantity of steps in the calculation cycle. The speed of multiplier decides the productivity of such a framework. In any framework plan, the three principle limitations which decide the exhibition of the framework are speed, region and force necessity. Vedic math was reproduced from the antiquated Indian sacred texts (Vedas) by Swami Bharati Krishna Tirthaji Maharaja after his eight years of exploration on Vedas. Vedic science is for the most part dependent on sixteen standards or word-formulae which are named as sutras. This is a fascinating field and presents some compelling calculations which can be applied to different parts of designing like digital signal processing and computing. Coordinating augmentation with Vedic Mathematics methods would bring about the saving of computational time.

Multiplication is a significant key capacity in number-crunching tasks. Multiplication based activities like Multiply and Accumulate(MAC) and inward item are among a portion of the often utilized Computation-Intensive Arithmetic Functions(CIAF) presently executed in numerous Digital Signal Processing (DSP) applications like convolution, Fast Fourier Transform(FFT), sifting and in chip in its number juggling and rationale unit. Since augmentation overwhelms the execution season of most DSP

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calculations, so there is a need of fast multiplier. At present, Multiplication time is as yet the prevailing variable in deciding the guidance process duration of a DSP chip. In numerous DSP calculations, the multiplier lies in the basic defer way and eventually decides the exhibition of calculation. The speed of Multiplication activity is critical in DSP just as in everyday processor. In the past Multiplication was carried out by and large with a grouping of expansion, deduction and shift activities. There have been numerous calculations recommendations in writing to perform Multiplication, each offering various benefits and having tradeoff as far as speed, circuit intricacy, and region and force utilization.

In this, Urdhvatiryakbhyam Sutra is first applied to the parallel number framework and is utilized to foster advanced multiplier design. This is demonstrated to be basically the same as the famous exhibit multiplier engineering. This Sutra additionally shows the adequacy of to decrease the NXN multiplier structure into a productive 4X4 multiplier structures. Nikhilam Sutra is then examined and is demonstrated to be substantially more productive in the Multiplication of enormous numbers as it decreases the Multiplication of two huge numbers to that of two more modest ones. The proposed augmentation calculation is then delineated to show its computational productivity by taking an illustration of decreasing a 4X4-bit Multiplication to a solitary 2X2-cycle Multiplication activity. This work presents a deliberate plan approach for quick and region effective digit multiplier dependent on Vedic arithmetic .The Multiplier Architecture depends on the Vertical and Crosswise calculation of old Indian Vedic Mathematics.

Previously, the boundaries like fast, little region and minimal expense where the significant spaces of concern, though power thought are presently acquiring the consideration of mainstream researchers related the VLSI plan. With the development innovation interest for fast and versatile advanced sign preparing framework is expanded. Multiplier is widely utilized in advanced sign preparing because of its quickest developing innovation. Presently a day advanced sign preparing is available in each specialized field. DSP assists with doing quickest augmentation and expansion tasks. The antiquated arrangement of Vedic science was rediscovered from the Vedas between the year 1911 and 1918 by Sri Bharati Krishna Tirthaji. This strategy is completely founded on 16 sutras in this paper we will talk about the design dependent on Urdhavatiryakbhyamin which in an upward direction and across numerical activity is performed by the sutra is introduced. The paper presents the fundamental rationale for 4x4 multiplier and the execution of it with less equipment utilized. Augmentation having wide application in various spaces of designing innovation and in advanced frameworks stalls calculation and exhibit calculation are the best calculation use for Multiplication tasks and different strategies incorporate Vedic multipliers dependent on "urdhvatiryakbhyam". Computerized multipliers are the most ordinarily utilized segments in any advanced circuit plan. They are quick and effective parts that are utilized to carry out. In light of the course of action of the modules, there are different sorts of multipliers exists. Reasonable multiplier engineering is picked for this application. The Vedic science is extremely straightforward, standard just as sensible. Its serious level of distinction is credited to the previously mentioned realities. It is these exceptional attributes, which made Vedic science, become so famous and hence it has gotten one of the main subjects of exploration in India as well as abroad too. Vedic arithmetic's rationales and steps can be straightforwardly applied to issues including geometrical capacities, plane and circle calculation, differential analytics, vital analytics and applied math of different kind.

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II. Literature Survey

The Vedic multiplier circuit is executed by utilizing GDI procedure and furthermore 18nmFinFET is conveyed for investigating reproduction results. Here, the essential goal is to upgrade the proposed multiplier hardware, where a trial investigation is led by containing the boundaries, for example, engendering Delay, Power, Area and Power-Delay-Product (PDP). All test examination is finished utilizing Cadence Virtuoso. [1]

The proposed strategy was planned and carried out in Verilog HDL. For HDL recreation, model sim device is utilized and for circuit combination, Xilinx is utilized. The recreation has been accomplished for 4 bit, 8 bits, 16 bit, 32 digit increase activity. Just for 32 digit twofold vedic multiplier procedure the reproduction results are appeared. This adjusted increase method is stretched out for bigger sizes. The results of this increase procedure is contrasted and existing vedic multiplier methods. [2]. The Vedic multiplier has a quickest number-crunching activity and less intricate than a multiplier. The Vedic multiplier is utilized to improve on the augmentation interaction and deferral. In the event that the Vedic multiplier is planned by utilizing CMOS semiconductors, the circuit will raise issue. To beat this issue, the Gate Diffusion Input (GDI) rationale has been executed in this paper utilizing FinFET innovation. Here, GDI rationale is utilized to diminish the semiconductor tally of the circuits. Nonetheless, in these interaction, two kinds of configuration approaches are thought of. The primary sort approach intends to carry out the 4-bit Vedic multiplier (Design 1) utilizing GDI based AND, half viper, and full snake circuits. Second sort approach is planned to plan a 4-bit Vedic multiplier (Design 2) by utilizing GDI based 2-bits Vedic multiplier, half snake and 4-bit Ripple convey circuits. In these, the circuit execution factors like normal force, postponement and semiconductor tally, and circuit region are thought of. [3]. Two plan approaches are mulled over. The exhibition of these circuits is investigated as far as normal force dispersal, postponement, and TC. The impact of supply voltage scaling is additionally examined. The circuit reproductions are completed at 130 nm for mass metal oxide semiconductor field impact semiconductor prescient innovation model-based gadget boundaries. [4].

8-bits Vedic multiplier is proposed utilizing changed Gate Diffusion Input (mGDI). 8-digit Vedic multiplier is planned utilizing UrdhvaTiryagbhyam sutra with 4 quantities of 4-bit Vedic multiplier and 3 viper circuits. The proposed mGDI based multiplier devours 66% less region, 76.1% less force and 60% less postpone when contrasted with ordinary CMOS plan. The proposed multiplier is carried out in rhythm virtuoso instrument on 180nm innovation. [5].

III. Implementation Details of Module

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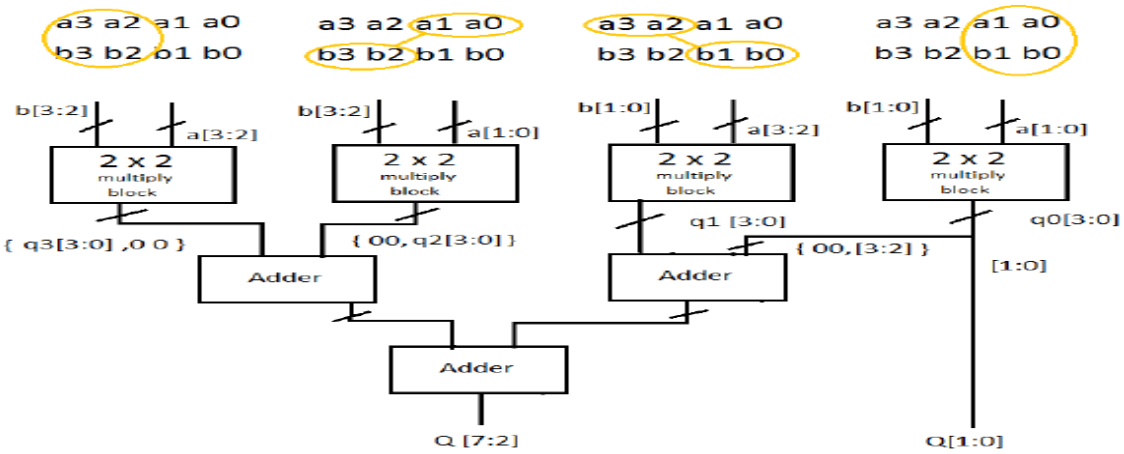

Fig. 1 System Architecture

In this paper we implement a Vedic multiplication technique which is based on "Urdhva-Tiryakbhyam – Vertically and crosswise" sutra. Vedic multiplier technique consists of generation of parallel partial products and addition operation simultaneously .This algorithm can be used for 2×2, 4×4, 8×8, 16×6....N×N bit multiplications. In this method sum and their partial products are calculated in parallel hence Vedic multiplier does not depend upon the processor clock frequency and reduces the power dissipation. The use of "Urdhva-Tiryakbhyam sutra" for multiplication operation reduces the latency of a multiplier unit by introducing concurrent computing of partial products. The main advantage of the Vedic multiplier is that it reduces delay as well as power when compared with the exiting multipliers. S0 is obtained by multiply the least significant bits of the multiplicand and multiplier. Numbers on both sides of the line are multiplied and added with carry from previous step in the last case. This generates one of the bits of the result sum and a carry. This carry is added in the next step hence the process goes on.

Model SIM Execution Method

•Graphical User Interface (GUI)
•Can accept menu input and command line input
•Main discussion of class
•Interactive Command Line (Cmd)
•Only interface is a command line console, no User Interface
•TCL Scripts and ModelSim Macros
• TCL – Industry standard scripting language
•Macros (DO files) – easily created from main window transcripts (GUI commands write equivalent Cmd functions to main window)

Basic Simulation Steps

Step 1 ⇨ Create library(s)
Step 2 ⇨ Map library to physical directory

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Step 3 ⇨ Compile source code
All HDL Code must be compiled
Different for Verilog and VHDL
Step 4 ⇨ Start simulator and load top-level design unit
Step 5 ⇨ Advance simulator

IV. RESULTS

The adder-cell is the most basic part of Vedic Multiplier. It consists of

1. Adder 1
2. Adder 2
3. Vedic Multiplier

All these components are implemented in VHDL

Ripple Adder

To obtain final result outputs of all carry save adders Ci and Si are added using Ripple Carry Adder.

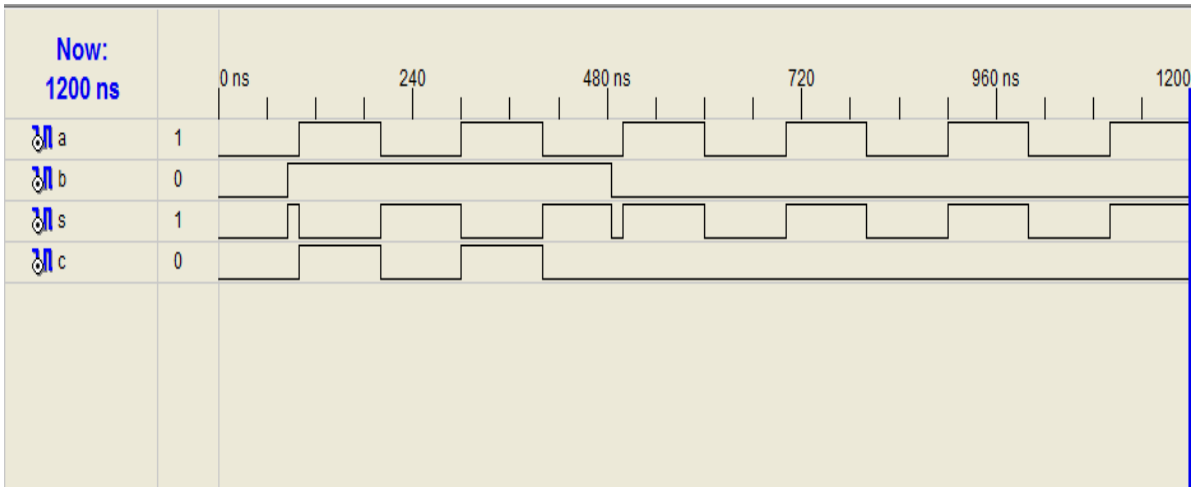

Fig. 2 Test Bench waveforms for Adder 1

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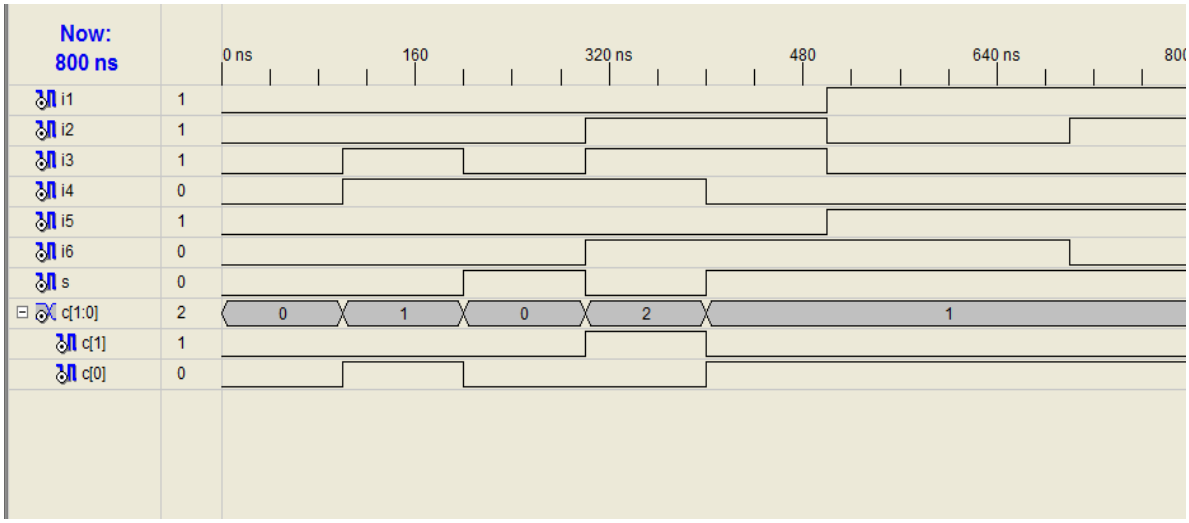

Fig. 3 Test Bench waveforms for Adder 2

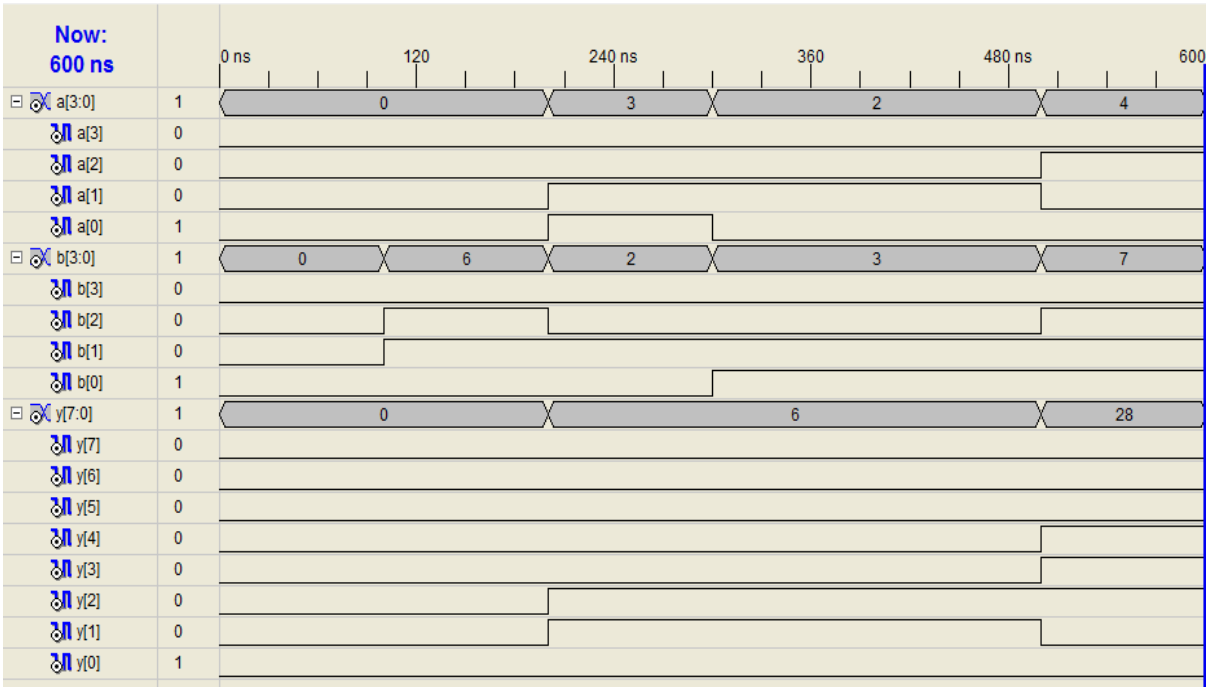

Fig. 4 Test Bench waveforms for Vedic Multiplier

V. CONCLUSION

In paper presents a novel way of realizing a high speed multiplier using UrdhvaTiryagbhyam sutra. A 4-bit modified multiplier is designed by using the proposed 4 bit adder. The proposed 4x4 multiplier gives a total delay of 12.825 ns which is less when compared to the total delay of existing multiplier architecture. Results also indicate a 13.19% increase in the speed when compared to normal Vedic multiplier. Our design more preferable over all other designs.

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REFERENCES

[1] MaltiBansal and Jasmeet Singh, "Comparative Analysis of 4-bit CMOS Vedic Multiplier and GDI Vedic Multiplier using 18nmFinFET Technology", International Conference on Smart Electronics and Communication, 2020

[2] M. BalaMurugesh and S.Nagaraj, "Modified High Speed 32-bit Vedic Multiplier Design and Implementation", International Conference on Electronics and Sustainable Communication Systems,2020

[3] P Saritha and J. Vinitha,"4-Bit Vedic Multiplier with 18nmFinFET Technology", International Conference on Electronics and Sustainable Communication System , 2020

[4] AnkitGarg and GarimaJoshi,"Gate diffusion input based 4-bit Vedic multiplier design", IET Circuits, Devices and System, 2018

[5] Shashank.Meti and C.N. Bharath,"Design and implementation of 8-bit vedic multiplier using mGDI technique", International Conference on Advances in Computing , Communications and Informatics, 2017

[6] Syed Zohaib Hassan Naqvi,"Design and simulation of enhanced 64-bit Vedic multiplier", 2017 IEEE Jordan Conference on Applied Electrical Engineering and Computing Technologies (AEECT)

[7] Jia Miao and ShuguoLi,"A novel implementation of 4-bit carry look-ahead adder",2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC)

[8] S.Nagaraj, B.Babu Rajesh, K.Chaithanya, P.Pratap," Simulation Of Low Power 9t&14t Full Adder With Reduced Noise", Journal of Advance Research in Dynamical and Control Systems ISSN 1943-023x12 special 2017.

[9] R. BalaSaiKesava,B. Lingeswararao, K. BalaSindhuri,N. UdayaKumar,"Low Power And Area Efficient Wallace Tree Multiplier Using Carry Select Adder With Binary To Excess-1 Converter",2016 (CASP)Conference on Advances in Signal Processing , Cummins College of Engineering for Women, Pune. Jun 9-11, 2016.

[10] Sridhar, K; Nagaraj, "High Speed IEEE-754 Double Precision Floating Point Adder/Subtractor and Multiplier Using Verilog", International Journal and magazine of Engineering, Technology, Management and Research ,ISSN NO.: 2348 -4845 ,Volume 2, Issue 4, 2015

[11] KokilaBhartiJaiswal,VNithish Kumar, PavithraSeshadri and LakshminarayananG,"Low Power Wallace Tree Multiplier Using Modified Full Adder",2015 3rd International Conference on Signal Processing, Communication and Networking (ICSCN).

[12] SandeepKakde, Shahebaj Khan, PravinDakhole, ShailendraBadwaik,"Design of Area & Power Aware Reduced Complexity Wallace Tree Multiplier",2015 International Conference on Pervasive Computing

ISSN: 2233-7853 IJFGCN