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Implementation of 2.4 GHz LNA for Wireless Applications

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***Abstract*—**Low Noise Amplifier (LNA) circuit is available in the initial juncture of microwave receiver, and this stage has vital role in minimizing noise figure of the system, providing required gain with adequate linearity, and guarantees steady 50 Ω input impedance. The modeling of a LNA in Microwave (MW) circuit necessitates the trade-off between various significant features like gain, Noise Figure (NF), stability. This state of affairs compels the designers to create alternatives in the design of MW circuits. The vital objective of the paper is that it implements a single stage 2.4 GHz LNA design by means of single-stub microstrip lines with minimum lengths using Agilent ATF-21170. The amplifier is manually designed using conventional techniques, Smith chart is used for the matching of the input and output of the amplifier. Optimization of the designed amplifier is done using Keysight Advanced Design System (ADS 2020) software.

***Keywords*—**ADS2020, ATF21170, Impedance matching, LNA, Microwave receiver

1. INTRODUCTION

A Low noise Amplifier (LNA) is an electronic amplifier that amplifies a very low power signal with no significant reduction in its SNR. An amplifier boosts the power of the signals including the noise available at its input. Low Noise Amplifier is mainly intended to suppress that extra added noise. Engineers can reduce the added noise by selecting lesser noise component, operating points and system topologies. With the rapid growth of the wireless industry, diverse varieties of wireless communication systems are essential. Low noise amplifier is the exceptionally essential constituent of RF receiver, forming the first stage of RF network [1-3]. LNA boosts the gain value or magnify the amplitude value of the signal and reduce the noise figure value of the signal. Different parameters are taken into account while designing an LNA like lesser value of noise figure, lesser value of input and output return losses, a larger value of IIP3, larger gain and lesser utilization of power. With the intention to accomplish the necessary gain it is crucial to have a minimum value of Scattering parameters (S- Parameters) represented by S11 and S22 named as input and output reflection coefficients respectively. The proposed model has been simulated and implemented using ADS software.

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2. LITERATURE REVIEW

The design, simulation and implementation of the 2.4 GHz is done by following steps like the dc biasing of the transistor, Stability bias, Input and output impedance matching network with and without stubs using ADS tool. Rafik M. Et-Trabelsi (2009) has proposed Optimum noise figure and gain for LNA [1]. Arun Sharma, et. al.(2016) designed the CMOS LNA is proposed with 0.18 μm technology [2]. S. Vimal, et al (2016), has proposed Performance improvement using L-L matching and π-π matching network [3].Tim Das (2013), has explained that the dynamic range of LNA is based on gain [4]. M.Ben Amor, et al (2008), has explained about T matching techniques employed to, increase gain with increase in amplifier stages [5]. Dr.S.P. Mahajan, et al (2013) has explained about Unconditional Stability over the complete range of frequencies along with sustainable gain and low noise figure [6]. Guillermo Gonzalez (1997) had explained about "Microwave Transistor Amplifier" [7]. Authors in [7], [10], [15], [16] has explained the simulation of various devices using ADS software.David M. Pozar (2009) et al, have reviewed "Microwave and RF Wireless System [8]. P.B. Kenington has explained about "High-Linearity RF Amplifier Design" in the year 2001 [9].S.Y. Liao (1990), has explained about "Microwave devices and circuits"[10]. P.B. Kenington et al in [11], has presented a high linearity RF amplifier design. S.Y. Liao in [12] has explained about various microwave devices and circuits. P.L.D. Abrie, in the year 1991 designed of RF and Microwave Amplifiers and Oscillators [13]. "Impedance Matching and the Smith Chart Fundamentals"[14].

3.1 OVERVIEW OF LOW NOISE AMPLIFIER

A Low noise amplifier is a vital module at the initial stage of a radio receiver circuit that helps in reducing unwanted noise at a specific dB. In the majority of receivers, the overall Noise Figure depends on the few modules of RF front end.

The use of LNA next to the RF source minimises the noise effects produced due to various phases of the receiver present in the system by the gain of the signal generated by means of the LNA. The noise produced with in the LNA is also added to the receiver signal.

The LNA amplifies the required signal, power by including very less noise and distortion as feasible. The function of LNA permits best repossession of the preferred signal in the later phases of the circuit.

Frii's formula is utilised to evaluate the overall noise factor of a cascade phases, each with its own noise factor and power gain (assuming that the impedance are matched at each stage). The overall noise factor can then be used to evaluate the overall noise figure.

The overall noise figure is given by,

$$F_{total}=F_1+ (F_2-1/G_1) + (F_3 -1/G_1G_2) +\ldots..$$

$$+ (F_n-1/G_1G_2\ldots.G_n)$$

Where F_4 and G_4 represents the i^{th} phase values of noise factor and the power gain respectively and n is the total number of phases. Both magnitudes are represented as ratio, not in decibels.

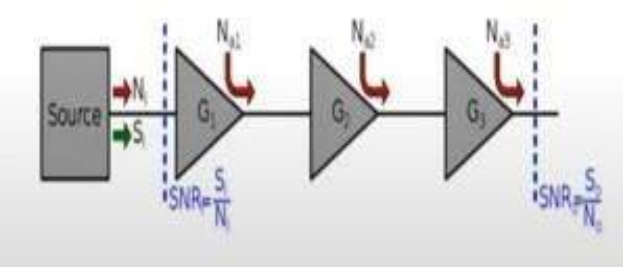

Fig. 1. Noise Figure at i/p and o/p Stage.

Noise Figure:

$$NF = 10\log_{10}(F)$$

$$= 10\log_{10}(SNR_i/SNR_o)$$

$$= SNR_i\,(dB) - SNR_o\,(dB)$$

3.2. LNA DESIGN SPECIFICATIONS

The following design specifications given in Table 1 are used for the simulation of the Low Noise Amplifier.

Table1. Design Specifications

Description	Range
Frequency Range	2.35 GHz -2.45GHz
Gain	>14 dB
I/P return loss(S11)	<-15dB
O/P return loss(S22)	<-15dB
Noise Figure	>=1.4dB
P_1 dB	>10dB
OIP3	20dBm

3.3 CHARACTERISTICS OF THE TRANSISTOR ATF-21107

- **Transistor Frequency Range:** 0.5 GHz to 6GHz.
- **Low noise figure:** 0.9dB at 4GHz
- **Gain:** 13 dB at 4Ghz
- **Output power:**23.6 dBm P_1 dB at 4 GHz
- **Hermetic Gold Ceramic Microstrip Package.**

3.4. TRANSISTOR DESCRIPTION

The ATF-21170 is a highly reliable better performing Gallium Arsenide Schottky barrier gate field effect transistor packed in a hermetic.

The GaAs FET component has a micron gate length of 0.3 and an overall gate periphery of 750 microns. Confirmed metallization systems made with gold and nitride passivation provides a strong dependable transistor.

4. MATCHING NETWORK

The input matching network forms the initial stage making sure that the maximum signal enters the LNA for further processing to achieve maximum power, and least amount of reflection. The maximum power transfer theorem, requires the input impedance of the low noise amplifier to be the complex conjugate of the source impedance. For ease of calculation a real value of 50 Ω source impedance is used. The inductive source degeneration LS is used to match with the desired 50 Ω source impedance. Reduced input return loss provides the maximum power transfer from previous stage [13].

4.1. LOW NOISE IMPEDANCE MATCHING

The Gamma optimum is the reflection coefficient of the source impedance provided to the device that permits the device to generate its NFmin. The ability of the amplifier in achieving the equivalent noise figure value equal to NFmin is limited by the losses present in the matching circuit. Gamma optimum must be equal to S11* indicating that the noise is not matched to the gain. Rn (noise resistance) is utilized to evaluate the sensitivity of the devices in noise figure to changes in source impedance, the normalization of Rn is equated to 50Ω.

5. RESULTS AND DISCUSSION

The simulation and design of Low Noise Amplifier is carried out by the following steps like the dc biasing of the transistor, Stability bias, Input and output impedance matching network with and without stubs.

5.1. STEP 1: DC BIASING OF TRANSISTOR

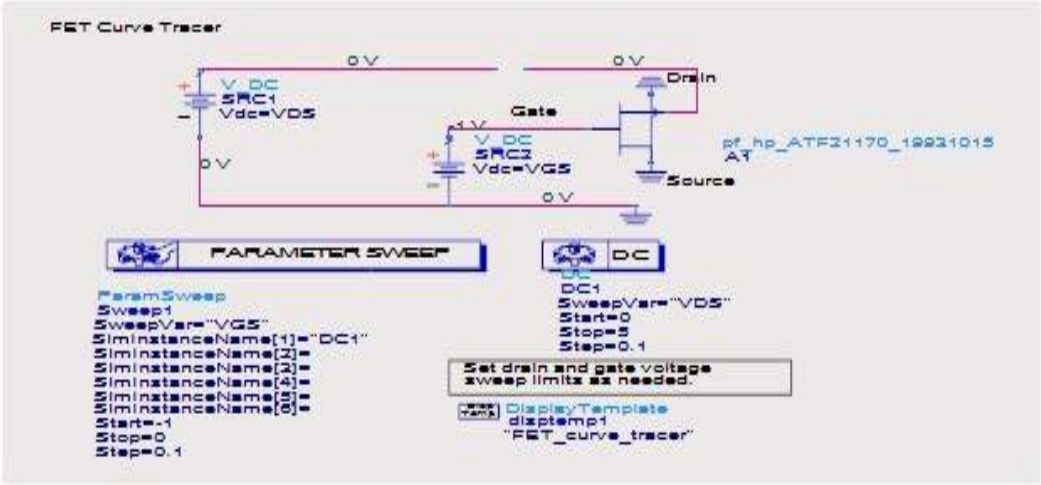

Fig. 2. DC Biasing Circuit of the Transistor

The figure 2 represents the DC biasing of the transistor in order to find the biasing condition of the transistor. The transistor used here is pf_hp_ATF21170_19901015. The FET curve tracer template is implemented because we are using FET transistor.

5.1.1. SIMULATION RESULT

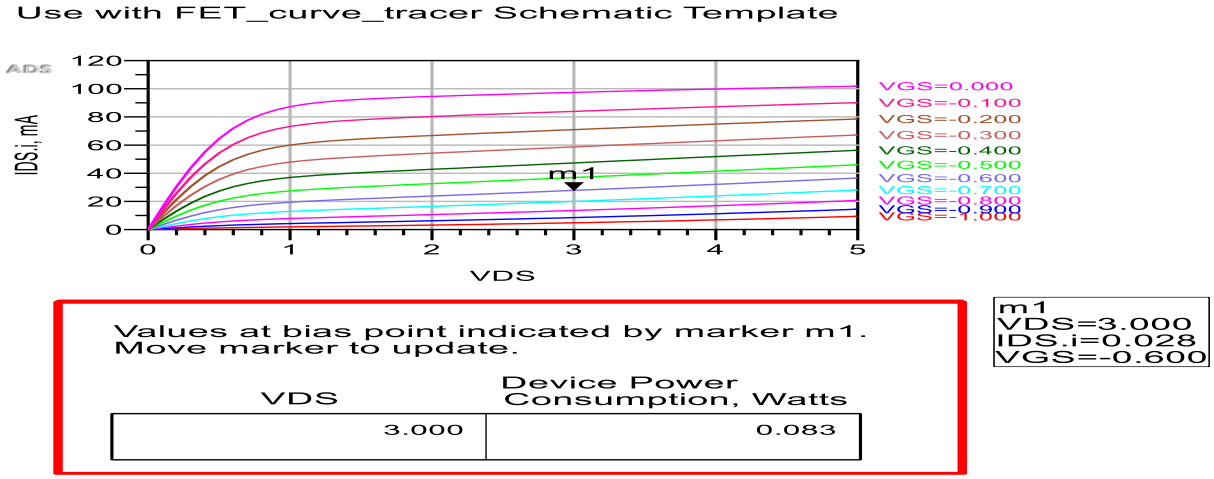

Fig. 3.DC Bias output graph.

The above figure 3 represents the of the DC biasing condition for the transistor. VDS=3V and IDS=0.028 mA

5.2. STEP 2: STABILITY BIAS DESIGN

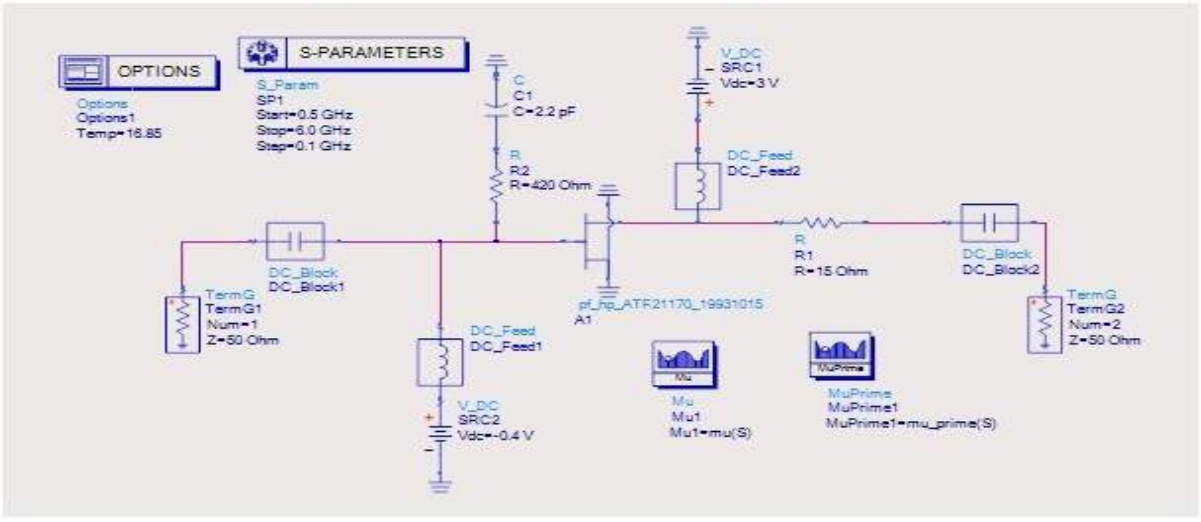

Fig. 4. Stability Circuit

To verify the stability of the transistor the above circuit is implemented. The S-parameter simulation is used to verify the stability. The resistors are included series and shunt in order to get proper stable condition for the transistor. The temperature temp is set to16.85 C because in the noise figure calculation the temperature must be less than 16.85 C as per IEEE standard.

5.2.1. SIMULATION RESULT

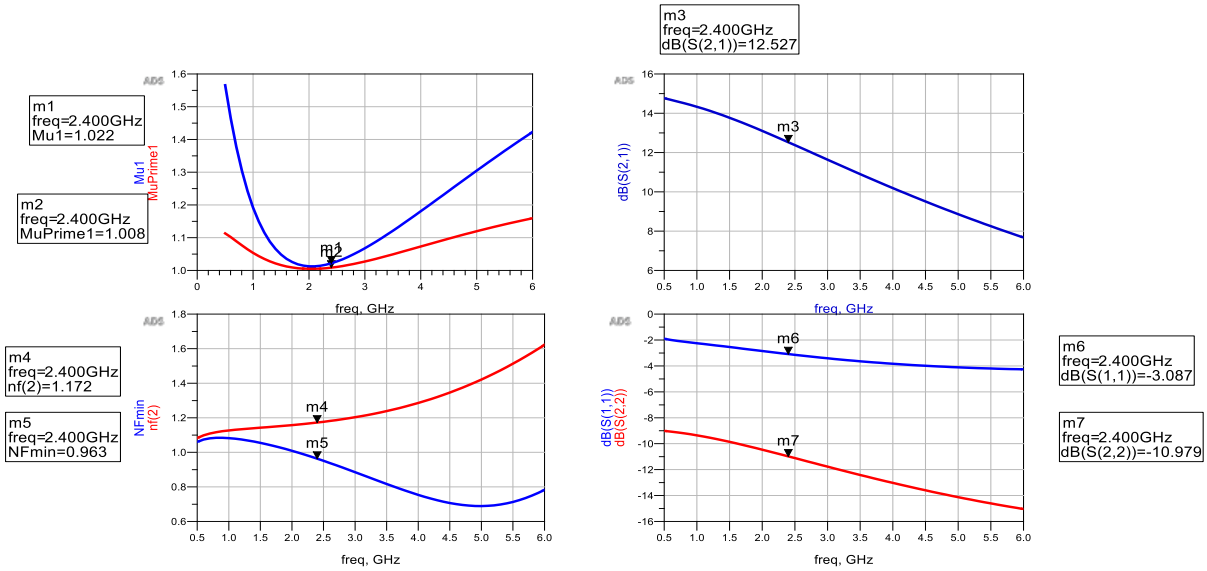

Fig. 5. Output of the Stability Circuit

The above figure represents the stability, NF, forward gain and return loss. The stability is around 1.008 and the noise figure is also good as expected. The noise figure is 0.983 and the gain obtained is 12.572 dB which is slightly less than our specification. This can be improved in further circuits. The return loss is also good.

5.3. STEP 3: BIAS NETWORK DESIGN

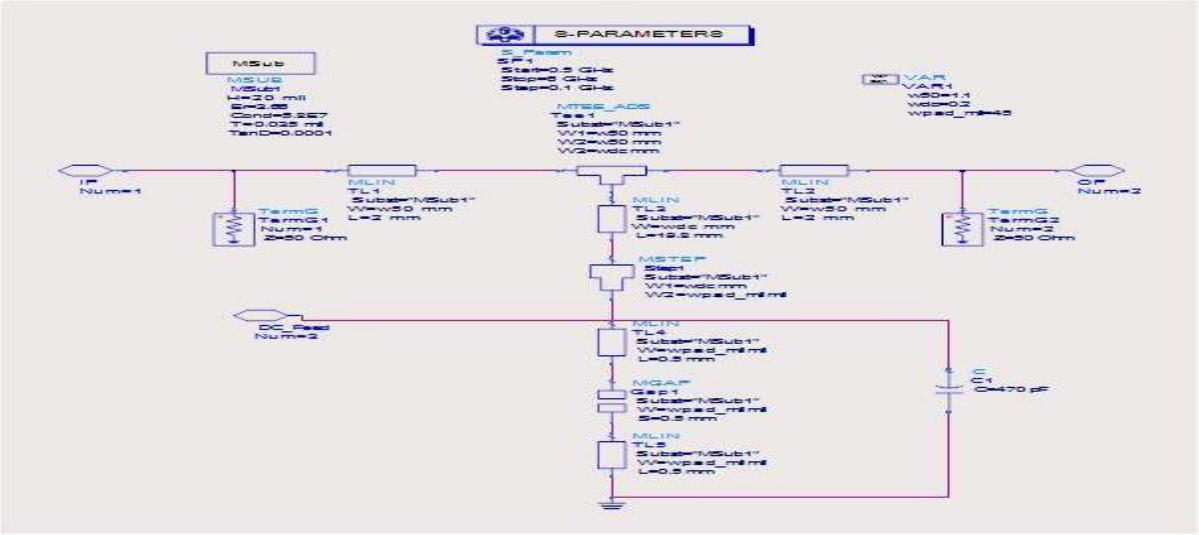

Fig. 6. Bias Network Design

The above circuit represents the bias network design which consisting of biasing circuit and the stability together. This circuit will be used in all the Impedance matching circuits.

5.5. STEP 5: IMPEDANCE MATCHING CIRCUIT WITHOUT STUB

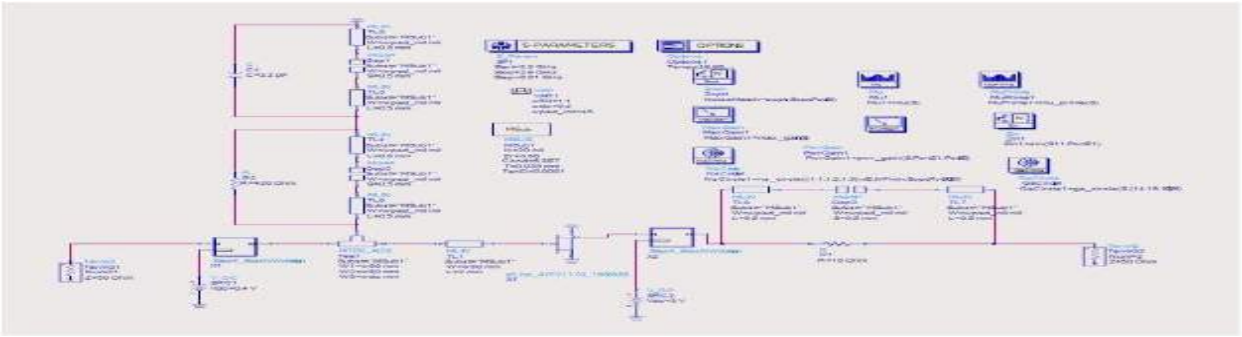

Fig. 7. Impedance Matching Circuit.

The above circuit is the impedance matching circuit which consists of stability circuit, biasing circuit, and the matching circuit. This circuit checks the matching property of the transistor. This circuit provides results matching condition as given in the specification.

5.5.1. SIMULATION RESULT:

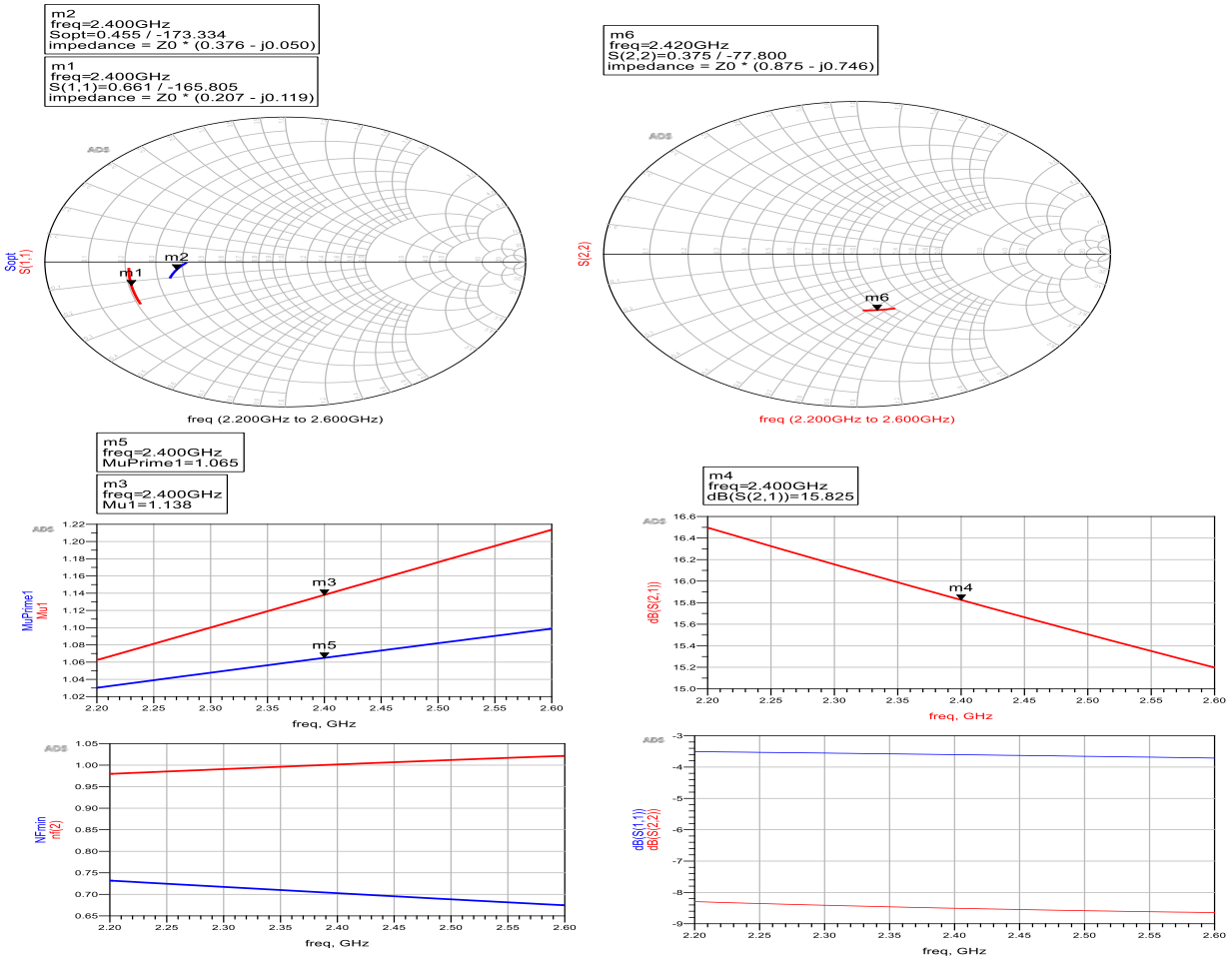

Fig. 8. Output of the Matching Circuit.

The stability is 1.05 and the Noise Figure is good than our Specification which is 0.874 dB and the gains is about 12.144 dB and return loss is less than -15 dB. The Gamma optimum is about 0.448 and the impedance is 19.112*j2.446.

5.6. STEP 6: INPUT IMPEDANCE MATCHING NETWORK WITH SINGLE STUB

The below circuit consist of stability, biasing circuit, along with a single stub matching circuit.

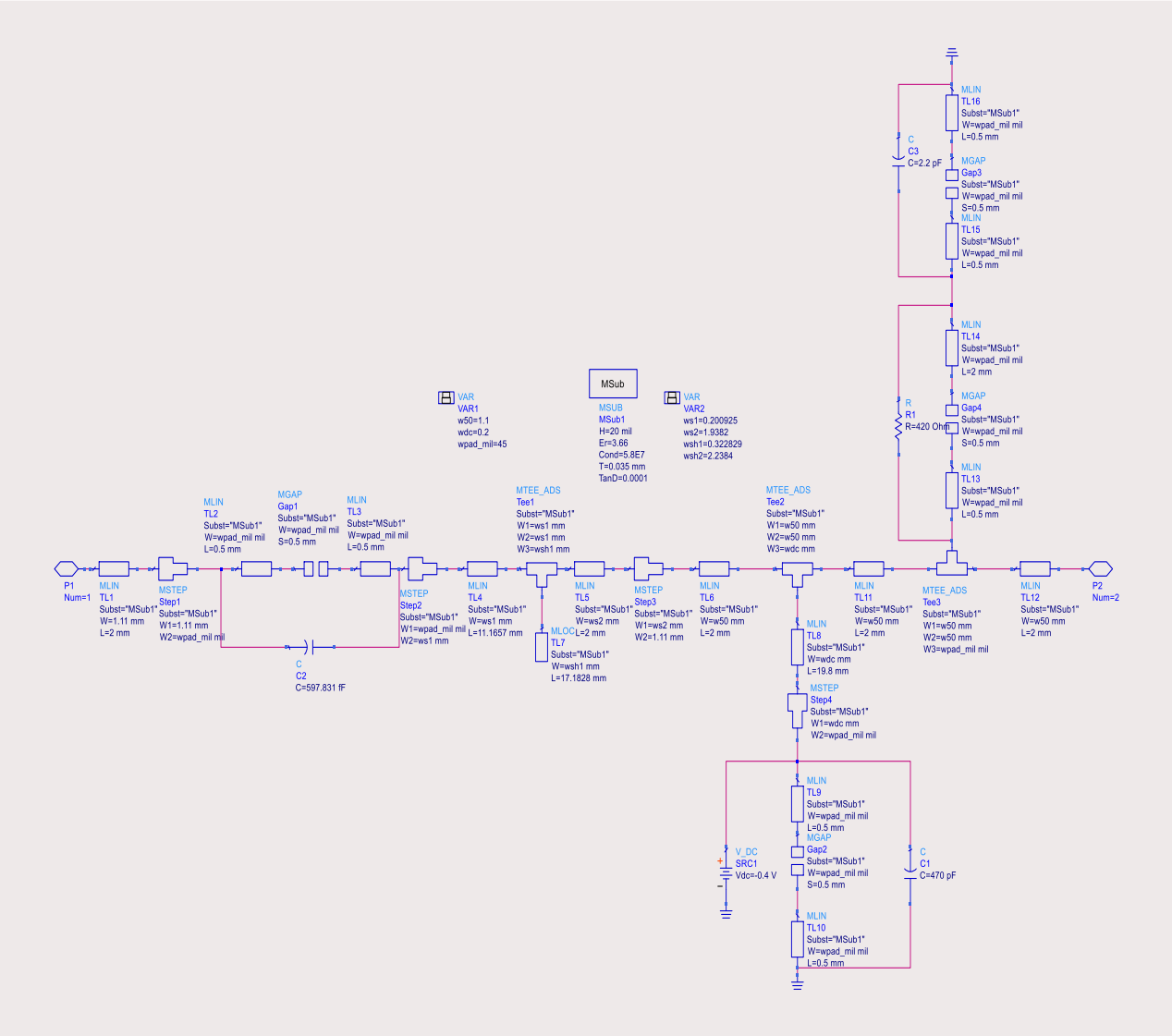

Fig. 9. Input Matching Circuit

5.6.1. STEP 6B: OUTPUT IMPEDANCE MATCHING NETWORK WITH DOUBLE STUB

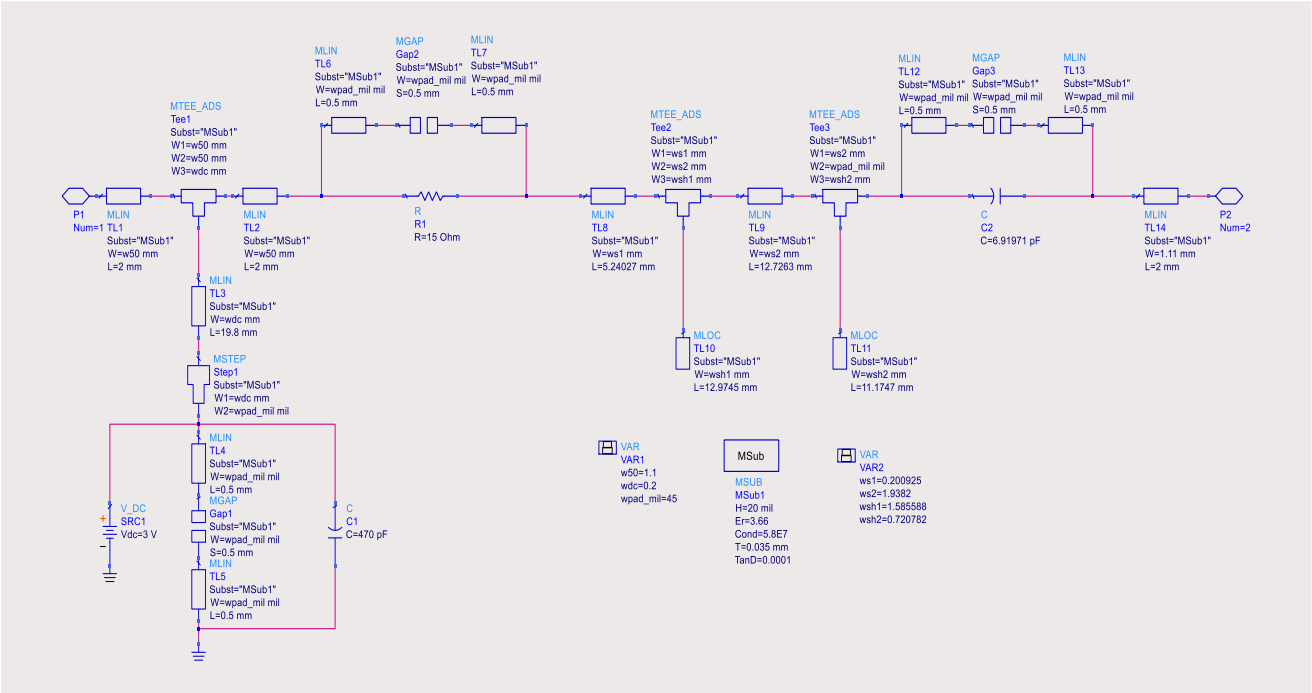

Fig. 10. Output Matching Circuit.

The output matching circuit has double stub at the output side of the circuit. The both input impedance and output impedance circuit will be use as combined circuit in further steps.

5.7. STEP7: INPUT AND OUTPUT IMPEDANCE MATCHING CIRCUIT

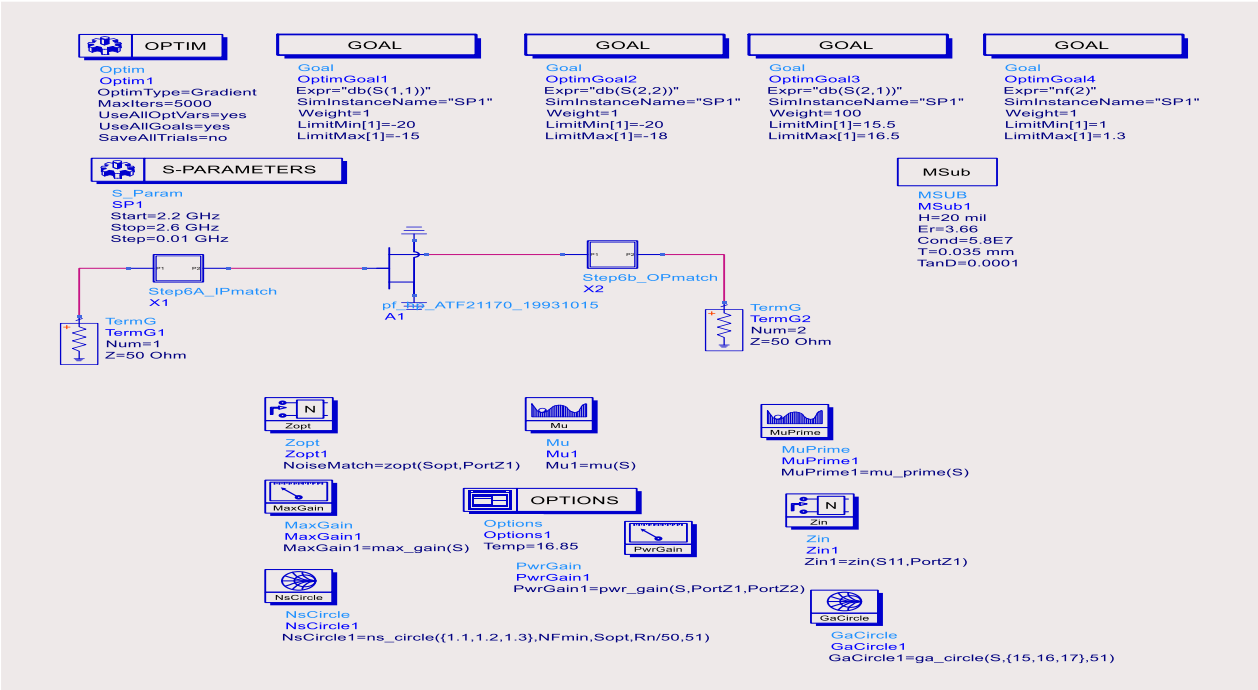

Fig. 11. Impedance Matching Circuit

The above circuit consists of both input and output impedance matching circuit. In the above circuit gain, noise figure and return loss are optimized in order to get the proper results.

5.7.1. SIMULATION RESULT

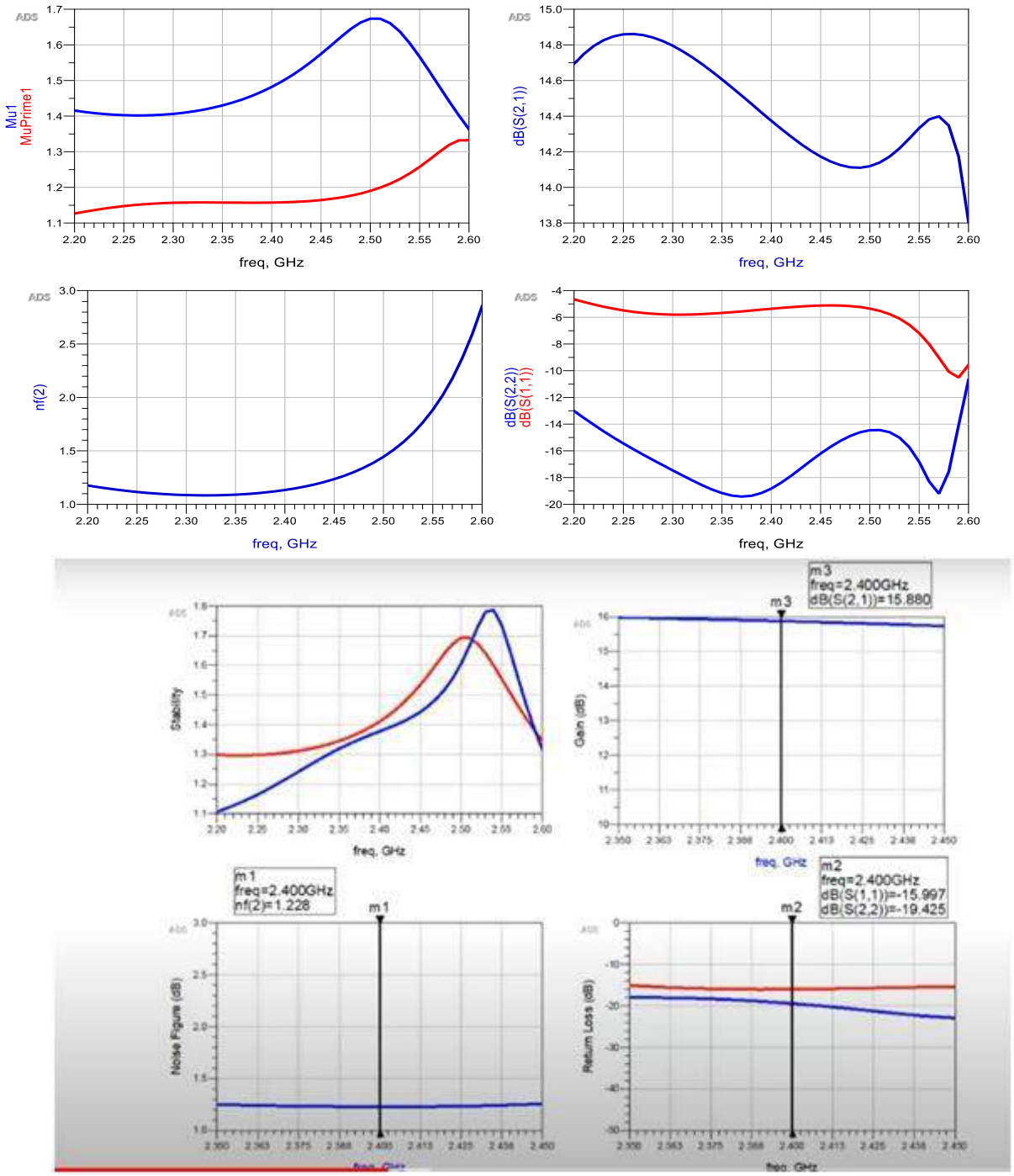

Fig. 12. Result of Impedance Matching Circuit.

The Noise figure is 1.228 dB which is less than 1.4db as specified and resulted gain is 2 dB greater than as specified.

The gain resulted was good for all further simulations and the return loss is less than <-15 dB as specified.

5.8. LAYOUT DESIGN

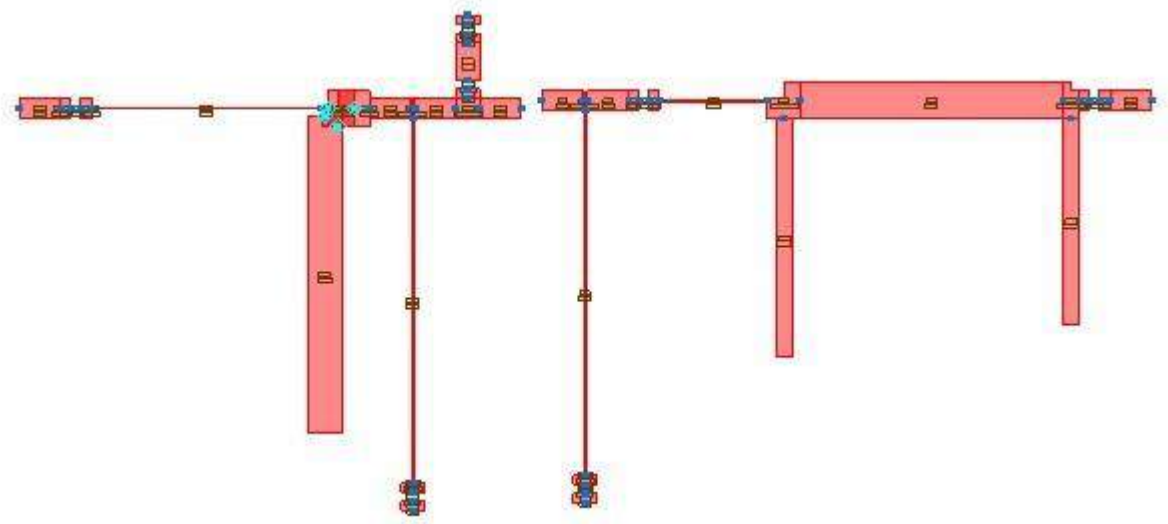

Fig. 13. Layout design of IP and OP matching circuit.

The above figure 13 represents the input and output matching layout design. The circuit ready for the fabrication. After fabrication components will be soldered and tested. Figure 14 shows the fabricated LNA.

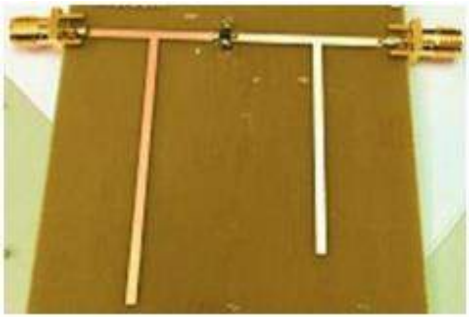

Fig. 14. Fabricated LNA

6. CONCLUSION

This paper illustrates the designing, simulation and implementation of a LNA that operates at a frequency of 2.4 GHz using Advanced System Design software with the consumption of less power value of 4.49mW and provides lesser noise figure value of 1.228 dB and a larger gain value of 15.86dB which can be used for various wireless applications.

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