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A New Approach for Implementing High Performance Capacity Achieving Codes For Wireless Communication Applications: Polar Codes.

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Abstract

An emerging error-detection and correcting technique developed in the recent years is Polar codes. The technique does not focus on randomization of the bits like other techniques does, but is based on the Shannon theory and channel polarization. This paper presents a successive cancellation (SC) algorithm based FPGA implementation of Polar codes. The implementation focuses on low complexity decoder for high speed applications. Simulation results show that the performance of polar codes can outperform that of turbo orLDPC codes.

Keywords: *Polar codes, FPGA, error detection and correction, Shannon theory.*

Introduction

Polar codes are used in the context of a coding problem that was traditionally formulated by Shannon in 1948, and which entails transmitting binary data over a noisy channel. Statistical models such as BI-DMS, BPSK+AWGN, and others are used to characterise noisy channels, as shown in Figure 1. In this case, binary bits are sent over the channel and a noisy version of those bits is received. All that's left now is to recover the original bits that were sent from the noisy version of those bits. The idea of Shannon is to improve the system's performance by doing something called redundancy. In simple words K bits are taken and are converted to N bits, and receive the noisy versions of the N coded bits, and estimate the original message from these noisy coded bits [1]. Basically, this is where the encoding and decoding takes place. This system can now perform far better than the previous one. This is known as the coding system, and it can only achieve Shannon capacity if it is done in a very intelligent manner. This has been an ongoing issue for many years. An encoding block, a decoding block, and a code-construction block make up the Polar Coding system. The parameters that go into the encoding and decoding blocks are determined by the Code-construction block. Polar codes are thought to be the first capacity-achieving codes. The codes for achieving capacity are nothing more than that.

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the names in the running heads and the author index

When these codes are used to simulate their performance, the codes that approach capacity appear to be very close to the capacity [2]. Unfortunately, there is no mathematical proof that they reach capacity asymptotically.

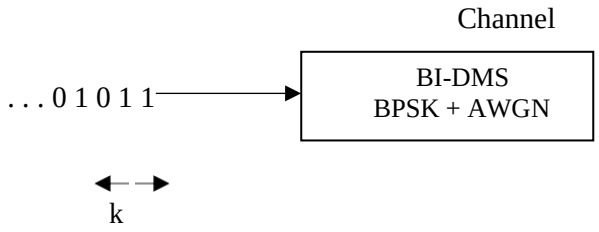

Fig. 1. Noisy channel representation

The channel polarization process for memory less binary channels was described by Arikan [3]. S. Liu is a Chinese character. Et al [4] proposed polar codes based on block fading channels. As the fading block changes according to the fading coefficient, the fading process is described as a natural polarization. G. B.Ocherer [5] proposed a higher-order modulation polar codes concept in which bit reliabilities after successive demapping are estimated using the LM-rate, a mismatched decoding rate that can be achieved. The polar codes are then reconstructed using Gaussian approximation.

M. S. H. Hassani, R. Mondelli, and S. H. Hassani the polar code with sub linear complexity and C was proposed by Urbanke [6]. S. A. Hashemi, W. Condo, and S. A. Hashemi J. Gross [7] demonstrated a high-reliability multi-mode polar encoder and decoder. C. discussed the successive cancellation decoding algorithm. Condo et al. [8], as well as S. A. Hashemi and colleagues [9]. The literature [10] discussed a minimum distance based and portioned list decoder. The memory problems associated with polar codes were also discussed [11].

$$\ldots Z_3\ Z_2\ Z_1 \longrightarrow$$

$$2.\quad \boldsymbol{F}^{\otimes n} \triangleq F \otimes F \otimes \ldots \ (n\ times)$$

3. Polar Codes

With respect to three parameters, N, K, and I, the polar code is desired.

1. The code length of the bits is mentioned as N.

2. K is used to represent the information in bits present in the length.

3. The bit reversed as a pair of K indices is represented by I.

f 0, 1,..., N 1; f 0; f 1; f 2; f 3; f 4; f 5; f 6; f 7; (1)

The information bit indices are mentioned above.

Bit reversal is simply taking n bits of integers and representing them in binary format, then reversing the order into the required format and taking them in the form of f.

b1, b2,..., bn, bn... b2b1 (2)

4. The frozen bit indices are mentioned as the complementary set fc.

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2.1 Kernel

The kernel is also highly utilized technique in the coding process. This is a triangular kernel. It utilizes koneke product operations as an outcome the matrix dimensions gets doubled in each iteration. Initially it begins with the 2*2 size and then goes to 4*4 sizeand soon.

2 by 2 matrixes

$$F^{\otimes 2} = \begin{pmatrix} F & F \\ 0 & F \end{pmatrix} \quad (4)$$

4 by 4 matrixes

$$F^{\otimes 3} = \begin{pmatrix} F^{\otimes 2} & F^{\otimes 2} \\ 0 & F^{\otimes 2} \end{pmatrix} \quad (5)$$

The dimensions grow as the powers are smaller.

1 Encoding

Encoding vector is nothing but multiplying the vector with the kernel.

Encoding eq: (kbits $\rightarrow Nbits$):

$$X = F^{\otimes n} d \quad (\sim x = Gu) \quad (6)$$

Where {

$$d_I c = 0, and$$

$d_i = u \rightarrow the\ message$

The above process is quite similar to the traditional encoding process, where k message bits are multiplied directly with the generator matrix (Gu) and obtains the information which is encoded.

D is not the matrix but the value of the d is embedded inside the matrix for obtaining the efficient outcomes. In the traditional process the message gets varied with respect to the information given by the user. But in the novel encoding process the information goes efficiently without any interference of the user. For example, if rectangular matrix is taken where the rectangular matrix is embeddedinside the matrix then

Example: N = 8, K = 5, f = {1, 3, 5, 6, 7}

Then x = $\boldsymbol{F^{\otimes 3} d}$

The d_0 ,2, d_4 represents the complementary information of the

So due to this the developers basically use only few columns for translating the information, where the blue colored columns gets eliminated, which is quite similar to the classic form of linear encoding. When compared to the traditional one, there isn't as much variation. Matrix multiplication is usually of quadratic complexity, which makes it more difficult to implement than simpler implementations. Because we're talking about polar codes, which are asynchrotically high, more efficient techniques are required. The developers have a specific type that is required for their work.

$$\begin{pmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \end{pmatrix} = \begin{pmatrix} 1&1&1&1&1&1&1&1 \\ 0&1&0&1&0&1&0&1 \\ 0&0&1&1&0&0&1&1 \\ 0&0&0&1&0&0&0&1 \\ 0&0&0&0&1&1&1&1 \\ 0&0&0&0&0&1&0&1 \\ 0&0&0&0&0&0&1&1 \\ 0&0&0&0&0&0&0&1 \end{pmatrix} \begin{pmatrix} d_0 = 0 \\ d_1 \\ d_2 = 0 \\ d_3 \\ d_4 = 0 \\ d_5 \\ d_6 \\ d_7 \end{pmatrix}$$

Fig. 2. Encoding example

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A very efficient O (N log N) implementation is available. It is capable of reducingthe N square order Through the linear order of N log N information.

3.2 Efficient O (N log_2 N) implementation

$$x = F^{\otimes} \ , in\ just\ (\frac{N}{2}\ log\ N)\ XORs \qquad (7)$$

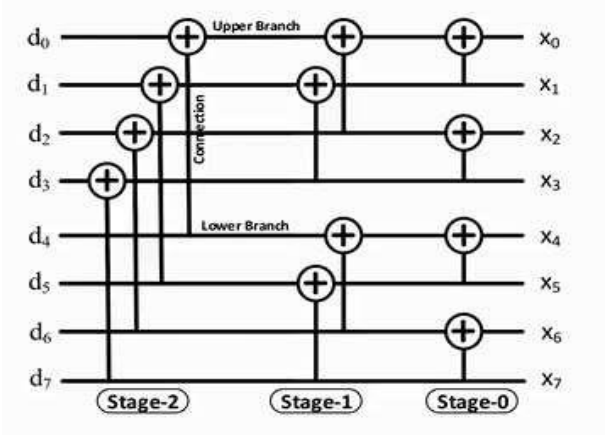

Fig. 3. Encoding computation tree

The edge or operation used in this technique is depicted in the diagram above. As a result of the x0 value block implementing one kernel, it is possible to conclude that whatever the input is, it will be executed here. It consists of four f values in stage 0. So, by cascading several small f values in an intelligent manner, the value of which can be computed efficiently, can be implemented here. The three stages are depicted in the diagram above.the end result The connection, as well as the upper and lower branches, can be used to represent any stretched circuit. The process described above is known as a highly efficient process. It can be used by running a matlab code and having a basic understanding of the circuit. Systematic coding is a method of coding which is capable of representing the entire coding process as an upending process of redundancy. As a result, after the encoding process, the messaged bits cannot be observed as identical to the encoded bits. Though the redundancy being added or upended, redundancy is being added in a very linear passion between the n bits that are being output, but incase the developers can sustain the messages as a copy paste as it is in the code word that is called a symmetrical
a code

3. Decoder

Successive cancelation decoder is the most common and efficient decoder used in the industry for decoding polar codes. It's a greedy tree search based method, where instead of searching the binary tree in an exhaustive process one foot link is selected every time and the search is carried out.

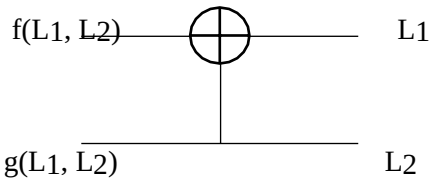

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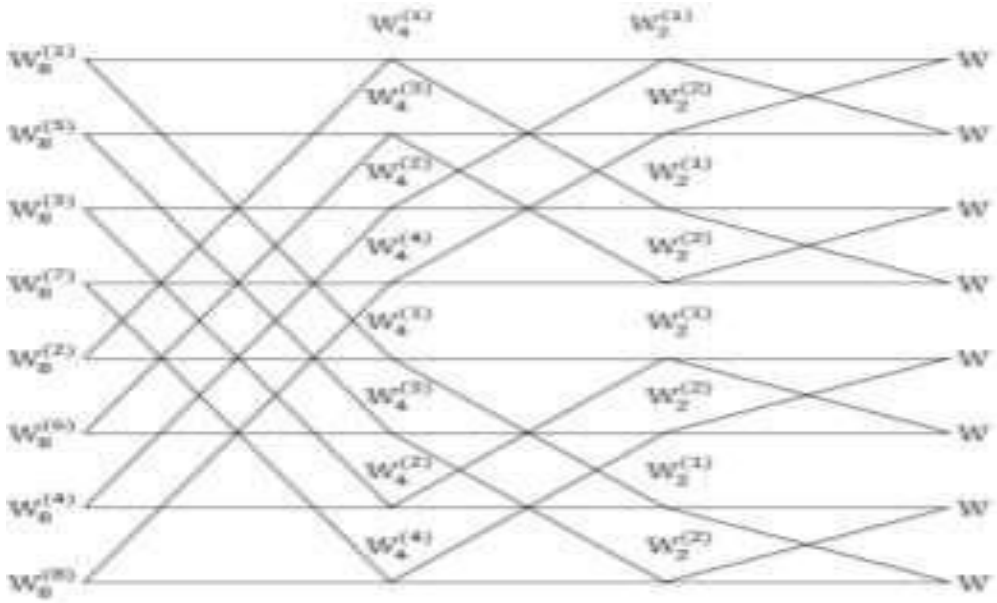
Fig. 4. Decoder basic structure

It is a two way recursion based process where if two inputs L1 and L2 are given to the fundamental construction block, two variable functions are produces as outputs. The second operation depends on the intermediate bit decisions from the upper branch.

$$\begin{pmatrix} L_1 \\ L_2 \end{pmatrix} \rightarrow \begin{pmatrix} f(L_1, L_2) \\ g(L_1, L_2) \end{pmatrix} = \begin{pmatrix} \frac{L_1 L_2 + 1}{L_1 + L_2} \\ L_1 . L_2 \text{ or } L_2 / L_1 \end{pmatrix} \quad (7)$$



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Step 3: u is decoded in this step. The procedure is the same as step 2, except that when computing g functions, the value u is used instead of L. When L is finally obtained, u is determined.

Step 4: After that, the remaining bits u,..., u are decoded in the order they were received. Each bit would be decoded using previous bits' knowledge.

4 Results

The polar encoder described in the above section is implemented using Verilog HDL in Xilinx 14.5 edition. The target board used is FPGA Vertex 7.

Fig. 6. Encoder schematic Gate level design **Fig. 7.** Encoder Simulation Results

The simulation results show the encoded results of the 8 bit data. Table 1 presents the device utilization summary of the proposed algorithm.

Table 1. Device Utilization summary.

Logic Utilization	Used	Available
Number of Slice LUTs	17	150720
Number of fully used LUT-FF pairs	0	17
Number of bonded IOBs	20	600

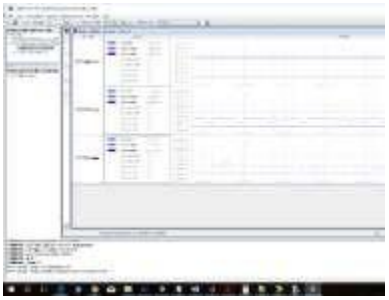

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Fig. 8. Chip scope analyser results

The chip scope analyser is used to examine the output from the FPGA board, as shown in figure 8. The schematic and gate level description of the polar decoder are shown in figures 9 and 10..

Fig. 9. Decoder Schematic Gate level design **Fig. 10.** Simulation Results

Figure 10 shows the simulation result of the decoder. The decoded data matches withthe input data bits given to the system.

Table 2. Device Utilization summary.

Logic Utilization	Used	Available
Number of Slice LUTs	17	150720
Number of fully used LUT-FF pairs	0	17
Number of bonded IOBs	21	600

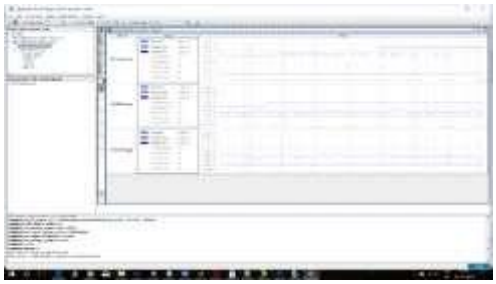

Fig. 11: Chip scope result

Conclusion

The proposed algorithm is synthesized and tested on the Vertex 7 FPGA board, and the paper presents a successful implementation of polar codes with successive cancellation decoding in Verilog HDL. In the paper, all of the results are tabulated and discussed. When compared to traditional counterparts, the procedure devised uses far less power and occupies far less space.

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