International Journal of Future Generation Communication and Networking
Vol. 13, No. 4, (2020), pp. 5089 - 5098

Designing Ultra Wideband Low Noise Amplifier

Mohamad Haneef, Dr. Rahul Mishra
Research Scholar, Department of Electronics and Communication Engineering, Dr. A.P.J. Abdul Kalam University, Indore, M.P.
Research Guide, Department of Electronics and Communication Engineering, Dr. A.P.J. Abdul Kalam University, Indore, M.P.

Abstract

This text reveals the configuration of a low noise amplifier for ultra-wide bands (UWB LNA). A symmetrical 3D RF integrated inductor was used to create the proposed UWB LNA which extends its bandwidth from 2.5 GHz to 16 GHz. This UWB LNA gains from the proposed LNA with an overall performance range of 6 dB-18 dB and -12 dB to 0 dB in low output mode and a bandwidth of –3 dB of 2 GHz. In the high gain setting mode, the noise figure (NF) is 3.5-4.5 dB. In a high-gain mode the planned LNA is 6 dB-18 dB and in a low-gain mode, -12 dB to 0 dB and a bandwidth-3 dB is 2 GHz. In high gain mode, the noise (NF) number is 3.5-4.5 dB.

Keywords: *Low Noise Amplifier (LNA), Ultra-WideBand (UWB), CMOS Technology, Noise Cancellation.*

1. Introduction

Due to its reduced cost and compatibility with silicone-based chip systems, CMOS technology is one of the most common technologies used for implementing RFIC's. A low noise amplifier is one of the most critical components in each receiver (LNA). An ultrawideband device is named, given it runs between 3.1 GHz and 10.6 GHz. The output evaluation of an LNA has included parameters such as energy usage, gain, noise figure, stability and linearity. To accomplish the above-mentioned goals, various topologies have been used such as the popular source with forward body prejudice, common source with resistive input and noise cancelation. The minimum voltage supply was 0.6 Volts, which finished with best power gain (S21) and the best interface for the third order (IIP3). Using a typical source with resistive feedback topology, the best input impedance matching was achieved. The technique of canceled noise created the minimum figure for noise among all works. A forward body preconditions technique obtained minimal power usage of 1.68 mW.

Ultra-Wideband (UWB) networking networks, in particular personal area network (PAN), are likely to play an even more significant role in today's short-range communications systems. The backbone of the UWB front-end RF receiver is known as a low noise amplifier. It absorbs and amplifies the signal through the UWB frequency spectrum. LNA's architecture standards provide low and flat noise characteristics, strong voltage and low power gains, reasonable large impedance input and output fit, high reverse insulation, and low DC power consumption. The amplifiers that have been sold have large bandwidth and high gain, but they utilize large fiber and chip regions. The basic gate amplifier

ISSN: 2233-7857 IJFGCN

provides large input matching, but has low gain and superior noise. The resistive feedback generates generally a strong fit between the broadband and the flat gain.

The architecture of the LNA must contend with trade-offs including LNA topology collection and broadband noise balancing. The architecture methodologies for UWB LNA can optimally increase the sensitivity of the receiver and therefore have specific low levels of signal handling. The antenna or antenna device must also be tightly integrated with the LNA in order to eliminate any losses and hence to minimize the sound of the front end, ideally on the same HF module.

When wireless communications are initiated, the UWB radio frequency transceiver (RF) is introduced, which has an appropriate function over the entire UWB frequency spectrum. RF transceiver is an instrument that transmits and receives RF signal in a single module and the key application is to provide sufficient information in the form of a voice, data or video that can be transmitted by the wireless media. The intermediate frequency (IF) RF transceiver is used to transform to RF and vice versa. The main crucial blocks of the RF transceiver are the low noise amplification (LNA) and the power amplifier (PA). The LNA receiving and PA transmitting paths link to the antenna through a duplexer, distinguish two signals from each other and avoid the comparatively efficient PA output from overloading the responsive LNA. Figure 1 displays the clearly-identified RF, LNA, and PA block diagram of the RF transceiver.

The emphasis of the work in this area is on developing UWB LNA for front ends of radio receivers, where LNA, a standard part of the wireless circuit, is used frequently. The first main block in the recipient's wireless architecture is LNA. The LNA has a strong effect on signal propagation and minimizes the noise intensity of the signal. It is a specific form of amplification for the amplifying of very poor signals captured by an antenna in the wireless communication systems. RF reception ratio may be improved by creating a UWB LNA high gain and low noise (NF) number. However, many other criteria, such as low power consumption, are still needed to extend battery life, particularly for mobile devices, high gain, strong wideband input/output matching, stability and linearity.

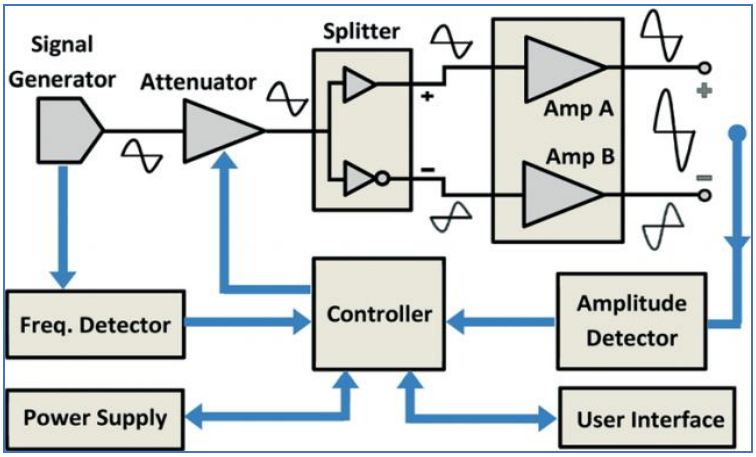

Fig. 1 Block Diagram for the Wideband Amplifier Circuit

Literature Review

HemadHeidariJobaneh (2020) This text designs and simulates an ultra-low-power and ultra-wideband LNA. The design's central aim is the minimal energy consumption in the CMOS technology of 0.13 μm. Three separate common-source LNAs are used in the proposed LNA. Furthermore, modern and reliable formulae are measured in this paper for input impedance, output impedance and typical source LNA. The forward body bias strategy is used to reduce the power usage of the circuit. For MATLAB, all the equations suggested in this paper are planned and resolved. In addition, the Advanced Design Method (ADS) is used for the screening of LNA using TSMC 0.13 μm CMOS process. For Noise Figure (NF), the input fitting (S11), gain (S21), gain (S23), power dissipation (IIP3) and power dissipation (NF) respectively, the results obtained are 2.13 dB-2.32 dB, -18.7 dB.

Jose E. Velazco (2019) The ngVLA 8-48 GHz frequency ranges have been introduced in a single broad band recipient kit. This frequency spectrum of five separate receivers is covered by the new JVLA. It is our view to decrease the amount of device reception required to reach the entire frequency spectrum. A four-course feed horn, low noise amplifiers (LNA), and a downgrade converter to analog intermedium frequencies are the recipient kit we created. The feedhorn as well as the LNA are cooled criogenically. On the LNA front, we followed two MMIC designs of 8 to 48 GHz; the first one using 70 Nm gallium arsenide, HEMT and the second one using HEMT 35 Nm indium phosphide. In this post, we mention the calculated gain and noise of the LNAs.

N.F. AB Halim, S.A.Z Murad, A. Harun, M.N.M Isa, S.N. Mohyar and A. Azizan (2019) This paper introduces a 3.1-6.0 Ghz high speed CMOS (UWB LNA) architecture with m technology as a wireless body bias technique. The UWB LNA in cadence program is programmed and simulated with 0.13-. Two common-source (CS) stage amplifiers with a forward body bias technique compose the UWB LNA suggested. In the first point, a source degenerated inductor is used to obtain a high linearity and broadband input. A shunt-speaking inductor is employed for higher frequency gain in the second level. The calculations reveal that the UWB LNA suggested has a power gain (S21) of 10 dB, an input range loss (S11) of less than 5 dB, a minimal range of noise (NF) of 8.5 dB in the frequency ranges of 3.1- 6.0 GHz with an input dissipation of 17,2 mW – 9 dBm and a 3rd intermodulation intercept. The UWB LNA design is 0,68 mm2 Proposed.

Maryam Vafadar (2016) This paper introduces an ultra-wideband (UWB) frontend low-noise (LNA) inductive amplifier architecture. A reusable, improved architecture for canceling noises is proposed and the advantages and disadvantages of the improvement process will be addressed. Capacitive peak is used to increase the gain ratio and bandwidth of 3 dB at the risk of total viability. The 0.18-μm tricample CMOS technology is manufactured for the LNA circuit. There is a strong matching measurement result with a low signal gain of 11 dB and a bandwidth of 3-dB of 2–9.6 GHz. The LNA consume 19 mW with an inductor-based configuration, a low supply voltage of 1.5 V. It demonstrates that an LNA that has been designed without an inductor. In an inductive system, the

silicon region is greatly reduced; just 0.05 mm2 of the LNA centre, which is one of the smallest designs recorded.

Vahid Farmehini, Ali Rohani, Yi-Hsuan Su and Nathan S. Swami (2014) Insulator-dependent dielectrophoresis allows contactless isolation and biosystem study, but cannot function efficiently within the MHz frequency range that is important for manipulating organic cells based on their particular structure or cytoplasmic electrophysiology. We present the design concepts for a broadband amplifier to cope with the steep decrease in output strength and the elevated signal distortions within standard amplifiers at MHz frequencies due to slew rate limitations. This is validated by the absence in the amplifier performance of harmonic distortions and parasitic DC up to 15 MHz and hence by the continuous force propagation into the MHz range of the cytoplasmic modification on the Cryptosporidium parvum oocysts.

UWB LNA Circuit Design

The Fig.2 The designed LNA broadband displays. It consists of two phases of CG (Q1) and Q2 and Q4 cascades. The root buffer (Q4 and Q5) is used for transforming the output impedance. The CG Small Signal Circuit with cascade is provided in Figure for wideband matching at input Equation gives the impedance on the input line (2).

$$Z_{in}(s) = (C_{gs1} \| L_s) \| \left\{ \frac{1}{g_{m1}} \left[1 + \frac{Z_{L(S)}}{r_{ds}} \right] \right\} \quad \textbf{(2)}$$

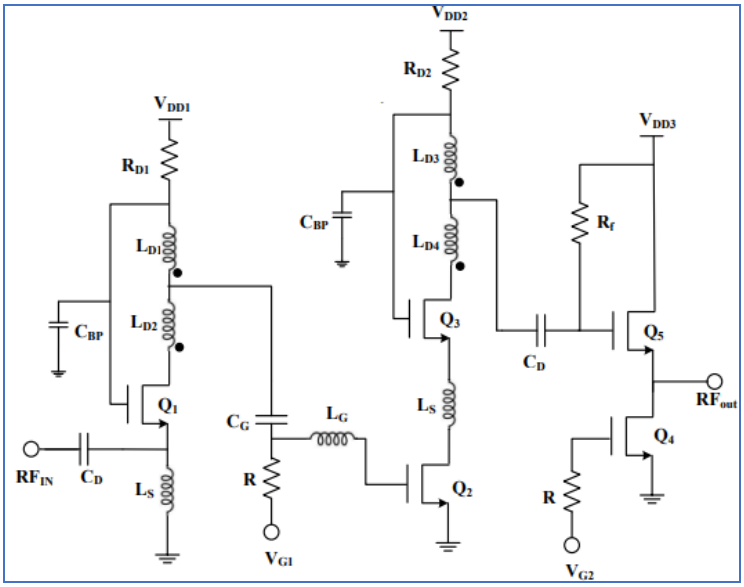

Fig. 2: Schematic of the Proposed LNA

The dual-resonance charge network delivers the right impedance across the broadband spectrum as seen in Fig. 3. There are two resonances for low and high frequencies. At output and the input Cgs1 and LS simultaneously echo, the Cgs2

display the high impedance direction (LD1 || LD2 || CD1) chosen less frequency |o, low frequency || CD1.

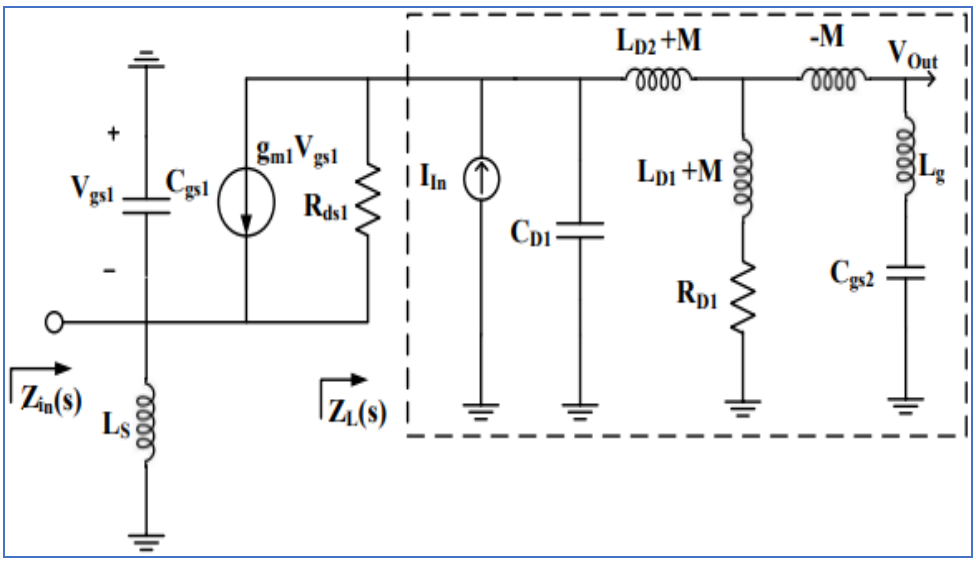

Fig. 3: The CG Stage Small Signal Equivalent Circuit with Load Network at the Drain of M1

Active Inductor Structure for UWB

Spiral inductor's principal drawbacks involve a huge area of silicon, minimal inductance, and low efficiency. Many active topologies, several of which use the framework of the C-G-Condenser, have been established and addressed. These projects have a limited area with a good quality silicone. Figure indicates the active structure of the induction used for this article. 3 is an active inductor updated variant. Transistor size has been appropriately chosen to have inductivity in the RF frequency range. The active inductor as the load in the second stage amplifier is used and attached to the drain by coupling condenser. Active inductor's frequency reaction indicates that the active inductor provides RF induction. Imagepresents the output in UWB frequencies of the active inductor structure. For high-frequency gains of LNA, there is a moderately high inductance (2nH-8nH) in the active inductor with a moderately high Q factor.

The usage of multiple transistors in the circuit layout is necessarily noisier than passive inducers. Each transistor contributes thermal noise to the circuit noise, such that a reasonable sizing of transistors is possible to obtain minimal noise. In order to minimize the noise figures in UWB LNA in general, a chip spiral inductor is often used to match the initial level.

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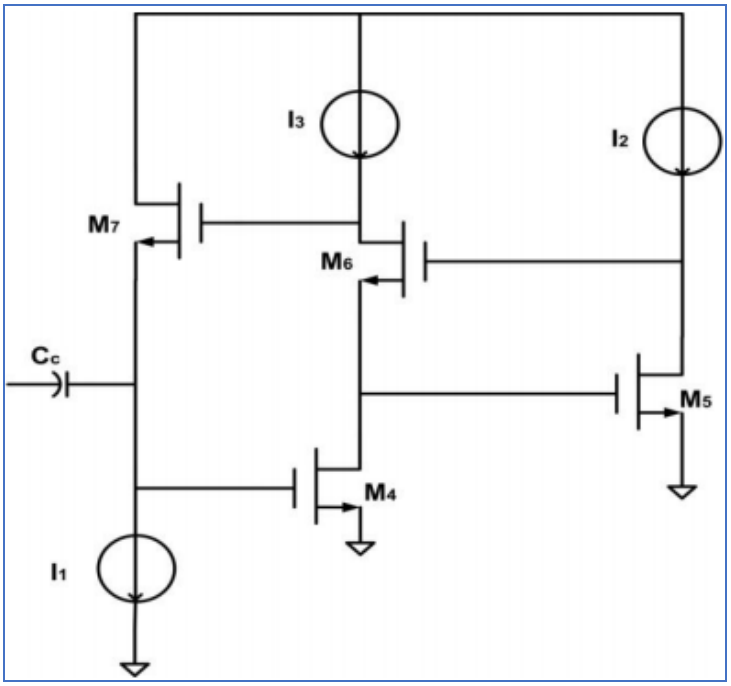

Fig. 4 Active Inductor Circuit Structure

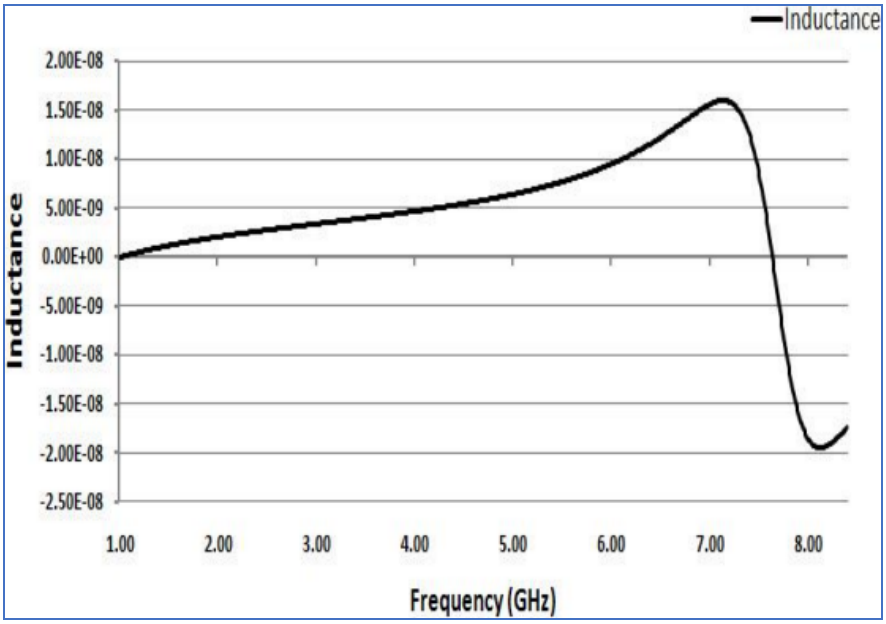

Fig. 5 Frequency Response of Active Inductor

Experimental Results

The proposed digital controllable gain inductor-free wideband LNA is produced in CMOS typical technology of 0.18 m. The chip image is displayed in the Fig. 6. Open drain buffer in the differential pair style is built-in to supply the output signal to measuring devices without significant gain loss or noise loss. On-wafer measures are carried out to classify the proposed LNA.

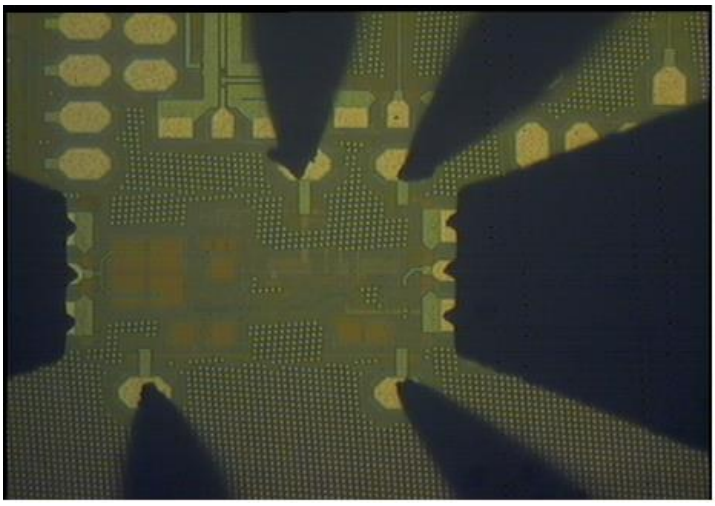

Fig. 6 Chip Photograph of the Proposed LNA

The parameters of dispersion computed (S) are shown in the diagram. Thirteen and Fig. 7. The LNA suggested for 75 Ohm characteristic impedances, which is very typical in tuner systems, has been designed because software-defined radio's low band (0.2-2 GHz) involves several standards such as cell TV tuner DV B-H (470-860 MS, 1670 to 1,675 MS), MediaFLO (712 - 722 MSh), etc. Initially. However, only 50 Ohm source and charging impedance are required for the measuring devices, which results in the degeneration of the measuring output of the circuit. The S11 of the proposed LNA stays below -10 dB in high-gain mode up to 1.3 GHz and up to -6 dB in 2 GHz. The LNA gain is 2 GHz -3 dB in bandwidth and the maximum potential value 18 dB is 2 dB less than the product of the post-layout simulation. The benefit during testing by digital bits differs and a predefined ground tuning of approximately 6 dB can be accomplished and a fine tuning of 2 dB. S11 is already below -5 dB in the working band of 0.2-2 GHz in low gains mode. Compared with the high gain mode the gain comes with a comparable bandwidth –3dB, around 2 GHz, and the overall gain is 0.

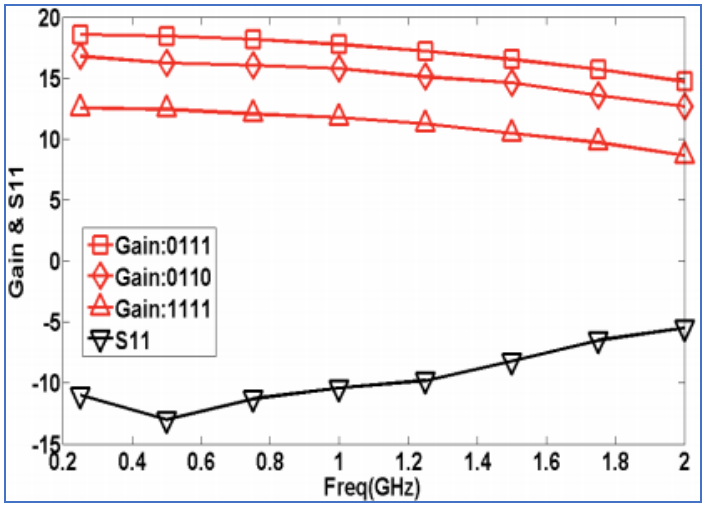

Fig. 7. The Measured S11 and Gain Performance of the Proposed LNA in High Gain Mode

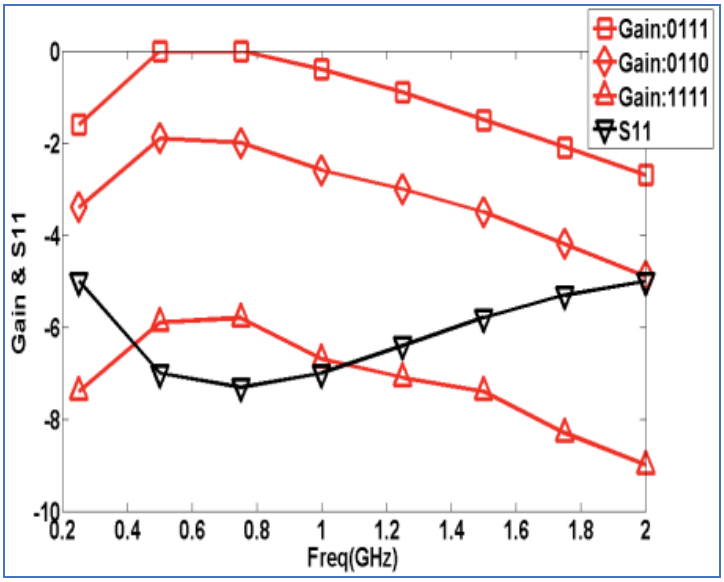

Fig. 8. The Measured S11 and Gain Performance of the Proposed LNA in Low Gain Mode

The tested noise number is 1.5 dB higher than the typical after-layout simulation, as the output of S11 is partially decreasing as a consequence of the conversion issue from 50 Ohm to 75 Ohm. The frequency band of 0.2-2 GHz in high-gain mode is between 3.5 and 4.5 dB as seen in the figure. 8.

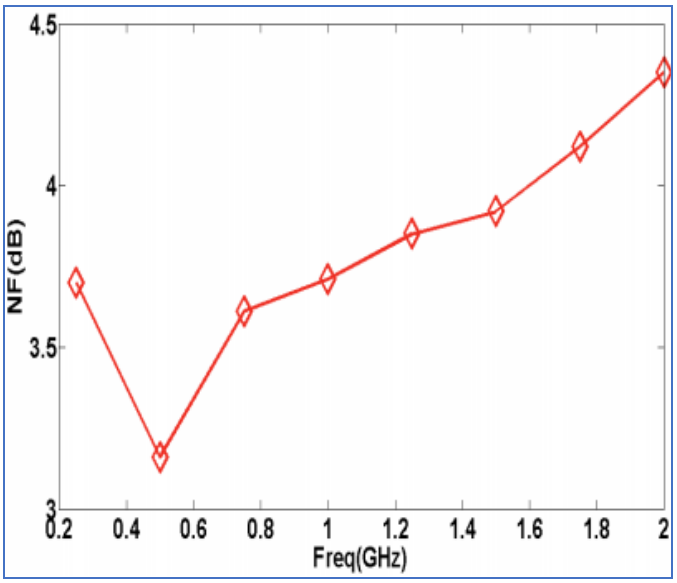

Fig. 9. The Measured Noise Figure Performance of the Proposed LNA in High Gain Mode

The IIP3 simulated post-layout of the proposed LNA is -7 dB with the exception of the free drain buffer. Because of our measurement devices the linearity testing has not been completed and has not been mentioned here.

ISSN: 2233-7857 IJFGCN

With the strength of the output buffer the proposed LNA absorbs 20 mW from 1.8V. The circuit is zone-efficient and takes up a Silicon region of m, including the 600 AMBAT 300 AM on the buffer chip and test pads, because of its inductorless feature.

Conclusion

The paper has shown the UWB-capable inductor-free LNA architecture. Without on-chip inductors, a syncretic usage of thermal noise cancelation, peak condenser and current reuse resulted for an ultra-wide 3-dB bandwidth. A profitable architecture was proposed based on the noise cancelation theory, and this circuit was studied in depth. It can't increase absolute bandwidth by capacitive peaks; nevertheless, it is an efficient means of regulating gain flatness. The LNA is manufactured in a 3-well 0,18-µm CMOS operation, rendering the implementations well balanced. Capacitive peak technology increases obtaining flatness of 0.2-2 GHz. This helps to achieve a high, reliable variable gain of 6 dB-18 dB and -12 dB-0 dB without compromising the output of the input impedance matching. The efficiency of the inductor-based designs is comparable and often stronger. When the maximum gain is obtained, the proposed LNA reaches a bandwidth -3dB of 2 GHz and a noise density of 3.5-4.5 dB. These findings suggest that our architecture is extremely acceptable for UWB LNA design.

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