Analysis and Design of OTA topologies for Biopotential signals

Kavitha M JSS Academy of Technical Education, Bangalore, India Dr. Akhila S BMS college of Engineering Bangalore, India

Abstract

Biomedical signals are very small amplitude and low frequency signals. Hence they require high gain, high CMRR and low noise amplifiers for processing. This paper presents Telescopic, Two stage and Folded cascode operational transconductance amplifier (OTA) topologies. The proposed OTA topologies employ a biasing, using constant current source with current mirror. The design of OTA is targeted for an implementation in biomedical devices. The proposed OTAs were designed in 180nm CMOS technology. Based on the simulation results, Telescopic OTA has high DC gain, wider bandwidth, lowest power dissipation and better settling time. Folded cascode OTA has moderate DC gain, wide bandwidth, lower power dissipation, higher CMRR and slew rate .Two stage OTA has moderate DC gain, low bandwidth with high power dissipation.

Keywords: Telescopic, Folded cascode, OTA, Two stage, current mirror.

I. Introduction

The miniaturization of electronic devices is due to semiconductor transistors, whose size has been decreasing drastically beyond Moore's prediction. The density of transistors on an IC has increased due to the scaling of the feature sizes. Technology scaling reduces the delay of the circuit elements, improves the performance and enhances the operating frequency of an IC. Due to advances in technology it is possible to implement on the same IC, analog and digital systems using the same technology. The whole world is analog in nature but the signal processing is becoming more and more digital. Digital circuits are advantageous than anlog circuits since they are less sensitive to disturbances, easy to design, more robust in supply and process variations. The analog signals acquisition and its processing require analog front-end (AFE). The block diagram of front-end for biomedical signal acquisition is as illustrated in Fig.1. It mainly consists of electrodes, amplifier, filter and ADC.



Fig.1. Block diagram of Biomedical signal acquisition

The bio-potential signal will be converted into an electrical signal by an appropriate sensor or transducer. The electrodes acts as transducer and its signals are usually appended with unwanted interferences. In order to amplify, only the biomedical signals by reducing the common mode noise - high gain, high CMRR and accurate amplifier is required [1]. The unwanted signal is then filtered and applied to ADC circuit for obtaining the digital values of analog data. The biomedical signal recording is one of the challenging task, since the biomedical signals have weak amplitude and low frequency, usually the amplitude varies between millivolts to microvolts and the frequency is below 1kHz. Table I shows the biopotential signals with their typical ranges of amplitude and frequency [2].

Bio-potential signal	Amplitude in mV	Frequency in Hz		
ECG (Electrocardiogram)	0.05 - 3	0.01 - 300		
EEG(Electroencephalogram)	0.001 - 1	0.1 - 100		
EOG(Electrooculogram)	0.01 - 0.3	0.1-10		
EMG(Electromyogram)	0.001-100	50 - 150		

Table I Typical amplitude and frequency ranges of Bio-potential signals

Operational amplifier circuits are the basic building block required for the design of many analog and mixed-mode circuits such as data converters, filters, amplifiers, portable devices, medical instrumentation and solar powered systems. The power reduction in portable devices that are battery operated like data converters and implantable medical devices is of concern. To reduce the amount of power dissipation usually on chip amplifiers are OTA. An op-amp without output buffer is OTA and it is voltage controlled current source, as it converts differential input voltage into an output current. As OTAs are smaller in size with simple design, they are preferred than op-amps .So, they are used in the applications where only capacitive load has to be driven, since it cannot drive resistive loads due to smaller currents. The commonly used CMOS OTA topologies are: Two stage, Telescopic and Folded cascode. The selection of an OTA topology is dependent on the circuit application and desired performance. The circuits consisting of OTA are affected by its specifications such as bandwidth, output swing, DC gain, settling time, linearity and power consumption. This paper is organized as follows. Related work is described in Section II. Implementation of different OTA topologies is explained in Section III. Measured results are rendered in Section IV and Conclusion in Section V.

II. Related Work

In [3] authors have designed cascoded telescopic opamp circuit to enhance differential gain and bandwidth, with additional two load capacitors. The load capacitors were designed with optimum values to reduce the power consumption. Telescopic opamp is designed based on MOSFETs zero temperature coefficient (ZTC) [4]. Two circuits were used for generating currents one with positive and other with

International Journal of Future Generation Communication and Networking

Vol. 14, No. 1, (2021), pp. 557-568

negative temperature coefficient. ZTC current reference is used for biasing the amplifier circuit. The circuit is designed with MOSFETs, BJT and resistors which occupies more area. Fully balanced OTA is designed by using dynamic threshold MOS (DTMOS) with adaptive biasing [5]. DTMOS transistors were used for primary stage implementation of OTA and active loads. In order to provide low power dissipation with improved slew rate, adaptive biasing circuit across reference side is implemented using NMOS transistors. Comparative analysis of opamp with different current mirror circuits such as Wilson mirroring, Wildar mirroring and cascode current mirroring is done in [6]. Wildar mirroring opamp circuit has low gain and consumes more power, whereas cascode op-amp has high gain. OTA is designed with two stages [1], first stage consists of folded cascade with a stack of 3 transistors followed by common source amplifier. Input is applied for PMOS differential pair and cascaded with second stage to achieve higher gain with maximum output swing. MOSFETs can be either bulk-driven MOS or gate-driven MOS .For low supply voltage, bulk-driven MOS are preferable than gate-driven MOS, has it is independent of threshold voltage. But the main drawback of bulk-driven MOS is low DC gain. High gain is one of the amplifiers important specifications. For example, a gain of 70-80 dB is required in switched capacitor integrators used in Sigma-delta modulators in order to deduce phase error and nonlinearities. In [7] high gain two stage amplifier is proposed and uses positive capacitive feedback for frequency compensation. One of the advantage of the designed circuit is it does not use common mode feedback circuit. To obtain larger output gain, folded cascode topology [8] is implemented with nmos input transistors. The length of all the transistors in the design is set to three times more than the minimum channel length in order to reduce the channel length modulation. The designed opamp is used for pipeline ADC applications. In MOSFETs, bias point is set by a stable dc drain current and dc drain-to-source voltage which ensures the operation of transistor in the saturation region required for faithful amplification, for all the applied inputsignal levels. The effective technique used for biasing MOSFET amplifier is constant-current source with current mirror is implemented in this paper. Current mirrors replicate the current from one device to another. Irrespective of the load conditions, the output current remains constant as current mirrors have high output impedance. It provides the active loads and bias currents to the circuits. This paper summarizes the comparison of Telescopic, Folded cascode and Two stage OTA topologies design with their performance parameters implemented in 180nm CMOS technology.

III. Implementation of OTA topologies

A. Telescopic OTA

The schematic of Telescopic OTA is illustrated in Fig.2. Transistor M1, M2 are nmos input devices and M3, M4 are nmos cascode devices.M5, M6, M7 and M8 are pmos cascode current sources. Telescopic

International Journal of Future Generation Communication and Networking

Vol. 14, No. 1, (2021), pp. 557-568

cascade OTA has high gain due to stacking of cascode transistors. Transistors Mb1 and M9 form the current mirror pair.



Fig.2. Schematic of Telescopic OTA

The designed OTA consists of differential amplifier across the input and the transistors of differential pair carry equal currents. The supply voltage applied to differential cascode OTA is 1.8V and a current source of 30μ A is applied to bias the circuit. Each cascode branch of OTA carries half of the bias current. The length of all the transistors is kept same, in order to reduce the errors due to the side diffusion of the source and drain areas. Table II summarizes the devices sizes of Telescopic OTA.

The transconductance of each transistor is calculated as,

$$g_{\rm m} = \frac{2*I_{\rm D}}{V_{\rm ov}} \tag{1}$$

and the width of each transistor is calculated by using current equation in saturation.

$$I_{D} = \frac{1}{2} K \left(\frac{W}{L}\right) (V_{GS} - V_{th})^{2}$$

$$\left(\frac{W}{L}\right) = \frac{g_{m}}{K * V_{ov}}$$
(2)
(3)

For NMOS transistor K is $\mu_n C_{ox}$ and for PMOS transistor K is $\mu_p C_{ox}$

The bias voltage for M3 and M4 is calculated as,

$$V_{\rm B} = V_{\rm GS3} + V_{\rm ov1} + V_{\rm ov9} \tag{4}$$

The gain of the circuit is obtained as,

$$A_{v} = G_{m} x R_{out}$$
(5)

Where G_m is approximately equal to g_{m1} and $R_{out} = [(g_{m3}r_{o3}r_{o1}) \parallel (g_{m5}r_{o5}r_{o7})]$ (6)

Transistor	W in µm	I _{Dsat} in µA	g _m in mA/V
M1,M2	15	15.41	.269
M3,M4	20	15.41	.219
M5,M6	40	15.41	.283
M7,M8	40	15.41	.217
Mb1	15	30	.448
M9	15	30.89	.458

Table II Device sizes of the Telescopic OTA

AC analysis of Telescopic OTA is as shown in Fig.3. For $C_L=1$ pF the obtained values of Open loop DC gain, unity gain bandwidth and phase margin are 92.07dB, 972 MHz and 64.57⁰ respectively. Fig.4. shows the transient analysis for Vin=1mV @ 100Hz.



Fig.3. Frequency response of Telescopic OTA

Fig.4. Transient response of Telescopic OTA

B. Folded Cascode OTA

Fig.5. illustrates the schematic of Folded Cascode OTA. It has NMOS input devices and PMOS cascade transistors. NMOS input devices have larger gain than PMOS input devices. In the designed OTA topology, the mirror circuit provides the gate voltages to the cascode load. The values of these voltages ensure that the transistors operate in the saturation region. MOSFETs M11 and M12 provide the DC bias voltages to M3-M6. M1 and M2 form differential amplifier circuit. The amplifier is applied with a V_{DD} of 1.8 V and a current source of 30µA is applied to bias the circuit. Table III summarizes the devices sizes of Folded cascode OTA.

The transconductance of each transistor is calculated as,

$$g_{\rm m} = \frac{2*I_{\rm D}}{V_{\rm ov}} \tag{7}$$

and the width of each transistor is determined as,

$$\left(\frac{W}{L}\right) = \frac{2*I_{D}}{K*V_{ov}2}$$
(8)

Vol. 14, No. 1, (2021), pp. 557-568

For NMOS transistor K is $\mu_n C_{ox}$ and for PMOS transistor K is	$\mu_p C_{ox}$
Resistance looking into drain of M6, $R_{up} = g_{m6} r_{o6} (r_{o4} \parallel r_{o2})$	(9)
Resistance looking into drain of M8, $R_{dn} = g_{m8} r_{08} r_{10}$	(10)
The output resistance, $R_{out} = R_{up} \parallel R_{dn}$	(11)
The DC gain of the circuit is given by,	
$A_d = g_{m1} R_{out}$	(12)

The output voltage of the OTA is
$$V_{out} = g_m V_{in} R_o$$
 (13)



Fig.5. Schematic of Folded cascode OTA

Table III Device sizes of Folded cascode OTA	Table	III	Device	sizes	of	Folded	cascode	OTA
--	-------	-----	--------	-------	----	--------	---------	-----

Transistor	W in µm	I_{Dsat} in μA	g _m in mA/V
M1,M2	15	15	.107
M3,M4	7	30.105	.136
M5,M6	7	15.105	.094
M7,M8	1.5	15.105	.107
M9, M10	1.5	15.105	.108
M11	7	30	.136
M12	7	30	.129

AC analysis of Folded cascode OTA is as shown in Fig.6. For $C_L=1$ pF the obtained values of Open loop DC gain, unity gain bandwidth and phase margin are 82.26dB, 17MHz and 85⁰ respectively.

International Journal of Future Generation Communication and Networking Vol. 14, No. 1, (2021), pp. 557-568 Fig.7. shows the transient analysis for Vin=1mV @ 100Hz. The advantage of folded cascode over telescopic is higher overall voltage swing, the draw backs are higher power dissipation, lower voltage gain and higher noise.



C. Two stage OTA

Fig.8. illustrates the schematic of two stage OTA. Transistors M1-M4 forms the first stage of differential amplifier stage with transistors M3 and M4 that forms a current mirror. The inverting and non-inverting input is provided at M1 and M2 respectively. The differential currents and the output resistance of first stage provide single-ended output voltage that drives the second stage. The second stage provides an additional gain which consists of PMOS current source load, M6 and NMOS common source amplifier M7. Coupling capacitor, Cc provides stability to the circuit. It does not affect gain but it affects Gain Bandwidth product. The supply voltage applied to two stage OTA is 1.8V and a current source of 30µA is applied to bias the circuit.



Fig.8. Schematic of Two stage OTA

The aspect ratio of M8 transistor is calculated by using current equation in saturation given by,

$$I_{D8} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_8 (V_{GS} - V_{th})^2$$
(14)

$$I_{D5} = \frac{\left(\frac{1}{L}\right)^3}{\left(\frac{W}{L}\right)^8} I_{D8}$$
(15)

$$I_{D1} = I_{D2} = I_{D3} = I_{D4} = I_{D5}/2$$
(16)

To ensure symmetry,
$$|V_{DS4}| = |V_{DS3}| = |V_{GS6}|$$
 (17)

Gain bandwidth expression is given by,
$$GBW = \frac{g_{m1}}{2\pi C_C}$$
 (18)

Aspect ratio of M1 and M2 is given by,
$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{g_{m1}2}{K_n * I_{D8}}$$
 (19)

Aspect ratio of M3 and M4 is given by,
$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \frac{I_{D5}}{K_p [V_{DD} - V_{INmax} - |V_{t5max}| + V_{t1min}]^2}$$
 (20)

Aspect ratio of M6 is given by,
$$\left(\frac{W}{L}\right)_{6} = \left(\frac{I_{D6}}{I_{D3}}\right) \left(\frac{W}{L}\right)_{3}$$
 (21)

$$\mathbf{I}_{D6} = \mathbf{I}_{D7} = \mathbf{I}_{D8} \frac{\left(\frac{\mathbf{W}}{\mathbf{L}}\right)^7}{\left(\frac{\mathbf{W}}{\mathbf{L}}\right)^8} \tag{22}$$

Table IV Device sizes of Two stage OTA

Transistor	W in µm	I_{Dsat} in μA	g _m in mA/V
M1,M2	3	15	.151
M3,M4	15	15	.15
M6	100	103.26	1.09
M7	14	103.26	.862
M5, M8	4.5	30	.266

AC analysis of two stage OTA is as shown in Fig.9. For $C_L=1$ pF the obtained values of Open loop DC gain, unity gain bandwidth and phase margin are 84.63dB, 8.1 MHz and 74⁰ respectively. Fig.10. shows the transient analysis for Vin=1mV @ 100Hz.



Fig.9. Frequency response of Two Stage OTA



Fig.10. Transient response of Two stage OTA

IV. Measurement Results

The proposed OTA circuits were simulated at 180nm CMOS technology with 1.8V power supply and targeted for its implementation in biomedical devices. The performance comparison of OTA topologies is tabulated in Table V. From the performance analysis of different OTA topologies, it is observed that each topology has its own advantages and disadvantages. For biomedical applications, OTA should provide a gain of 60dB and the phase margin must be larger than 45 degrees to ensure stability. The single stage telescopic amplifier consumes low power compared to other two topologies, hence can be used for low power applications. Telescopic OTA has high DC gain, wider bandwidth with lowest power dissipation, whereas folded cascode OTA has moderate DC gain, wide bandwidth with lower power dissipation .Two stage OTA has moderate DC gain, low bandwidth with high power dissipation. The differential gain of OTAs is as shown in Fig.11. Transient response for V_{in}=1mv @ 100Hz is as shown in Fig.12.

Parameters of OTA	Two stage	Telescopic	Folded Cascode		
DC Gain(dB)	84.636	92.073	82.26		
Bandwidth(Hz)	460.87	972	1279		
UGB(MHz)	8	30	17		
Phase Margin(deg)	74	64.57	85		
Power dissipation(µw)	294	109	162		
CMRR (dB)	92.596	135.97	165.59		
Slew Rate (v/ns)	0.05	0.023	0.022		
Settling time (ns)	154.07	56.73	82.153		
Squared output noise (mv^2/\sqrt{Hz})	11.11	2.11	44.183		

Table V Performance comparison of different OTA topologies



Fig.11.Comparison of DC Gain and UGB of Telescopic, Two stage and Folded cascode OTA.



Fig.12. Transient response of Telescopic, Two stage and Folded cascode OTA for Vin=1mV, fin=100Hz.

CMRR is an important specification of OTA which quantifies the rejection ratio of common-mode signals. It is a significant parameter in noise reduction, which is larger for folded cascode OTA.Slew rate is the rate at which the output responds to the changes in the input. Higher slew rate is preferable and it is achieved in Folded cascode OTA. Settling time is the closed-loop parameter and it is the time taken by the output to settle from the time of application of step input. The settling time depends on slewing behaviour and bandwidth. Telescopic OTA has better settling time. Fig.13. Illustrates slew rate and settling time of OTAs. Fig.14 shows the step response in a unity gain configuration for 1V input signal. Fig.15 shows the input referred noise as a function of frequency. The measured performance of OTA topologies are summarized in Table VI, with comparison to other published work.



Fig.13. Output waveform illustrating slew rate and settling time of Telescopic, Two stage and Folded

cascode OTA.



Fig.14. Measurement results of step response @ input signal of 500 kHz, 1V.



Fig.15. Input referred noise as a function of frequency.

Table VI OTA	Performances	and Comparison
---------------------	--------------	----------------

References	[1]	[3]	[5]	[6]	[8]	This work		
Technology(nm)	180	180	180	180	130	180		
OTA topology	Folded	Tele	Two	Two	Folded	Two	Two Tele Folded	
	cascode	scopic	stage	stage	cascode	stage	scopic	cascode
Supply voltage(V)	1	1.8	1	1.8	1.8	1.8	1.8	1.8
Load Capacitance(pF)		8	10		1	1	1	1
DC gain(dB)	67.81	43.41	83.56	20	64.5	84.63	92.07	82.26
Phase margin(deg)	45.9	91.19	64.08		68.4	74	64.57	85
UGB (MHz)	.964	820.46	39.18	1.2	695.1	8	30	17
Power consumption(mw)	7.243u	.4	.105	50	0.14	.29	.10	.16
CMRR(dB)	104.95	43.4	86.15	3	41.48	92.59	135.9	165.59

V. Conclusion

In this paper, low power and high gain OTA topologies were presented in 180nm CMOS technology for its implementation in biomedical devices. In recent years, telescopic and folded cascode OTAs are preferred due to their higher bandwidths and low power consumption in data converter applications. The drawbacks of telescopic cascode OTA topology shown in Fig.1 are limited output swing,

require higher supply voltage and consume more voltage headroom. In modern circuit design, limited output swing with high supply voltage is not preferred hence folded cascode OTAs are preferred.

References

- H S Raghav, B P Singh and S Maheshwari, "Design of low voltage OTA for bio-medical application," 2013 International Conference on Microelectronics, Communications and Renewable Energy, Kanjirapally, pp. 1-5, 2013.
- [2] Mohammed Samar Ansari, "Analog front-end design for biomedical signal acquisition systems," CSI Transactions on ICT, pp.1-5, 2019.
- [3] D. S. Shylu, D. Jackuline Moni, Neenu Brigit Francis, "Design and analysis of low power pseudo differential class-AB Telescopic operational amplifier," International Journal of Research in Engineering and Technology, Vol. 03, pp. 243-248, 2014.
- [4] L. Kouhalvandi, S. Aygun, E. O. Guneş and M. Kirci, "Design of a high gain telescopic-cascode operational amplifier based on the ZTC operation condition," 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Batumi, pp. 538-541, 2017.
- [5] M. Mahendra, S. Kumari and M. Gupta, "Low Voltage High Performance Fully Balanced Operational Transconductance Amplifier with Improved Slew Rate," 7th International Conference on Signal processing and Integrated Networks (SPIN), Noida, pp. 819-823,2020.
- [6] S. Kothapalli, M. Samson, S. Majji, T. R. Patnala, S. R. Karanam and C. S. Pasumarthi, "Comparative Experimental Analysis of different Op-amps using 180nm CMOS Technology," 2020 International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE), Vellore, pp. 1-6, 2020.
- [7] Alireza Mesri, Javad Javidan, Mahmoud Mahdipour Pirbazari, "Analysis and design of a two-stage amplifier with enhanced performance," Microelectronics Journal, vol. 46, Issue 12, pp.1304-1312, 2015.
- [8] Sohiful Anuar Zainol Murad, Izatul Syafina Ishak, Mohd Fairus Ahmad and Shaiful Nizam Mohyar, "Design of a low-power CMOS operational amplifier with common-mode feedback for pipeline analog-to-digital converter applications," Turkisk Journal of Electrical Engineering & Computer Sciences, pp. 1908-1921, 2017.
- [9] M Yavari and T Moosazadeh, "A single-stage operational amplifier with enhanced transconductance and slew rate for switched-capacitor circuits," J. Analog Integr. Circuits Signal Processing, vol. 79, No. 3, pp. 589–598, 2014.
- [10] B. Razavi, "Design of Analog CMOS Integrated Circuits," NY, Oxford University press, 1982.
- [11] P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design," New York, McGraw Hill, 1998.
- [12] Jacob Baker, Harry W Li, David E Boyce, "CMOS circuit design, layout and simulation," IEEE press series on Microelectronic Systems, 1998.