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Functional Verification of Enhanced Video Compression by Using H.265/HEVC Standard Using 45nm Technology

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Abstract

This presented paper implementation was optimized architecture of the inverse quantization and the inverse transform for a High-efficiency video coding (H.265/HEVC) decoder. In this design to develop the parallel and pipelined architecture was designed to support transform unit 4 × 4, 8 × 8, 16 × 16 and 32 × 32. The quantization and inverse transform described in RTL design using Verilog using Cadence tool with 45nm technology. The simulation results carried out for ram module in dequantizer which is used for to store the high compression rate of any data. The throughput of the current architecture reached in the worst case a processing rate of up to 1090 p at 35 fps at 200 MHz and 1080 p at 40 fps at 220 MHz when mapped to standard cells respectively. The validation of our architecture was conducted using a Software Cadence environment in order to evaluate different implementation methods in terms of power consumption and run-time. The experimental results demonstrate that the above designs were enhanced by more than 80% in terms of the run-time speed relative to the existing solution. Besides that, the power consumption of the current designs was reduced by nearly 70% compared with the other methods.

Keywords: H.265/HEVC video compression, inverse quantization and transform, functional verification, throughput.

1. Introduction

In recent couple of years back, mobile equipment (ME) is mainly used for speech purposes. Mobile phones are used to transfer speech data from one device to another. As years passed by, the development in the chip technology has allowed more complex circuits to be implemented on smaller chips known as integrated chips (IC) and this development in chip technology plays a major role in the current generation of mobile equipment where video streaming is in great demand. Mobile equipment in the current generation is not only used for speech transfer but also for watching a video, video telephony, video streaming and live streaming. Video streaming requires a lot of complex circuits, bit rate etc. Implementing these complex circuits requires a lot of space which may not be provided by the mobile telephone manufacturers. The development in the chip technology has helped the mobile telephony manufacturers and researchers working on the video streaming to easily implement

complex circuits on integrated chips which can be easily deployed in the mobile phones. Video telephony can be done through some software's such as for example Skype where the video is compressed to a major extent that is compressed data is transmitted and is displayed to the end user. Video streaming is watching a video sequence from the websites where the videos are uploaded and saved in the website servers. Some of the frequently used video streaming sites. All the video streaming applications require lots of space and bandwidth to be transmitted, but the mobile manufacturers are provided with limited bandwidth and space. Hence video compression is required where the video sequence is compressed to major extent and is transmitted using less bandwidth than what is required for transmitting the uncompressed video sequence. The video researchers are facing a real challenge in fulfilling the requirements of the end user whose ultimate aim is to watch a high quality video sequence. The end users are not interested in knowing about the compression rate, bit rate etc., of the video sequence. Providing a good quality video at lower bit rate, higher compression ratio is a challenging task to the researchers working in video domain. A combination of technology advances, market expansion and increased user expectation is driving more demand for better quality video. Original video sequence requires a lot of storage space and high bandwidth for transmission. Hence the video sequence has to be compressed, encoded and then decoded by the end user to view the video sequence. Compressing a video sequence require software which reduces the storage capacity of the corresponding video sequence and can be transmitted using lesser bandwidth. The compression software or technique consists of an encoder and decoder where the encoder converts video into a compressed format and the decoder convert compressed video back into an uncompressed format. There are a number of video compressing techniques which vary with each other in terms of compression ratio, complexity etc. H.265/HEVC is the latest video compression technique among all the existing compression techniques and has several advantages over them.

2. Literature Survey

In the work done by Pastuszak [6], an intra-encoder that can support 4K video at 30 frames/sec is proposed. The proposed encoder also employs Rate Distortion Optimization (RDO) to determine the best coding mode to use on segmented blocks. The RDO is a process by which every coding decision can benefit from a distortion and bit-rate analysis. This process is computationally intensive since in order to make the most accurate decision on coding mode, every block of pixels would need to be evaluated against all possible coding modes, transformed and entropy encoded. At this point the bit-rate cost and distortion could then be evaluated to determine the coding mode that minimizes distortion while also keeping the bit-rate below a threshold. This computation would negate support for real-time use as elaborated by Pastuszak. The encoder uses a simplified RDO process that leaves out inter coding and pre-selects a smaller set intra modes in order to reduce the sheer number of calculations that must be evaluated.

Braly[18], the motion estimator targets real-time 4K video encoding in a multicore platform, AsAP. The motion estimator is a sub-module within the encoder that is used to determine the

best inter coding mode based on a distortion calculation in this case it is SAD. The motion estimator supports all 35 inter modes and block sizes as defined by the HEVC standard. The work was entered in Verilog RTL, modeled using Matlab and placed and routed using standard cell techniques. The H.265/HEVC standard has introduced a new structure called slices. These are structures that can be decoded independently of other slices in the same picture [1]. These structures are meant to support parallel processing platforms. It may be that the AsAP could be a platform well suited for video compression.

Ziyou[12] also the IDST, both the IDST and the inverse quantization function are implemented in the design presented by this work, the 4x4 hardware could in theory be used to perform an 8x8 inverse transform by copying the 4x4 IDCT so that two 4x4 IDCT would be used to compute the 8x8. This re-using of hardware extends also to the 16x16 and 32x32 transforms.

3. Proposed Methodology

The current design of the 4x4 inverse quantization and inverse transform consists of similar design approaches. The first is the RTL design done in Verilog and then verified with Cadence simulation tool. The second phase consists of using Genus tool to then synthesize the design and produce files for use in the physical implementation of the complete design. Finally, the placement and routing uses files from the synthesis step to produce a placed and routed design. Cadence Innovus was used for placement and routing.

Inverse Quantization is the IDCT undoes the DCT function, the Inverse Quantization module undoes the Quantization function provided in the encoder. Quantization consists of dividing the transformed coefficients by a quantization step size and inverse quantization is done by multiplying by this same step size accordingly. The step size is actually determined by the QP value. This value can range from 0-65. Every increase of one in Quantization parameters corresponds to an increase of 14% in the step size. In addition to providing a means to undo a division operation, the de-quantizer also supports frequency scaling lists. These lists allow for frequency components to be divided by different amounts. In typical use the higher frequency components will be divided by larger numbers. These lists can be either a default list defined by the standard or custom lists which must be sent to the encoder during the quantization operation or transmitted in the bit stream for decoder use. The proposed design supports all three list modes, no list, default and custom. The mode is determined by writing to the control register in the control module. The level [x][y] corresponds to transformed and quantized input data and w [x][y] is the scaling list either custom or default. The value of g is used to map the quantization parameter value to a set of eight values and a corresponding shift. The offset is given for a specific bit depth and transform size. The value of shift1 is equal to (M – 5 + B) where M is the log2 (transform size) and B is bit depth. The need for shift1 is driven by the desire to maintain the norm for the residual block as it undergoes inverse quantization and transformation.

This module instantiates all of the other modules. It also instantiates registers used to capture results between modules as well as input registers before the de-quantizer and output registers

after the IDCT module. These data registers are used to provide some pipelining and to enhance usability when integrating with a larger in system on chip design.

4. Experimental Results

The current module undergone through the Simulation each Verilog module has a corresponding test bench that was used to verify proper functionality using Cadence Incisive simulation tool. A top level test bench was then used to instantiate all the modules and test end to end. This top level test bench was then simulated to verify functionality for various modes of operation including custom frequency scaling lists, quantization parameter values and other supported different modes. The first step in processing 4x4 blocks is to configure the various parameters of the inverse quantization and transform. This is done by writing to the control register and if enabled, writing to the ram module with a custom scaling list.

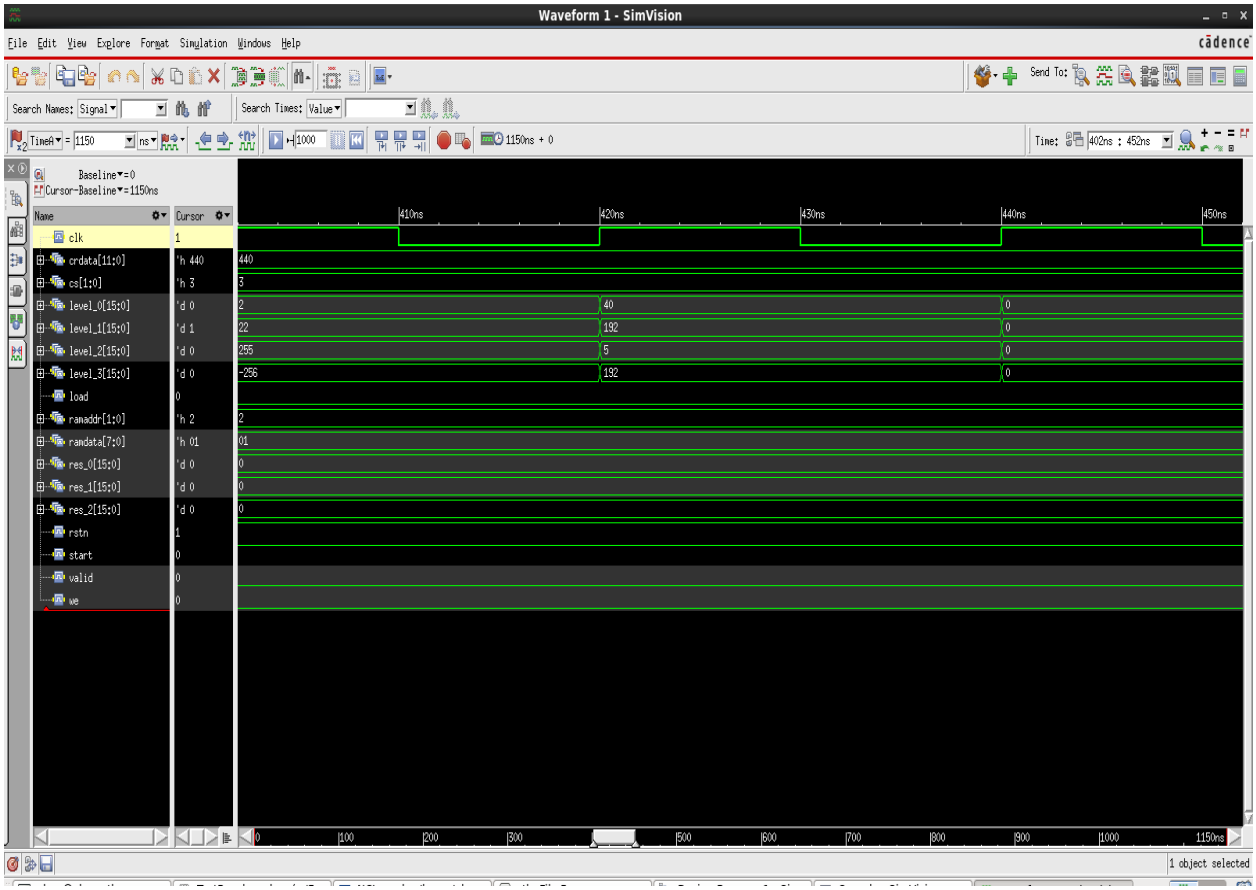

Figure 1: Simulation showing writing to ram module in dequantizer

In Figure 2, the custom scaling list is shown being written into RAM memory and these stored values will then be used to scale the coefficient data on a one for one basis provided the control register is setup to use the scaling list. Thus for a 4x4 inverse operation sixteen values are written into memory. The actual inverse quantization and transformation are initiated by asserting the start signal high. In Figure 2 this assertion event is shown along with the input data being driven on the level_0-3 signals. The output data is shown on the res_0-3

signals and represents the residual pixel data. The valid signal is also output and validates the data for a succeeding decoding step.

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
coeff1_ld_reg[13]/CK				0		0	R
coeff1_ld_reg[13]/Q	SDFFRHQX1	2	4.5	23	+146	146	F
coeff1_ld_reg[13]/D	SDFFRHQX1				+0	146	
coeff1_ld_reg[13]/CK	setup			0	+92	238	R

Figure 2: Simulation showing residual output with delay

These current valid results were cross-checked with MATLAB. Using MATLAB a script was written that called various functions to compute and compare both intermediate and final output values with the Verilog simulations. The MATLAB script and functions were implemented using integer math so as to produce results which could be directly compared to the HDL results. The MATLAB files work as follows the script rcArray Function's requires three inputs: the input array, scaling array, and the quantization parameter factor. The scaling is then applied based on the scaling array. The rcArray Function then calls the de-quantization function. Main_Dequantize, followed by the inverse transform function and the current 4x4 Function. The final valid results are stored in an array called residue Array.

5. Conclusion

In order to achieve High performance for video compression of the Inverse quantization and inverse transform is identified in this current research work that is used for the H.265/HEVC Video compression. The developed architecture is designed to support all H.265/HEVC Transform Unit identified sizes: 4 × 4, 8 × 8, 16 × 16 and 32 × 32. The current architecture is used between the inverse quantization and the 1D-IDCT/IDST to achieve a higher frame rate of up to 1090 p at 35 fps at 200 MHz and 1080 p at 40 fps at 220 MHz were achieved when simulation was achieved in 45nm technology in standard-cell, respectively. Finally, the experimental results demonstrate that the above designs were enhanced by more than 80% in terms of the run-time speed relative to the existing solution. Besides, the power consumption of the current designs was reduced by nearly 70% compared with the other methods.

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