Ultra-Low-Power Functional VLSI Chip Using Mirror-Amplifier

Rishikesh Kumar Thakur

Abstract

Device density in VLSI today enforces the process of chip designing much more complex; whereas MAGIC CAD tools made the IC design in this work, comparatively easier. Study on various amplifiers for sensor applications showed that their powers ranged from a few milliamperes to a few hundred milliamperes at the submicron fabrication processes by MOSIS, but within the affordable cost. Objectives of lowering the power at least by 1000 times in those fabrication processes engaged this research towards completing a new design, called the mirror-amplifier. This design is verified for precise functional behavior for the sensor and total power consumption, using MAGIC extractor and PSPICE electrical simulation tools. A compact model chip layout made silicon area more efficient for MOSIS tiny-chip fabrication in 0.6µm processes. To make even more economical, a multi-die placement technique was applied to the chip layout for this tiny-chip in silicon area of 1500µmX1500µm. MOSIS design rules for multi-die fabrication was verified for process scribe-lines and die packaging. This paper presents details of the key research works, results, completed chip layout and packaging of the chip.

Key words: Mirror-Amplifier; Compound Device; Mixed-Signal Chip; Precision Sensor; Chip Package.

1. INTRODUCTION

As MOS Integrated Circuits (ICs) have come to dominate analog, digital, and mixed-signal electronic circuit designs over the last 15 years [1], the pressure to reduce system cost has favored all-CMOS solutions over systems that mix bipolar and CMOS chips or use Bi-CMOS technology [2]. In current design practices, bipolar devices are usually found only in very-high performance wired and wireless designs, where extreme device specifications (high f_t, low noise, and superior matching) require high-yielding, power-efficient components [3]. Similarly, compound semiconductor devices are used only in the case of very high-speed circuits in applications running at GHz level with low power [1]. With a continuing reduction of MOS transistor channel lengths, modern CMOS silicon processes offer transistor with a higher cut off frequencies [4]. So as it is known that CMOS technology is capable to implement radio frequency (RF) transceivers, recently many researches on radio frequency (RF) ICs in GHz-level-band have been accelerated because of the potential Industrial, Scientific, and Medical (ISM) band and the wireless vehicular radar applications [5-6, etc.]. CMOS processes that have been developed primarily for logic are now also used as amplifier and sensor [7]. Several researchers have presented CMOS amplifiers for an optical receiver with external photo detectors [8-10, etc.]. Most of these amplifiers depend on analog CMOS process technologies. Recently, there have been attempts to use standard digital CMOS technologies since there are more demands to have analog and digital circuits on same chip allowing a very high bandwidth and very low power at the same time [10].

Today’s electronics industry is increasingly focused on the consumer marketplace, which requires low-cost high-volume products to be developed very rapidly. This, combined with advances in deep sub-micron technology has resulted in the ability and the need to put entire systems on a single chip. As more of the system is included on a single chip, it is very likely the chip will contain both analog and digital sections, which make the IC, design procedure a lot more complex [11]. The increasing complexity and decreasing feature size have made the demand of IC products more compact with more facilities and low power and fabrication cost. With this thought as a goal, this paper presents a proposal of ultra low power mixed signal mirror- amplifier with its VLSI design and packaging that can be used as precision sensor. The proposed circuit is basically composed of two differential amplifiers as mirror-amplifier having a NAND gate between them. Hence the designed chip is composed of both analog and digital signal handling capability with high bandwidth (GHz).

In science and industry, accuracy is the degree of conformity of a measured or calculated quantity to its actual, nominal, or some other reference value. We cannot have accuracy without precision. Precise characterization to the degree of mutual agreement requires a series of individual measurements, values, or results. Op-amp with high DC open-loop gain combined with low input offset voltages and offset bias currents can be used as precision sensor [12]. In this study CMOS differential amplifiers have done this job with mirror architecture.

2. CIRCUIT DESIGN

The figure 1 represents the schematic of the mirror-amplifier circuit. Construction of this circuit consists of two differential amplifiers creating mirror architecture and a NAND gate between them makes it also digital compatible. It contains total of 14 MOS transistors in which 6 of them are p-MOS (M1-M6), and rest 8 are n-MOS (M7-M14). The operation of the circuit is done by total of five input terminals (Vsensor, Vbias, Clock, and two ChipEN) and one output terminal Vout with constant DC supply of 5V.

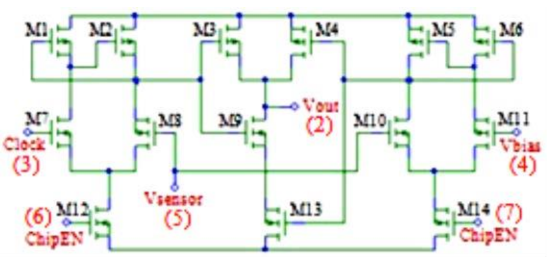

Fig 1: PSpice schematic of the mirror-amplifier.

3. CIRCUIT LAYOUT

To design the concerned schematic of mirror-amplifier in VLSI layout structure MAGIC 7.5 is used with the process configuration of 0.6µm that is supported by MOSIS with a package of 1500µmX1500µm tiny-chip die. The figure 2 below represents the VLSI layout of the mirror-amplifier. The total design of the circuit layout consists of 3 portions, where 2 of them are differential amplifiers acting as input stage with mirror architecture and the rest-one is output stage in the form of NAND gate. Dimensions of MOS transistors are chosen according to the requirements of optimization. Lengths of all MOS transistors are same that is 2λ but for the input stage the ratio of p-MOS to n-MOS widths is 6:3 and for the output stage is 12:6. For designing a single transistor, p- diffusion and n-diffusion are used for p-MOS and n-MOS respectively with poly-silicon to make the gate. In the whole circuit layout layer-1 and layer-2 metals are used for connecting nodes (wires), where poly contact, p-diffusion contact, n-diffusion contact and via-1 contacts are needed as contact materials. The layout has area of 126λX59λ or 37.8µmX17.7µm in 0.6µm CMOS process.

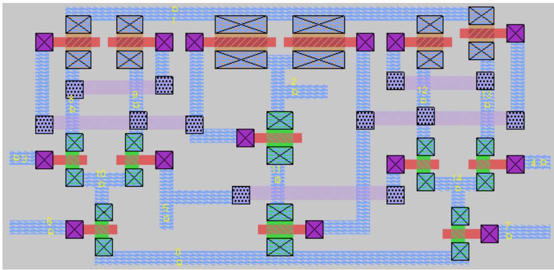

Fig 2: VLSI layout of the mirror-amplifier.

4. SIMULATION RESULTS

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To verify the circuit operation and get the output toggle point for an optimized precision sensing operation towards ultra low power dissipation, simulation is done in two steps in this study. In the 1st step, Output is taken with respect to node 4 with 0.9V DC (threshold) supply at node 5 and 0V to 2.5V clock pulse at node 3. In this case output toggles and get steady at 2.5V (above threshold) giving a power dissipation of 8.41 milliwatts. It is found that Hysteresis at threshold voltage level causes dynamic power loss [13]. This design has flexibility of voltages to bias CMOS circuitry.

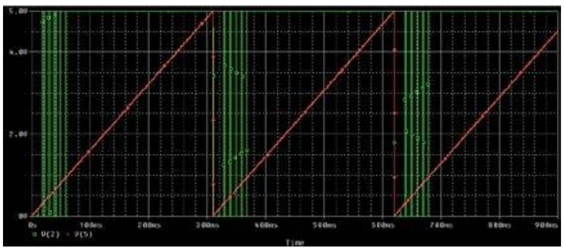

Fig 3: 1st step simulation result from the MAGIC extraction file of the designed layout using PSpice.

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In the 2nd step, output is taken with respect to node 5 with 2.5V DC supply at node 4 that is got in the 1st step. Clock pulse is still 0V to 2.5V. In this case output toggles and get steady at 0.9V that is the threshold voltage of MOS transistor. Power dissipation is 9.13 nanowatts in this case. Thus system is improved for ultra-low-power operation.

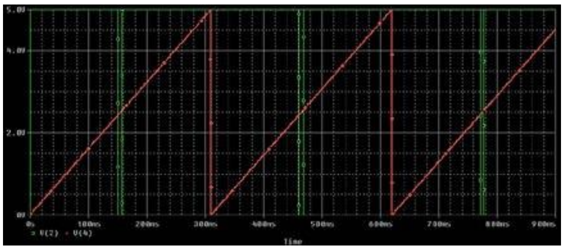

Fig 4: 2nd step simulation result from the MAGIC extraction file of the designed layout using PSpice.

One of the goals of this paper is to achieve low-power circuit designs, which already satisfied in the 1st step simulation techniques. But it showed sign of dynamic power losses due to Hysteresis. Among several solution of Hysteresis, one is adding external feedback resistor to the chip. The 2nd step simulation technique was taken for the better operation of the designed circuit. This way the output becomes single shot output as the sensor voltage ramps from 0V to 5V.

5. CHIP LEVEL DESIGN

The chip level design procedures come with the steps of pad frame design, pin configuration, floor planning etc. Pad is designed with the dimension of 90µmX90µm according to the MOSIS specifications and 60µmX60µm glass opening over the pad for bonding purpose [14]. The pad frame consists of 16 pads in total. The designed mirror- amplifier is set in the pad frame that consumes total of 1967λX1967λ or 590.1µmX590.1µm in CMOS 0.6µm processes. So for multi-die placement for economical consideration, the total silicon size (MOSIS Tiny Chip at 0.6µm process) of 1500µmX1500µm is divided into 4 sub-dies with the scribe lines of 50µm. Hence the total area needed for this multi-die placement is 1380.2µmX1380.2µm which is very efficient for this design.

Floor planning can be done manually by hand, or by using interactive tools. In this study floor planning is done manually and then implemented by MAGIC. Total pin configuration of the multi-die placement is given in the table 1, and figure 5, 6 represent the view of the complete ICs as floor- planned with single mirror-amplifier and dual mirror-amplifier respectively.

Table 1: Pin configuration

Die	Modules	Pin Name	Pad #
Sub-die # 1,2	Single mirror-amplifier	Vdd	4
		GND	13
		EN1	16
		EN2	3
		Clock	1
		Bbias	2
		Vsensor	15
		Vout	14
	NAND gate	Vdd	4
		GND	13
		In1	6
		In2	8
		Vout	7
	Sense amplifier	Vdd	4
		GND	13
		EN	11
		Q	12
		Qbar	10
		Vout	9
Sub-die # 3,4	Mirror-amplifier#1	Vdd	4
		GND	13
		EN1	16
		EN2	3
		Clock	1
		Bbias	2
		Vsensor	15
		Vout	14
	Mirror-amplifier#2	Vdd	4
		GND	13
		EN1	10
		EN2	7
		Clock	11
		Bbias	6
		Vsensor	9
		Vout	8
	Inverter	Vdd	4
		GND	13
		In	12
		Vout	5

Figure 5 represents the chip layout of a single mirror-amplifier with an extra NAND gate and a Sense Amplifier. This chip is placed in the top sub- dies (die # 1 and 2). NAND gate is designed with larger width for higher current driving purposes. It can also be used as inverter by tying two inputs. So it can work as inverted output buffer. Also it can be connected to the output pin of the mirror-amplifier to have halt-run feature. The logical operation of this halt-run operation is given in the table 2. The output of the amplifier can be halted by logic '0' and be running by '1'. Both NAND and the Sense Amplifier can be used for electrical characterization purposes after fabrication.

Table 2: Halt-run operation of the sub-die # 1 and 2

Halt Bit to NAND Input1	Mirror-Amp Out Bit to NAND Input2	NAND Output	Status
0	1	1 (no-change)	Halt
0	0	1 (no-change)	Halt
1	0	1 (inverted)	Run
1	1	0 (inverted)	Run

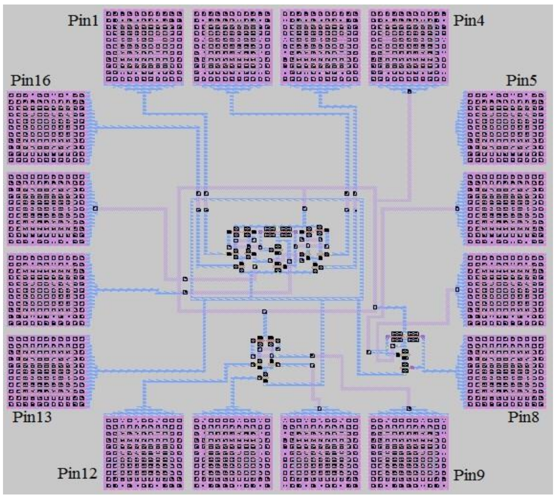

Fig 5: Sub-die chip layout of a single mirror-amplifier with a NAND gate and a Sense amplifier

Figure 6 shows the chip layout of dual mirror-amplifier with an extra inverter. This chip is to be placed in sub-die # 3 and 4. The inverter is also designed with larger width for higher current driving purposes. It can be used when the output of the mirror-amplifier needs to be inverted.

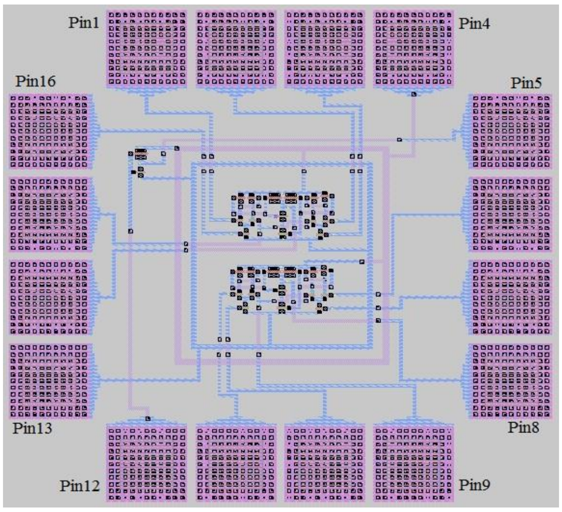

Fig 6: Sub-die chip layout of dual mirror-amplifier with an additional inverter

6. CHIP PACKAGING

The package serves a variety of important needs. Its pins provide manageable solder connections. It gives the chip mechanical support. It conducts heat away from the chip to the environment [15]. The package structure corresponding to the designed chip layout can be served by MOSIS. For this design purpose a plastic compound-molding package is chosen from MOSIS in which the pads are connected to the package leads by gold bonding wire. It is an open cavity (where die sits in and then bonded) package with lid. Top of packaged chip called the lid and it is loose to be opened. This gives advantages to go in the package and complete special electrical tests like: die probing (electrically connected needles touching components on silicon), component thermal tests, microscopic visual tests like damage by short circuit, moisture effect tests etc. The table 3 below shows the other identifications of the chosen package, and the figure 7 and 8 show the designed multi-die chip after cut along the scribe lines. Those separated 4 sub-dies are placed in the package individually.

Table 3: Identifications of the chosen package

Package part number	OCP_QFN_5X5_16A
Package manufacturer	SEMPAC
Package size	5mmx5mm
Die placement cavity	3.1mmx3.1mm
Pins	16

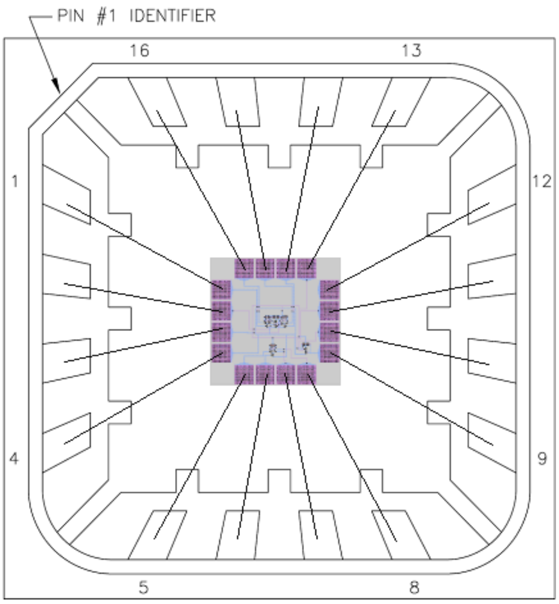

Fig 7: Bonding diagram of the single mirror-amplifier sub-die in SEMPAC package

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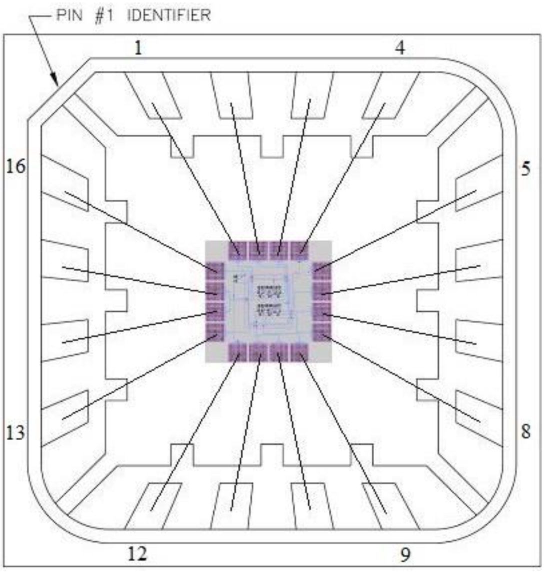

Fig 8: Bonding diagram of the dual mirror-amplifier sub-die in SEMPAC package

7. CONCLUSION

The VLSI technology is going to enter in the nano-tech era. With the practice of designing nano-power chip many problems are raised and power managing challenge is got tougher. In this study an ultra-low-power mirror-amplifier is designed in CMOS 0.6µm process for precision sensing application, which dissipates power of 8.41 milliwatts in the 1st experiment and latter 9.13 nanowatts in the 2nd experiment by choosing the correct biasing setups. For economic consideration multi-die placement is done with a suitable package by SEMPAC. Four sub-dies are designed in two groups for characterization purposes. One design has a NAND buffer that can provide an additional operation for halt and run functions. Further study may be focused on more enhanced mirror-amplifier design with more efficiency and power reduction.

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