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Nano-Power Sensor Applications in VLSI Multi-Die Tiny Chip

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Abstract

Semiconductor integration has improved over the years by increasing device switching speed and device density, causing increased power consumption and dissipation; therefore, the issues has been considered and improved here. Previously designed VLSI mirror-amplifier had power dissipation of 8.41 milliwatts in CMOS 0.5µm process. Latter the technique was re-applied in this work to completed characterization of each pin signal functions with biasing steps to determine accuracy at the low power response of the IC in order to improve the total power consumption. Signal pin orientation in the simulation and choosing the correct biasing point in two steps proved to be correct procedure to improve. Supply voltage was considered as 3V for the MOSIS process technology. Latest MAGIC layout CAD tools were used for design, and PSPICE was used for simulation and electrical characterization with the help of MAGIC layout extraction tool. Keeping the process and scaling unchanged at 0.5µm as the previous design, the new VLSI design yielded the power dissipation of 4.39 nanowatts in 2nd step by reducing the dynamic loss. The electrical characterizations also confirmed that the chip precisely senses ultra-high-Z signals at inputs for this application. Multi-die chip placement is done for fabrication and also made the final product less expensive by the in-house custom designed pad-frame. This paper presents details of the key research works, results, completed chip layout and applications of the chip.

Keywords—*Nano-Power VLSI; Mirror-Amplifier; Mixed- Signal Applications; MOSIS Tiny-Chip; MOSIS CMOS Design; Multi-Die Placement.*

I. INTRODUCTION

As MOS Integrated Circuits (ICs) have come to dominate analog, digital, and mixed-signal electronic circuit designs over the last 15 years [1], the pressure to reduce system cost has favored all-CMOS solutions over systems that mix bipolar and CMOS chips or use Bi-CMOS technology [2]. In current design practices, bipolar devices are usually found only in very-high performance wired and wireless designs, where extreme device specifications (high f_t, low noise, and superior matching) require high-yielding, power-efficient components [3]. Similarly, compound semiconductor devices are used only in the case of very high-speed circuits in applications running at GHz level with low power [1]. With a continuing reduction of MOS transistor channel lengths, modern CMOS silicon processes offer transistor with a higher cut off frequencies [4]. So as it is known that CMOS technology is capable to implement radio frequency (RF) transceivers, recently many researches on radio frequency (RF) ICs in GHz-level-band have been accelerated because of the potential Industrial, Scientific, and Medical (ISM) band and the wireless vehicular radar applications [5-6, etc.]. CMOS processes that have been developed primarily for logic are now also used as amplifier and sensor [7]. Several researchers have presented CMOS amplifiers for an optical receiver with external photo detectors [8-10, etc.]. Most of these amplifiers depend on analog CMOS process technologies. Recently, there have been attempts to use standard digital CMOS technologies since there are more demands to have analog and digital circuits on same chip allowing a very high bandwidth and very low power at the same time [10].

Today's electronics industry is increasingly focused on the consumer marketplace, which requires low-cost high-volume products to be developed very rapidly. This, combined with advances in deep sub-micron technology has resulted in the ability and the need to put entire systems on a single chip. As more of the system is included on a single chip, it is very likely the chip will contain both analog and digital sections, which make the IC, design procedure a lot more complex [11]. The increasing complexity and decreasing feature size have made the demand of IC products more compact with more facilities and low power and fabrication cost. With this thought as a goal, this paper presents a proposal of nano-power mixed signal mirror-amplifier with its VLSI design that can be used as precision sensor. The proposed circuit is basically composed of two compact sense amplifiers placed as mirrors to each other for I/O. A NAND gate is placed in between these amplifiers' outputs. Hence the designed chip is composed of both analog and digital signal handling capability.

II. CIRCUIT DESIGN

The Figure 1 represents the schematic of the mirror-amplifier circuit, which is designed by Dr. Shuza Binzaid. Construction of this circuit consists of two compact circuits of sense amplifiers creating mirror architecture and a NAND gate in between them. Analog inputs are placed at these sense amplifiers. The output is the NAND output here. Thus this circuit also becomes digital compatible. Thus it becomes a mixed signal chip. It contains total of 14 MOS transistors in which 6 of them are p-MOS (M1-M6), and rest 8 are n- MOS (M7-M14). The operation of the circuit is done by total

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of five input terminals; Vsensor (node 5), Vbias (node 4), Clock (node 3), and two ChipEN (node 6 & 7) and one output terminal Vout (node 2). It is powered by a constant DC supply of 3V.

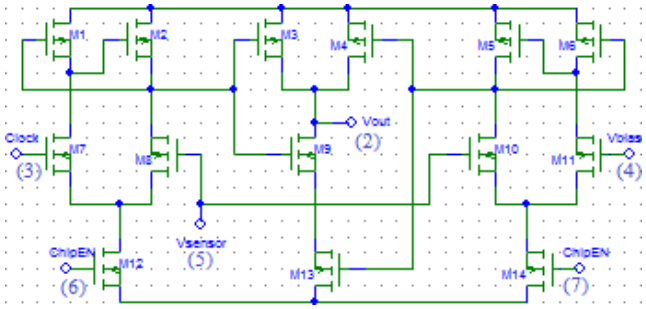

Figure 1. PSpice schematic of the mirror-amplifier.

III. LAYOUT DESIGN OF THE CIRCUIT

To design the concerned schematic of mirror-amplifier in VLSI layout structure MAGIC 7.5 is used with the process configuration of 0.6µm (in layout design) that is supported by MOSIS with a package of 1500µmX1500µm tiny-chip die. The figure 2 below represents the VLSI layout of the mirror-amplifier. The total design of the circuit layout consists of 3 portions, where 2 of them are differential amplifiers acting as input stage with mirror architecture and the rest-one is output stage in the form of NAND gate. Dimensions of MOS transistors are chosen according to the requirements of optimization. Lengths of all MOS transistors are same that is 2λ but for the input stage the ratio of p-MOS to n-MOS widths is 6:3 and for the output stage is 12:6. For designing a single transistor, p-diffusion and n-diffusion are used for p-MOS and n-MOS respectively with poly-silicon to make the gate. In the whole circuit layout layer-1 and layer-2 metals are used for connecting nodes (wires), where poly contact, p-diffusion contact, n-diffusion contact and via- 1 contacts are needed as contact materials. The layout has area of 126λX59λ or 37.8µmX17.7µm in 0.6µm CMOS design process.

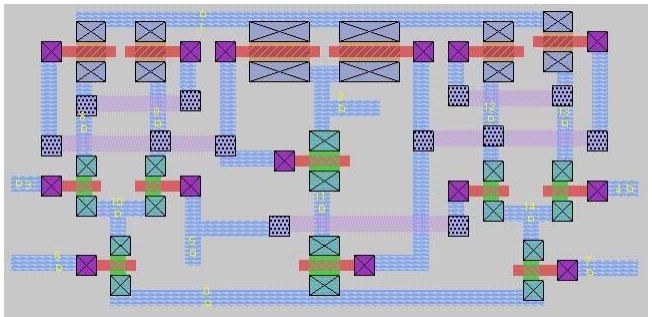

Figure 2. VLSI layout of the mirror-amplifier.

IV. SIMULATION RESULTS

This versatile design has shown the concept to be accurate where it was improved from milliwatt to nanowatt power dispassion by reducing dynamic power loss.

To verify the circuit operation and get the output toggle point for an optimized precision sensing operation towards nano-power dissipation, simulation is done in two steps in this study. In the 1st step, Output is taken with respect to node 4 with 0.4V DC (below threshold) supply at node 5 and 0V to 1.5V clock pulse at node 3. In this case output toggles and get steady at 1.4V giving a power dissipation of 1.66 milliwatts. It is found that Hysteresis at threshold voltage level causes dynamic power loss [13]. This design has flexibility of voltages to bias CMOS circuitry.

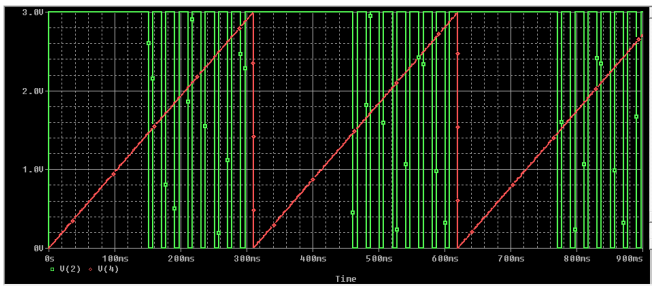

Figure 3. 1st step simulation result from the MAGIC extraction file of the designed layout using PSpice.

In the 2nd step, output is taken with respect to node 5 with 1.4V DC supply at node 4 that is got in the 1st step. Clock pulse is still 0V to 1.5V. In this case output toggles and get steady at 0.18V that is the threshold voltage of MOS transistor. Power dissipation is 4.39 nanowatts in this case. Thus system is improved for our desired operation.

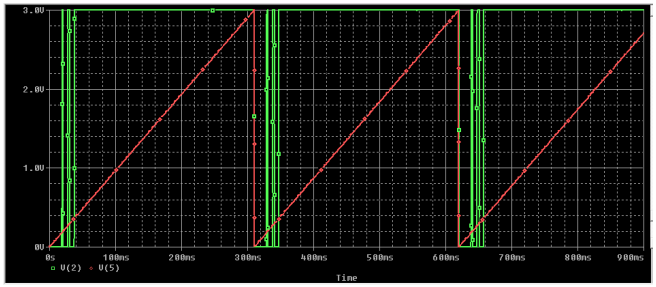

Figure 4. 2nd step simulation result from the MAGIC extraction file of the designed layout using PSpice.

The major goal of this study is to achieve nano-power circuit designs is satisfied in the 2nd step simulation techniques. But the 1st step showed a sign of dynamic power losses due to Hysteresis. Among several solution of Hysteresis, one is adding external feedback resistor to the chip. The 2nd step simulation technique is taken for the better operation of the designed circuit. This way the output becomes single shot output as the sensor voltage ramps from 0V to 3V.

V. CHIP LEVEL DESIGN

The chip level design procedures come with the steps of pin configuration, pad frame design, floor planning etc. Pad is designed with the dimension of 90µmX90µm according to

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the MOSIS specifications and 60µmX60µm glass opening over the pad for bonding purpose [14]. The pad frame (in Figure 5) consists of 16 pads in total. The designed mirror-amplifier is set in the pad frame that consumes total of 1967λX1967λ or 590.1µmX590.1µm in CMOS 0.6µm design process. So for multi-die placement for economical consideration, the total silicon size (MOSIS Tiny Chip at 0.5µm or 0.6µm process) of 1500µmX1500µm is divided into 4 sub-dies with the scribe lines of 50µm. Hence the total area needed for this multi-die placement is 1380.2µmX1380.2µm which is very efficient for this design. Floor planning can be done manually by hand, or by using interactive tools. In this study floor planning is done manually and then implemented by MAGIC. Total pin configuration of the multi-die placement is given in the Table 1. To accommodate all necessary signal pins in the sub-die for MOSIS tiny silicon chip size, the layout is configured to have maximum of 16 pins for the package. Thus four dies could be placed in the silicon and two types of layout is placed in the tiny chip. Figure 6, 7 represent the view of the complete ICs as floor-planned with single mirror-amplifier and dual mirror-amplifier respectively.

TABLE 1. PIN CONFIGURATION

Die	Modules	Pin Name	Pin #
Sub-die #1,2	Single mirror-amplifier	Vdd GND EN1 EN2 Clock Bbias Vsensor Vout	4 13 16 3 1 2 15 14
	NAND gate	Vdd GND In1 In2 Vout	4 13 6 8 7
	Sense amplifier	Vdd GND EN Q Qbar Vout	4 13 11 12 10 9
Sub-die #3,4	Mirror-amplifier#1	EN1 EN2 Clock Bbias Vsensor Vout	16 3 1 2 15 14
	Mirror-amplifier#2	EN1 EN2 Clock Bbias Vsensor Vout	10 7 11 6 9 8
	Inverter	Vdd GND In Vout	4 13 12 5

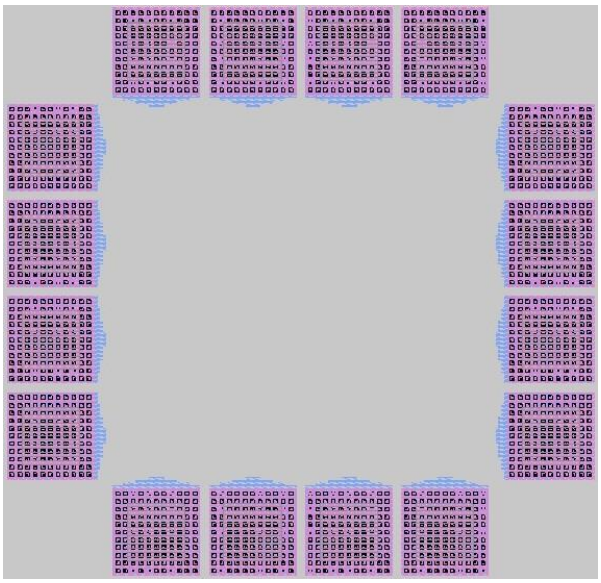

Figure 5. 16 pin pad frame with the designed three metal layer pads.

Figure 6 represents the chip layout of a single mirror-amplifier with an extra NAND gate and a Sense Amplifier. This chip is placed in the top sub-dies (die #1 and 2). NAND gate is designed with larger width for higher current driving purposes. It can also be used as inverter by tying two inputs. Also it can be connected to the output pin of the mirror-amplifier to have halt-run feature. The logical operation of this halt-run operation is given in the Table 2. The output of the amplifier can be halted by logic '0' and be running by '1'. Both NAND and the Sense Amplifier can be used for electrical characterization purposes after fabrication. In this operation, Halt bit is considered as the output only control bit of the mirror-amplifier.

TABLE 2. HALT-RUN OPERATION OF THE SUB-DIE # 1 AND 2

Halt Bit to NAND Input1	Mirror-Amp Out Bit to NAND Input2	NAND Output	Status
0	1	1 (no-change)	Halt
0	0	1 (no-change)	Halt
1	0	1 (inverted)	Run
1	1	0 (inverted)	Run

Figure 7 shows the chip layout of dual mirror-amplifier with an additional inverter. This inverter functions as providing complemented data output and also its drive current are high that is applicable in certain electronic circuit operations. This chip is to be placed in sub-die #3 and 4. The inverter is also designed with larger width for higher current driving purposes. It can be used when the output of the mirror-amplifier needs to be inverted externally through chip-packaged pins by simply connecting the output of the mirror-amplifier and input of the inverter.

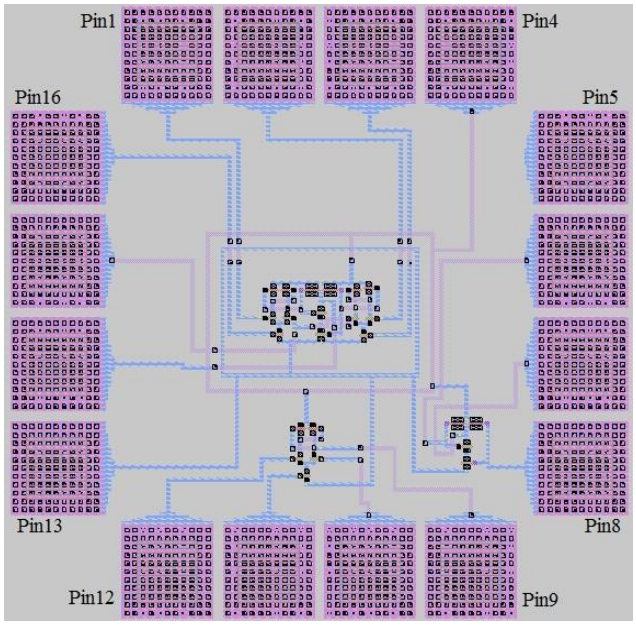

Figure 6. Sub-die chip layout of a single mirror-amplifier with a NAND gate and a sense amplifier.

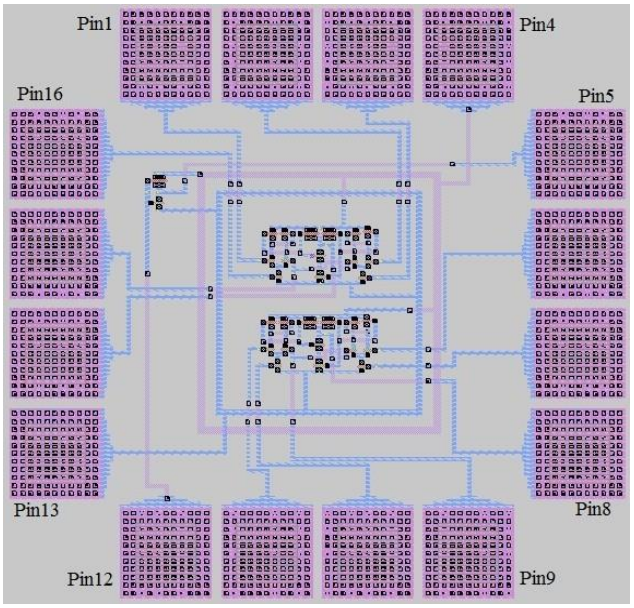

Figure 7. Sub-die chip layout of dual mirror-amplifier with an additional inverter.

VI. CHIP PLACEMENT

As it is mentioned that for cost effective fabrication and speed concern, multi-die placement is chosen, this is why MOSIS multi-die placement specifications are followed for their tiny chip area. Figure 8 represents the specifications that are followed in this work for final placement. In this figure the line at the die perimeter and the line among the sub-dies (chip) are called scribe lines. The dimensions of sub-dies and scribe lines are mentioned before like, the total silicon size (MOSIS Tiny Chip at 0.5µm or 0.6µm process) of 1500µmX1500µm is divided into 4 sub-dies with the scribe lines (A distance is maintained to separate dies on silicon through a cutting process. These cutting lines are called scribe lines) of 50µm. Hence the total area needed for this multi-die placement is 1380.2µmX1380.2µm.

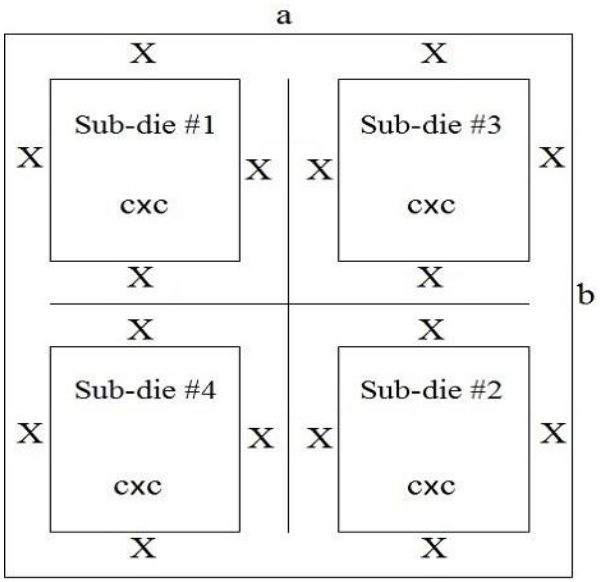

Figure 8. Block diagram of multi-die placement according to MOSIS.

VII. APPLICATIONS

It is proposed that the designed precision sensor can be practically applicable in the following areas as it has very low power dissipation, less area requirements, low sensing and biasing points:

A. In SRAM, DRAM

For contemporary memories, array structures and periphery circuits, such as decoders, charge pumps, level shifters, and sense amplifiers, determine the overall system performance in terms of power dissipation and access speed. The high-speed low-power sense amplifier is one of the critical components. Due to low-voltage operation, current sensing techniques have received a lot of attention in the last decade [15]. Many sense amplifiers based on cross-coupled transistor structures were designed to overcome the loading effects for DRAM or SRAM [16]. However, SRAM design is constrained by its compact area requirement, which forces the use of near minimum sized transistor for the memory cell design, and designing high speed sense-amplifier circuit is a challenge, particularly for large SRAM designs are realized in CMOS technology. This low power mirror-amplifier is certainly an upgrade to those of such designs for the future where biasing is absolutely crucial in high-speed designs.

B. In Flush Memory

Another category of memories is flash memory. The trend is not only high-density and low-voltage, but also multi-level. Therefore, the threshold voltage deviation of the programmed memory cells has to be well controlled for low-

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voltage operation. The sense amplifiers require high sensitivity and excellent mismatch immunity in threshold voltage and (channel width/channel length) ratio of devices. For flash memories, comparison of current difference between the flash cell and the reference cell is the direct and fast method to read the data [15].

C. In MRAM

Magnetic random access memory (MRAM) is a promising low-power nonvolatile memory technology that may one day supplant FLASH and DRAM.

D. In Biomedical

Biomedical devices need to be very sensitive in detection of a specific signal from tumors or any other diseases alike. Perfection of that devices are improved by the perfection of the sensor circuit, and applications of that devices get flexible and expanded by the optimization and decreasing the sensor circuits' power dissipation and area consumption.

E. In Botany

In botany, precision sensors are also needed to sense the p^H level of plants and get some automated services based on the sensed p^H level.

F. In Communication and Defense

Besides, communication networks like, BTS or satellite needs precision sensor to measure the perfection of the signals and the strength level of the signals. Precision sensors are also applicable in national defensive networks or in defensive war arms.

VIII. CONCLUSION

With the practice of designing low-power chip many problems are raised and power managing challenge is got tougher as we are already in pre-nano-tech era. In this study a nano--power mirror-amplifier is designed in CMOS 0.6µm (in layout design, for mask design it is 0.5µm) process for precision sensing application, which dissipates power of 1.66 milliwatts in the 1st experiment and latter improved to 4.39 nanowatts in the 2nd experiment by choosing the correct biasing setups. For economic viability, a challenging design technique of multi-die placement is completed and explained for safe die separation technique by scribe lines position in tiny chip silicon. Four sub-dies are designed in two groups for characterization purposes. The design has a NAND buffer that can provide an improved operation of Halt and Run functions of the output only control bit, and with the large aspect ratio it can drive large load also. Another design has two mirror-amplifiers together to make chip dual. Further study may be focused on more enhanced mirror-amplifier design with more efficiency, further power reduction and exploring various applications.

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