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Design And Implementation Of A Power Efficient Vedic Multiplier

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Abstract

The ever-increasing demand in enhancing the ability of processors to handle the complex and challenging processes has resulted in the integration of a number of processor cores into one chip. Still the load on the processor is not less in generic system. This burden can be minimized by boosting the primary processor with Co-Processors, which are implemented to work on particular functions like arithmetic computation, Digital Signal Processing, Graphics etc. The speed of ALU majorly depends on the multiplier.
The research has established and analyzed that Nikhilam Navatashcaramam Dashatah Sutra is the most effective Sutra, which gives the minimum of delay for multiplication of all the types of short and long numbers. Further, Nikhilam Navatashcaramam Dashatah Sutra multiplication and implementation of the Verilog HDL coding is done using Xilinx Tool.

Keywords*—Multiply and Accumulate (MAC), Adders, Vedic Multiplier, Array Multiplier*

1. Introduction

The Multiplication has an essential role in fundamental arithmetic operations. Multiply and Accumulate (MAC) based Multiplication operations is used most frequently for computation and it is currently implemented in most of the Digital Signal Processing applications in processors of ALU. As we know the normal multiplication is the most time taking factor in the Digital Signal Processing(DSP) chip so to avoid this the high-speed Vedic Multiplier is implemented to overcome and get the results more hastily. The multiplier is of two types: serial multiplier and parallel multiplier. The parallel multiplier is often preferred because it uses combinational circuits and does not contain any feedback structures.In parallel multiplication, there are of two types namely, array multiplication and tree multiplication. The basic array multiplication, which follows add and shift algorithm is simple and it is widely used in most of the applications due to its structure and less area. But the propagation of carry in each stage produces a considerable delay in the circuit (Sonia Verma et al. 2011).[5]

Damble et al. (2013) compared various array multipliers by calculating propagation delay of all multipliers. Another array multiplier called Braun multiplier is introduced to reduce the carry propagation delay in the simple array multiplication by using carry save adder in each stage instead of carry propagation adder (Anitha et al. 2012). [6]. The number of components and critical path are same assimple array multiplication. To reduce the critical path delay, row bypassing (Manchal Ahuja 2013), column bypassing (Sunil Kumar 2014) and 2-D bypassing were designed to increase the speed. In the bypassing techniques, the delay is reduced. But due to extra circuitry, the area and power are increased (Anitha et al. 2012).[7] Wallace (1964) proposed a tree-based structure to reduce the delay. The reduction of stage delay is in the order of O (log n). Power consumption of this multiplier is less comparedwith array multipliers.

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The partial products are reduced in parallel using a tree of carry save adders. It uses log depth network and tree network for reduction. It is Faster, but its structure is irregular. In the conventional Wallace multiplier, the Ripple Carry Adder is used in the last stage to produce the final product. The Carry Look-Ahead adder can also used to increase the speed. The high-speed Wallace multiplier uses 4:2, 5:2 and 7:2 compressors for the partial product tree reduction (Avinash et al. 2007).[8]

Dadda multiplier is another well-known tree multiplier. It has the same general stages as Wallace tree. But it does not attempt to reduce the partial products in each layer. Many authors presented the analysis of different multipliers based on speed and power using various adders. (Partha Sarathi Mohanty 2009 and Puneet Bhardwaj 2011).[9]

Ridhi Seth (2010) compared floating point adder, subtractor and multiplier for Digital Signal Processing applications. Simran Kaur (2011) combined Booth recoding and Wallace multiplier to low power high speed multiplier using FPGA.Jayashree et al. (2012) tried an attempt to design Booth multiplier for signed numbers and systolic architecture for unsigned numbers. The implementation is done in Xilinx FPGA.[10]

This paper summarizes adetailed literature survey for the investigation about multiplication is presented in this chapter. In addition, the theoretical formulations involved in the various designs are also discussed. The power and speed are a major concern in the design of portable and superfast electronic gadgets. Multiplication is used in Digital Signal Processing, Image processing or arithmetic unitsin the microprocessors and contributeslargely to thepower consumption. The speed, power and area are three important parameters in VLSI design. With advances in technology, many researchers have tried multipliers which offer either of the above-said targets.

2. VEDIC MULTIPLICATION ALGORITHMS

Vedic mathematics - a gift given to this world by the ancient sages of India. A system which is far easiest and more entertaining than modern mathematics. The simplicity of the Vedic mathematics is the calculations can be carried through mentally though the methods can also be written down. There are much more advantages in using a flexible and mental system. Vedic can bedeveloped their own methods; they are not limited to single method. This will make it more creative, interesting and intelligent pupils.

Vedic math refers to the method of calculations based on 16 sutras, asupa-sutrasand their algorithms are derived from these sutras. Any mathematical problems like “arithmetic,algebra, geometry or trigonometry” can be solved mentally by using these sutras.

A. “Nikhilam Navatashcaramam Dasatah” Sutra

The meaning of Nikhilam Sutra is all from nine and last from ten. All cases of multiplication can employ Nikhilam Sutra, it is more effective, when the numbers involved are large. For performs the multiplication operation, first it finds the large numberand compliments it from its nearest base. This multiplication algorithm is less complex for large numbers.

B. “Urdhva-tiryakbyham” Sutra

Urdhva Tiryakbhyam Sutra is applicable to all the cases of multiplication. This sutra performs the multiplication using the principle Vertically and crosswise multiplication. The generation of all the partial products can be done with the concurrent addition. The fig 1 explains coextending in generation of partial products and their summation.

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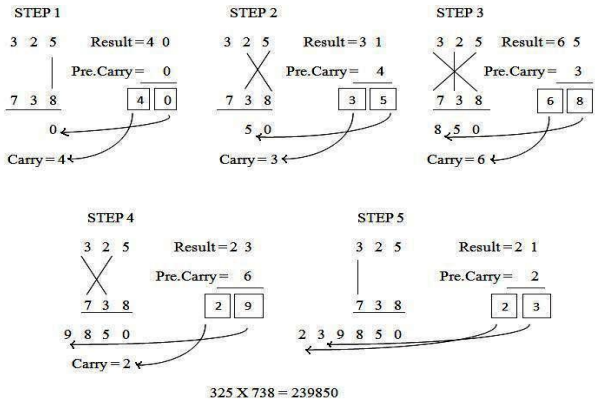

Fig.1: Showing Multiplication of two decimal numbers by Urdhva Tiryakbhyam

The algorithm can be generalized for n x n bit number. The same amount of time will require by this multiplier to calculate the product and thus it is independent of the clock frequency. There is an increase in processing power as a result of high clock frequency. The power dissipation is also increasing which is a disadvantage results in higher device operating temperatures. Through the implementation of Vedic multiplier in processor design the problems are easily overcome and hence the device failure may avoid. The great advantage of this multiplier is gate delay and area increase very slowly with the number of bits increases as compared to conventional multipliers. Hence it is more efficient than conventional multipliers. This architecture is very efficient in the terms of silicon area or speed.

3. Related works

Gokhale & Bahingondu (2015) presented a paper that implements the Vedic multiplier using area efficient carry select adder [1]. The carry select adder is designed using Binary to Excess-one Converter (BEC). The proposed modified CSA based multiplier is compared with Booth multiplier using Xilinx.Anju (2013) compared the performance of Booth multiplier and Vedic multiplier (Urdhava Tiryabhyam) using VLSI technology[2]. The author gave the comparison through the implementation results in Xilinx FPGA. The author concluded that the Vedic multiplier possesses high speed, low area and low power compared with Booth multiplier.Heena Goyal et al. (2015) designed the Vedic multiplier with carry select adder and square root carry select adder [3]. Compared with conventional multipliers, Vedic multipliers occupy less area and delay (Arushi Somani et al. 2012 and Saurabh Sunil Bengali et al. 2011). S.V. Mogre, D.G. Bhalke (2015). "Implementation of High-Speed Matrix Multiplier using Vedic Mathematics on FPGA" [4]. 2015 International Conference on Computing Communication Control and Automation.

A. Performance

- *Power*

Vedic Multiplier requires very less number of gates for given 8x8 bits Multiplier so its power dissipation is very less while compared to other multiplier architecture. Vedic Multiplier has less switching activity as compared to other architecture for same operation.

- *Speed*

Vedic multiplier have high speed compared to array multiplier and Booth multiplier. As the number of bits increases from 16x16 bits to 32x32 bits, the timing delay is reduced to a great extent for Vedic multiplier as compared to other multipliers. Vedic multiplier has the biggest advantage as compared to the other multipliers over gate delays and regularity of layout structure. Delay in the Vedic multiplier for 16 x 16-bit number is 32 ns where-as the delay in the Arrayand Boothmultiplier are 43 ns and 37 ns respectively [12]. Thus, this Vedic multiplier shows the fastest speed among the conventional multipliers.

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- *Area*

The area for Vedic multiplier is very less as compared to other multiplier architectures i.e. the number of devicesareused in the Vedic multiplier are 259 where-asin the Array and Booth Multiplier is 495 and 592 respectively for 16 x 16-bit. Thus, Vedic multiplier is fastest and the smallest of the reviewed architectures. Due to its regular and parallelpattern, this architecture can be easily obtained on silicon and it can work at high speed without increasing the clock frequency. The best advantage is as the number of bits increases, the gate delay and area increase very slowly as compared to the square and cube architectures of other multiplier architecture. Speed improvements are acquired by parallelizing the generation of partial products. It is demonstrated that the design is quite organized in terms of silicon area/speed. Such a design should enable substantial savings of resources in the FPGA when used for image/video processing applications.

4. Methodology and description

A. Implementation

The proposed architecture performs all these operations as mentioned above among these the multiplication and multiplication and accumulation operation uses Vedic multiplier. By using this multiplier, we have reduced the power consumption to maximum extent by reducing the number of computations required to perform the same operation.

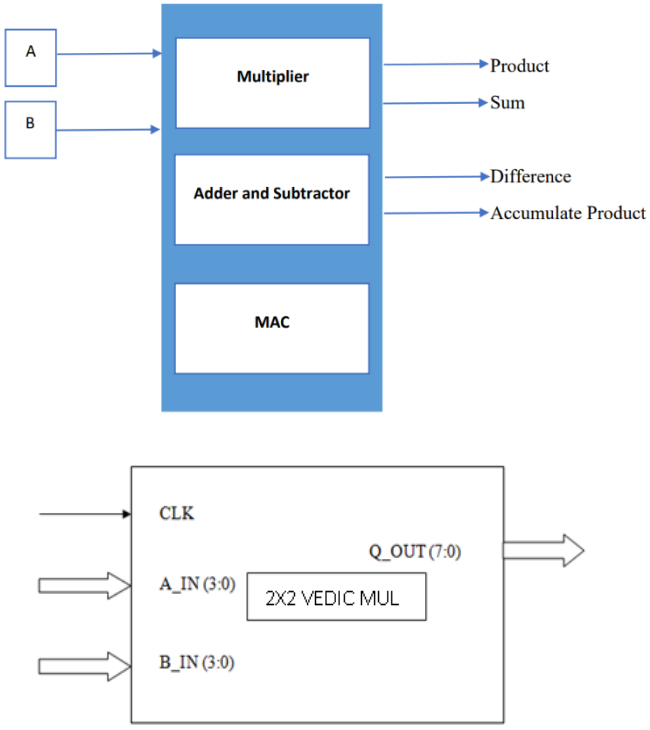

Fig.2. Showing Block diagram of 2x2 Multiplier

A. Implementation Of 2x2 Bits Vedic Multiplier

One-bit multipliers and adders are the basic building blocks of this multiplier. Two input AND gate and for addition full adder can be utilized for performing the one-bit multiplication. Figure 3.2 shows the 2 x 2-bit multiplier.

Let us take the two inputs, each of 2 bits; say A and B. Consideringthe output can be of four digits, say Q3-Q0. As per common method of multiplication, the results are obtained after getting partial product and adding. In Vedic method, Q0 is vertical product of A0 and B0 bits, Q1 is addition 0 crosswise bit multiplication i.e. A1 & B0 and A0 and B1, and Q2 is again vertical product of A1 and

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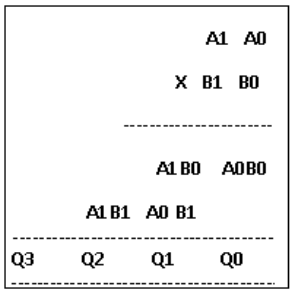
B1 bits with the carry generated, if any from the previous addition during Q1. Q3 output is nothing but carry generated during Q2 calculation. This module is known as 2x2 multiplier block.



B. Implementation Of 8x8 Bits Vedic Multiplier

The 8x8 bit multiplier is build using 4X4 bit blocks. In this the 8-bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Likewise, the multiplicand B can be decomposed into BH-BL. The 16-bit product can be written as:

P = A * B = (AH-AL) * (BH-BL)
P = AH * BH + AH * BL + AL * BH + AL * BL

The outputs of 4X4 bit multipliers are added subsequently to obtain the final product. Thus, in the final stage two adders are also required.

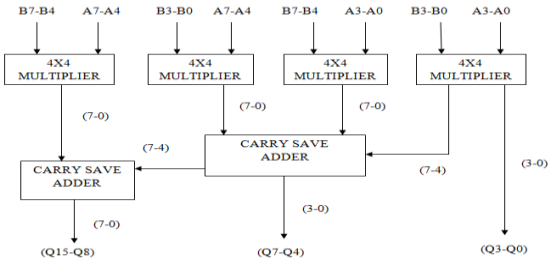


Fig.3. Showing Block diagram of 8x8 Multiplier

RESULT = (Q15- Q8) & (Q7- Q4) & (Q3-Q0)

Now the basic block of 8x8 bits Vedic multiplier is 4x4 bits multiplier which implemented in its structural model. For bigger multiplier implementation like 8x8 bits multiplier the 2x2 bits multiplier units has been used as components which are implemented already Xilinx ISE Tool library. The structural modeling of any design shows fastest design.

C. Ripple Carry Adder

Ripple Carry Adder (RCA) is a basic adder, which contains the series structure of Full Adders (FA); each FA is used to add three bits which consist of carry generated from the previous full adder. This propagation of the carry to successive stages increases the delay with the increase in the number of input bits in RCA

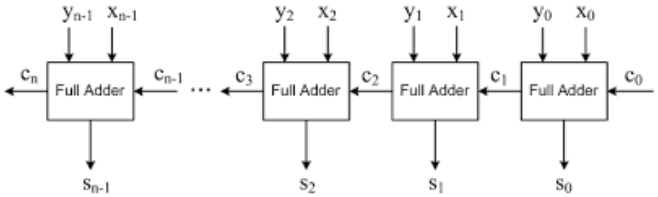


Fig.3. Showing Block Diagram of Ripple Carry Adder block

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D. Carry Save Adder

CSA(also called Wallace tree) performs the addition of m numbers in lesser duration compared to the simple addition. It takes three numbers (a+b+c) to add together and outputs two numbers, sum and carry (s+c). It is carried out in one time unit duration.In carry save adder, the carry(c) is taken until the last step and the ordinary addition carried out in the very last step. This allows the architectures, where a structure of carry save adder is used to calculate the partial products very quick. At last any one basic adder is used to add the last set of carry bits to the last partial products to give the final result of multiplication. Usually, a very fast carry look ahead (CLA) or carry select adder (CSA) is used for this last stage, in order to obtain the optimal performance.

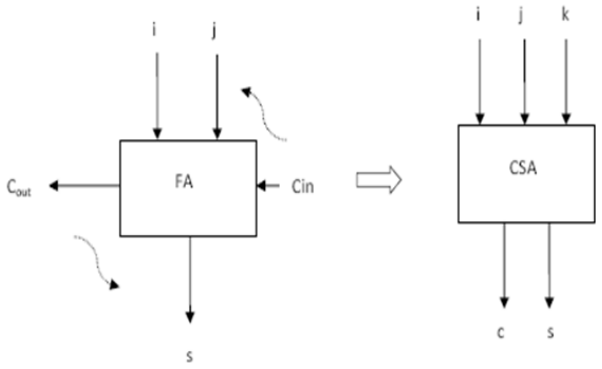

Fig.4. Showing Block Diagram ofCarry Save Adder

5. Designing of multipliers

- *Vedic Multiplication*

Byusing Vedic multiplicationsutrasthe proposed multiplier is designed.These Sutras have been used traditionally for the multiplication of two numbers in the decimal number system. In this work, we are applying the same conceptto make the proposed algorithm compatible with the digital hardware. Vedic multiplication based on some algorithms; some are discussed below:

A. Nikhilam Multiplier

Nikhilam sutra is mainly used when both the operands are of different size. In this paper multiplier with same size operands has been proposed based on Nikhilam sutra.

Let us see multiplication of two decimal numbers (92 * 94) here the base is chosen 100 since it is greatest and also nearest to both two numbers. With simple multiplication of the numbers of the second Column (8*6, = 48) the RHS of the product resulted. By cross subtracting the second number of second Column from the first number of first Column or vice versa.

i.e., 92 - 6 = 86or 94 - 8 = 86 the LHSof the product can be obtained. By concatenating RHS and LHS (Answer = 8928) the final result is obtained.

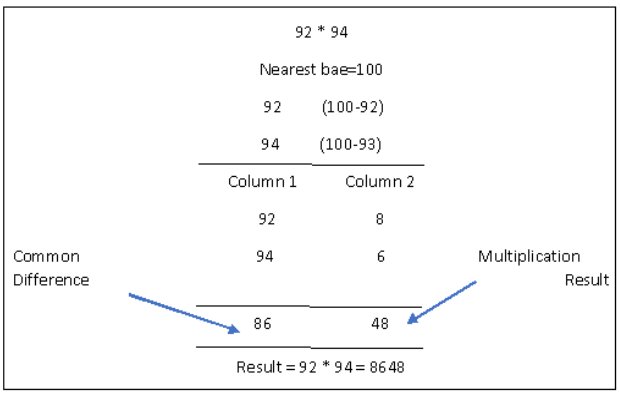

Fig.5. ShowingMultiplication Using Nikhilam Sutra

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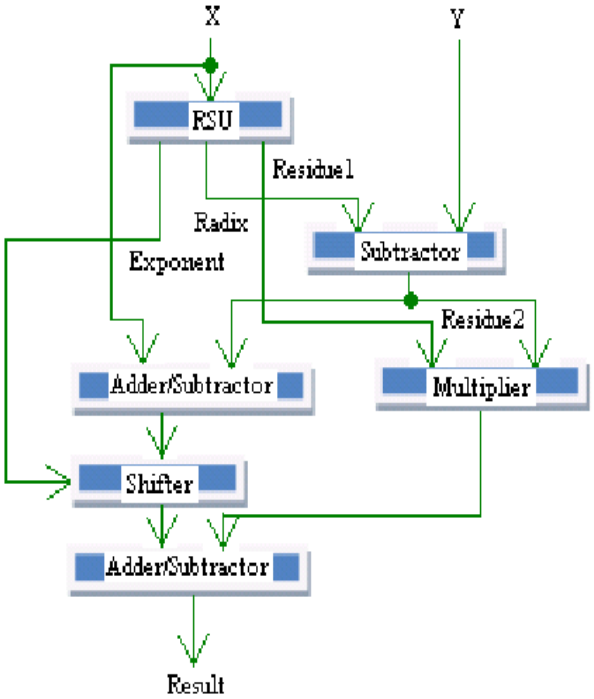
B. Flow Chart



The generalized architecture for Nikhilam multiplier

C. Modules

Example Module Structure:

module <module name>(<module_terminals_list>);

…..

<module internals>

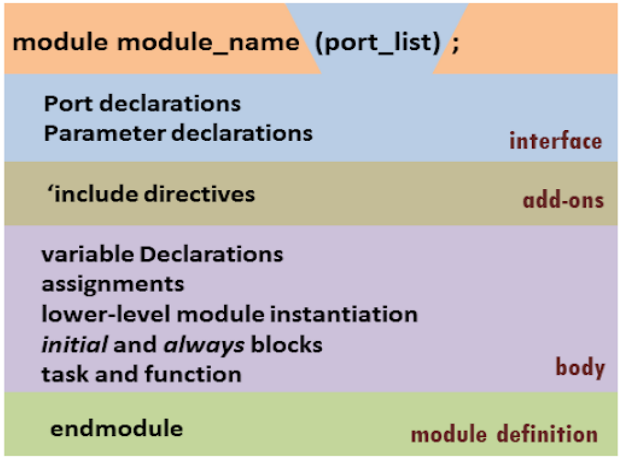
….

….

….

….

endmodule



D. Proposed Design

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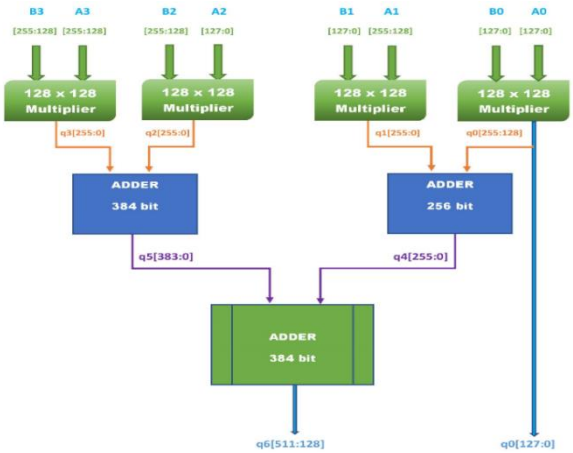

Fig. 6: Showing Block diagram of 256x256 Multiplier

A. Verilog

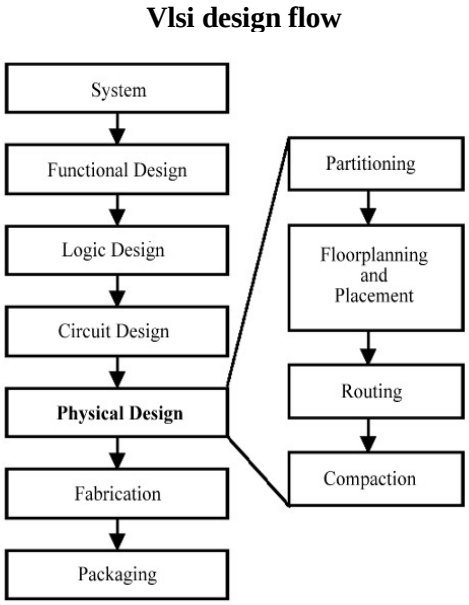

Fig. 7: Showing VLSI Design Flow

6. Results and discussion

The arithmetic operations in real time applications is multiplication and the effective phenomenon of fast multiplier circuit has been an essence of attentiveness decennary. Minimizing the power consumption and delay are very important factors for all the applications,

A. Synthesis Results.

The speed of ALU majorly depends on the multiplier.

The research has established and analyzed that Nikhilam Navatashcaramam Dashatah Sutra is the most effective Sutra, which gives the minimum of delay for multiplication of all the types of short and long numbers. Further, Nikhilam Navatashcaramam Dashatah Sutra multiplication and implementation of the Verilog HDL coding is done using Xilinx Tool.

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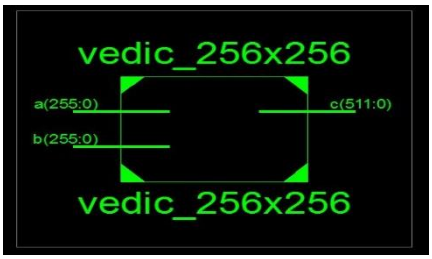

Fig. 8: Showing RTL SCHEMATIC

The designs of 256x256 bits Vedic multiplier have been implemented on Spartan XC3S500-5-FG320 and XC3S1600-5-FG484 device.

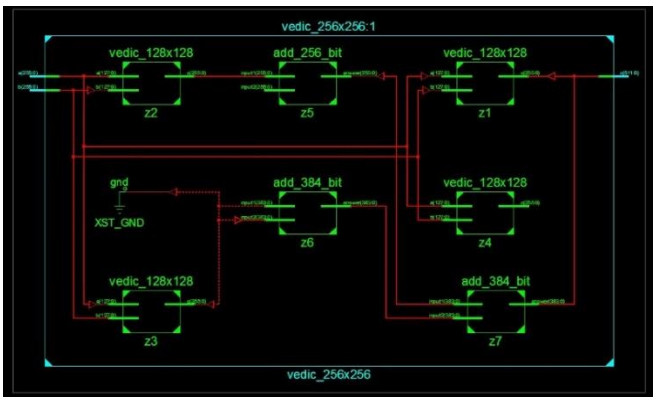

Fig. 9: Showing Detailed RTL SCHEMATIC

The RTL (Register Transfer Logic) can be viewed as black box after synthesize of design is made. It shows the inputs and outputs of the system. By double-clicking on the diagram, we can see detailed schematic like gates, and adders, multipliers and interconnection between them.

B. Use of Simulation software

The developed design for different operations, is simulated and verified their functionality. In order to synthesis, the device named as "XC3S500E" has been chosen and the package is "FG320" with the device speed "-4".

The proposed architecture was developed and is simulated on Modelsim different inputs have been applied and the functionality of the developed code is checked and found to be correct.

TABLE 1: Comparison of Array and Vedic Multiplier (in nano seconds)

MULTIPLIER	**Array Multiplier**	**Vedic Multiplier**
4x4	32.001ns	14.639ns

TABLE 1: Comparison of Vedic Multipliers (in nano seconds)

VEDIC MULTIPLIER	**TIMING DELAY**
2x2	6.376ns
4x4	14.639ns

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8x8	25.536ns
16x16	44.793ns
32x32	82.639ns
64x64	152.653ns
128x128	173.781ns
256x256	266.639ns

C. Timing Delay Summary

```
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
No clock signals found in this design

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 266.639ns
    ----------------------------------------
    Total                    266.639ns (148.106ns logic, 118.534ns route)
                                       (55.5% logic, 44.5% route)

=========================================================================


Total REAL time to Xst completion: 27855.00 secs
Total CPU time to Xst completion: 27855.45 secs
```

D. Device Utilization Summary

Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	59451	4656	1276%
Number of 4 input LUT's	103549	9312	1111%
Number of bonded IOB's	1024	232	441%

7. CONCLUSION

Thus, an efficient Vedic multiplier which has very high speed, less power and with slightly wider area was designed. Using this multiplier module, a Vedic unit was constructed and both these modules were integrated into an arithmetic unit along with the basic adder subtracted.

The designs of 256x256 bits Vedic multiplier have been implemented on Spartan XC3S500-5-FG320 and XC3S1600-5-FG484 device. The computation delay for 16x16 bits Booth multiplier was 80.09 ns and for 16x16 bits Vedic multiplier was 38.815 ns. Hence we can see that the Vedic multipliers are much faster than the conventional multipliers. The algorithms of Vedic mathematics are much more efficient than of conventional mathematics.

Nikhilam, Urdhva Tiryakbhyamand Anurupye sutras are such algorithms by using this we canminimize the power,delayand hardware requirements for multiplication of numbers. The hardware realization using Vedic algorithms are very simple which we can see it in the proposed multiplier.

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