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Closed Loop Current Mode Controlled SEPIC Re-Lift Converter System Using Time Response

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Abstract

The abysmal performance of a classical converter at high conduction duty due to an increase in power loss necessitates the power supply designers to use voltage-lift (VL) techniques. Ripple content present in output of power converter largely affects the performance of load. Hence soft-switched single ended primary inductor converter (SSSEPIC) is proposed between solar system and load to decrease the ripple content. This research work deals with the simulation of SEPIC re-lift converter system (SEPIC-RLCS) in closed loop mode of operation. The ripple content in output voltage is filtered with the help of a T-filter. Besides achieving a good regulated dc output, the prime objective of this work is to obtain an enhancement in dynamic response of SEPIC-RLCS. Simulation studies are performed for dual loop proportional integral (PI), proportional integral derivative (PID), fractional order proportional integral derivative (FOPID), hysteretic controller (HC) and fuzzy controlled (FC) closed loop SEPIC-RLCS by developing Matlab Simulink models. Time domain parameters are compared and comparative results demonstrate the superior performance of fuzzy controlled system. Therefore fuzzy controlled SEPIC-RLCS can be used as a good replacement for the existing dc-dc converters.

Keywords: *Single ended primary inductor converter (SEPIC), Re-lift converter system (RLCS), Dual loop controller, Voltage lifting (VL) techniques, Matlab Simulink.*

1. Introduction

A brute-force approach employed to get steep voltage ratio from conventional boost converters is to simply increase their operating duty. On the contrary, the efficiency of power converter gets lowered because parasitic elements will get excited at high duty cycle operation. Furthermore, the reverse recovery effect introduced at high conduction duty is a key issue that has to be dealt with appropriately in designing power converters. Accordingly, with a trade-off on efficiency it is possible to realize high static gain from a traditional boost converter [1]-[3]. Countless converter structures exist in literature to mitigate the aforesaid shortcomings in a classical boost converter. Boost operation in a converter without resorting to a high duty ratio is possible with the help of coupled magnetic devices, voltage multiplier modules in conjunction with a classical converter, multi-stage converter and as well as by making use of the voltage increasing capability of a transformer [4]-[7]. Voltage operating range of a power converter can also be extended by means of transformer-less structures (i.e. by integrating energy storage elements into the design) [8]. Notwithstanding the fact that these techniques provide an enhanced voltage transfer ratio, the power losses and high input ripple content in a coupled inductor design, substantial increase in cost with the use of multiple power switches, control circuit complexity in multi-stage design and switching surges in transformer holds back the utility of these methods [9],[10]. A thorough review of pros and cons of several voltage boosting

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structures proposed in literature is studied and their appropriate applications are listed in [11]. The power converter literature has witnessed a quantum leap forward in design with the advent of VL design techniques. The idea of using VL method to accomplish high step-up ratio originated from F.L.Luo. For use in electronic design, F.L.Luo has formulated a series of high-efficiency positive/negative dc output converters which can give wide voltage conversion ratio with high power density and a simple control structure [12],[13]. Design of high gain power converters by employing VL technique is discussed and different VL circuit structures have been developed from SEPIC prototype for applications that require high voltage ratio [9]. VL modules are added into a converter that splits inductor on either side of load and a new series of positive output transformer-less circuit arrangements have been devised to get high voltage transfer ratio. The characteristics of VL structures built in laboratory are evaluated in closed loop by using a control strategy that employs variable structure [10]. At high operating frequencies, zero voltage/current turn-on and turn-off methods are invariably used in power converter design to reduce switching stresses and also to improve the power transferring efficiency [2]. Due to high gain flexibility, less ripple content in input and non-inverting output, SEPIC topology is chosen amongst a multitude of power conversion topologies for applications that need high voltage in dc level [14]. H.L.Do has presented a high-efficiency soft-switched novel ripple-free SEPIC converter structure for use in high step-up applications [2].

The converters need to be operated in closed loop so as to achieve faster dynamic response and to get a good regulated dc output. In the design of a closed loop control system, the classical approach is to use PI controller. Conversely, PI controller is not capable of providing regulated output voltage due to input voltage fluctuations and variations in load current. In addition, a high degree of accuracy cannot be expected from PI controller as it is very much sensitive to variations in circuit parameters. The dynamic response of converters employing variable structure control has been extensively investigated in literature [10], [15]. The idea of using fuzzy controller (FC) stems from the fact that it is robust, model-free and can be incorporated into the system with ease. The performance of a fuzzy controlled SEPIC converter to track the maximum power point in a photovoltaic (PV) system is experimentally investigated in [16]. Inspired by results shown in [2], [9], [10], [12] and [16], the aim of this work is to compare the dynamic response of dual loop PI, PID, FOPID, HC and FC SEPIC-RLCS. Simulation results have been comprehensively analyzed in time domain and comparative results demonstrate an improvement in dynamic characteristics of dual loop fuzzy controlled system. To the best of author's knowledge, no attempt has been made in power converter literature to investigate the voltage boosting ability of SEPIC re-lift converter system using dual loop controllers.

The paper is organized as follows: Section 1 gives an introduction in brief about the recent works reported in literature. Section 2 describes the operation of ripple-free SSSEPIC circuit developed by H.L. Do [2]. Section 3 presents the simulation results of various dual loop controlled SEPIC-RLCS. The inferences made from the simulation results are provided in section 4.

2. ZVS Resonant SEPIC Converter [2]
(Adapted from Hyun-Lark Do IEEE Trans. on Power Electronics, vol. 27, no. 6, June 2012)

Several topological variations of SEPIC exist in the literature. Hyun-Lark Do [2] has proposed a ripple free circuit configuration of SEPIC using soft-switching scheme and the converter structure is presented in Figure 1(b). Figure 1(a) shows a simple classical SEPIC converter with a resonant inductor L_r, clamp circuit auxiliary switch S_a along with clamp capacitor. Figure 1(c) represents the equivalent circuit model of SSSEPIC in which L_c is reconfigured as magnetic inductor L_m along with an ideal transformer which has a turns ratio of 1: n. The switches D_a and D_m coupled across auxiliary switch S_a and main switch S_m are utilized for freewheeling purposes. The internal capacitances of switches S_a and S_m which operate

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asymmetrically are represented by C_a and C_m respectively. If capacitors C_1, C_o and C_c are assumed to be fairly large, voltage ripples can be ignored. Smoothing inductor L_1 helps in decreasing ripple content in the input.

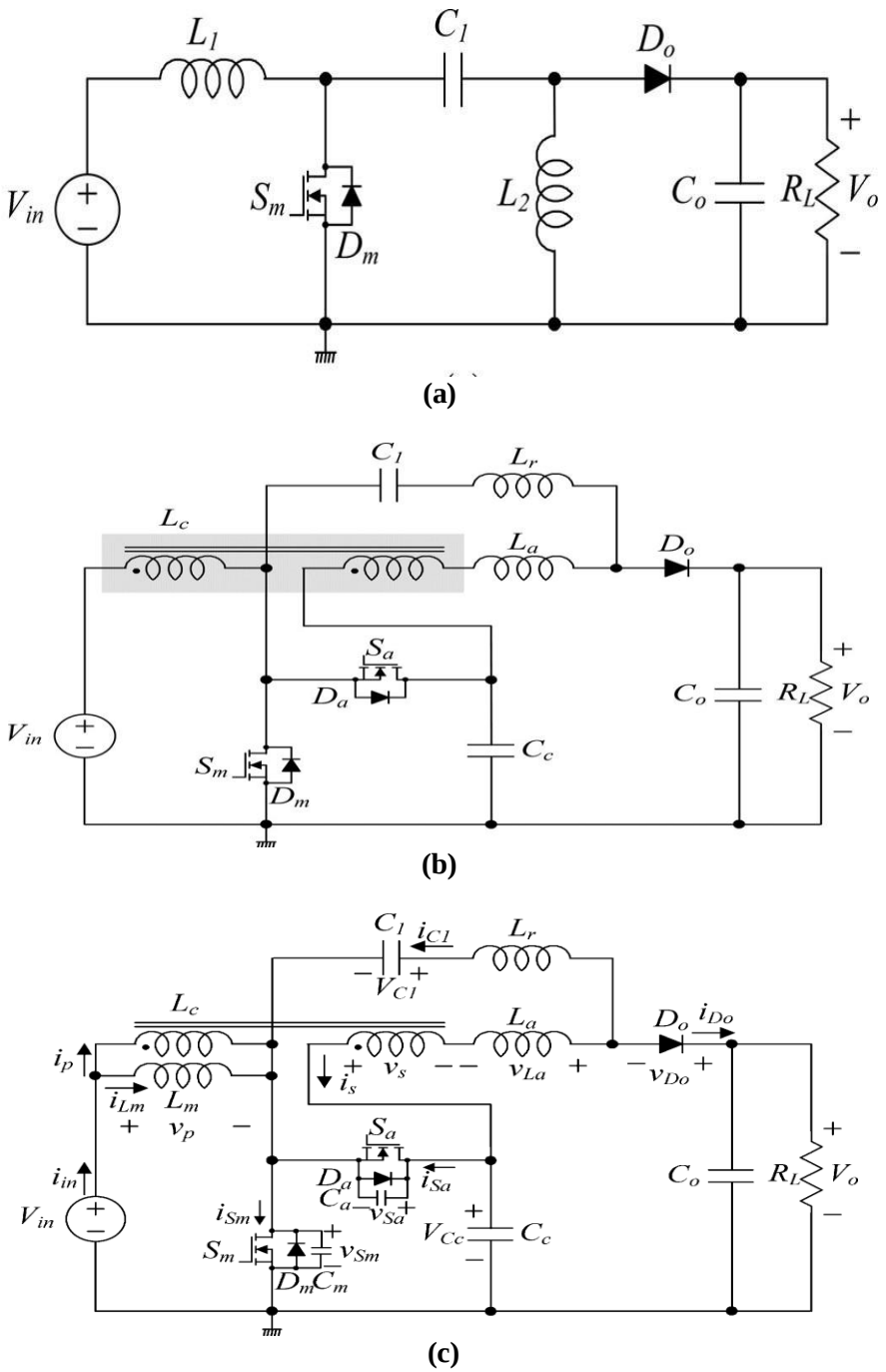

Figure 1. (a) Classical SEPIC (b) SSSEPIC structure (c) Ripple-free equivalent circuit model of SSSEPIC

3. Simulation Results

The present work is intended to compare the voltage enhancing ability of SEPIC-RLCS in dual loop by using traditional and intelligent controllers. The schematic diagram of SEPIC-RLCS in two loop is shown in Figure 2.

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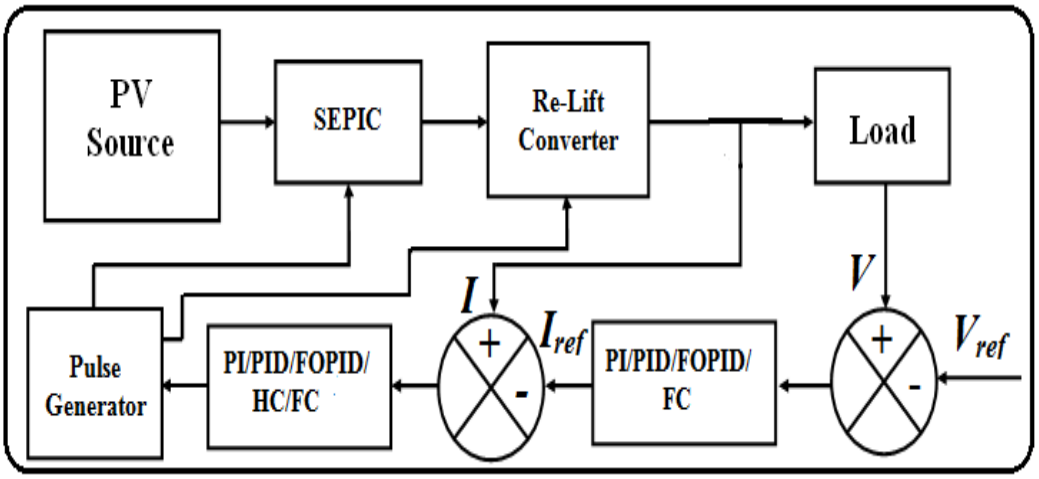

Figure 2. Schematic diagram of SEPIC-RLCS in two loop

3.1. FOPID-HC Controlled Closed Loop SEPIC Converter with Re-lift System

The Matlab simulink model of FOPID-HC-CLSRLCS is given in Figure 3(a). The measurement of power from solar system is shown in Figure 3(b). Voltage across solar module of FOPID-HC controlled CL-SEPIC converter with re-lift system is shown in Figure 3(d) and its value is 18 Volts. The circuit of re-lift converter is shown in Figure 3(c). When switch M_1 is closed, four current loops are established: (i) V_{in} gets coupled to inductor L and charges L to V_{in}. (ii) V_{in} gets coupled through M-D-C_2 thereby charging C_2 to V_{in}. (iii) V_{in} gets coupled through D-L_1-M_1 and charges L_1 to V_{in}, as L, C_2 and L_1 are connected in parallel. (iv) V_{in} gets coupled through D-D_1-C_3-M_1 to ground and therefore C_3 gets charged to V_{in}. If M, M_1 is opened, C_2 and C_3 are connected in series through L_1. The voltage of both capacitors gets added up and thus charging the output capacitor to $2V_c$. The input of SEPIC shown in Figure 3(d) is fed from solar panel which generates 18V. A voltage and current loop is provided in Simulink model presented in Figure 3(a). Voltage loop will ensure that the load voltage is equal to set voltage and the current loop provides protection to converter and load. Load voltage is sensed and it is applied to the voltage comparator. A set voltage of 80V is applied using constant block. The voltage error signal generated is applied to FOPID controller and its output represents the set value of current. The actual current is measured using a current measurement block and it is compared with reference current. The error signal generated from current comparator is applied to HC which use two limits for current (i.e. upper limit I_u and lower limit I_L). The pulse width generator (PWM) generates pulses required by the switch of re-lift converter whenever the sensed current is less than I_L and stops generating, if the current from measurement block is greater than I_u. The output waveforms obtained across R-load of FOPID-HC-CLSRLCS are shown in Figures 3(e), 3(f) and 3(g) respectively. Their values are found to be 80V, 0.65A and 60W. Table 1 provide the values of parameters taken for simulation study.

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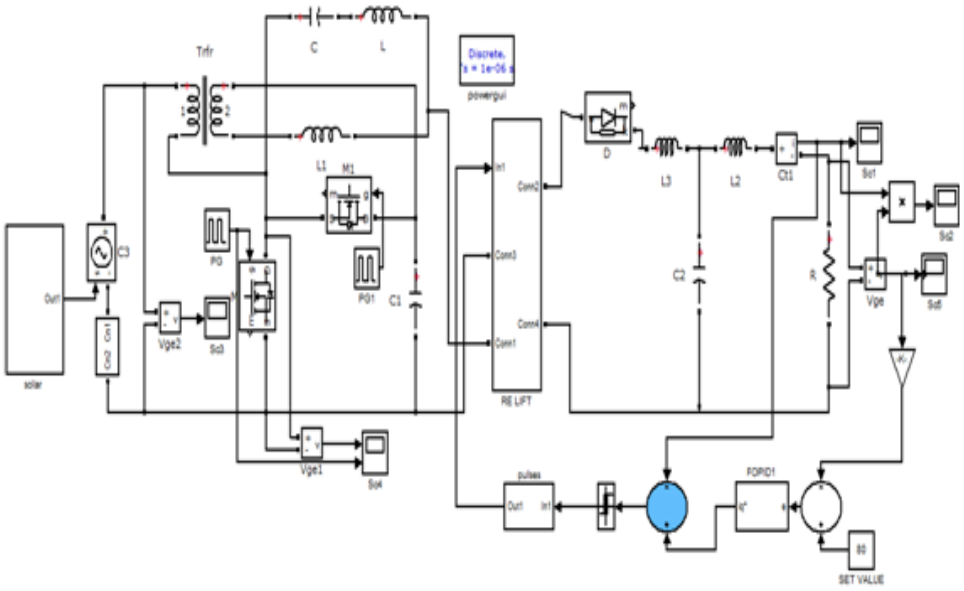

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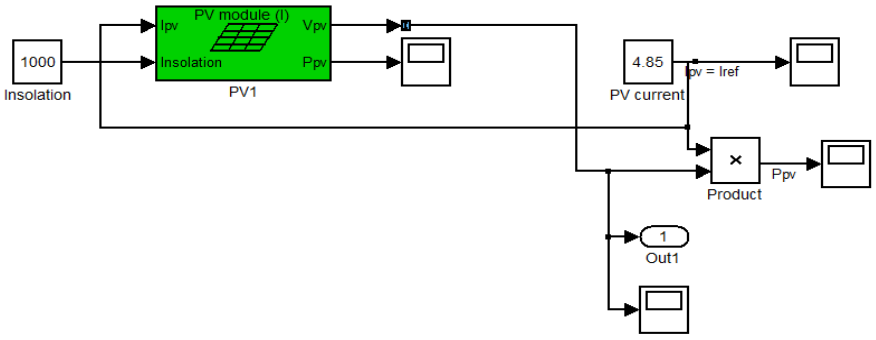

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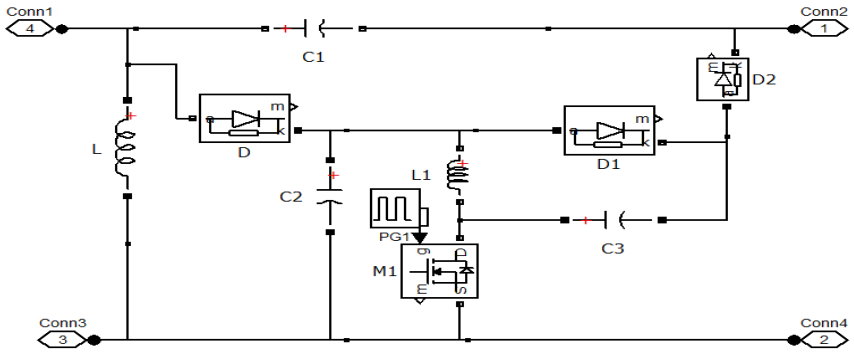

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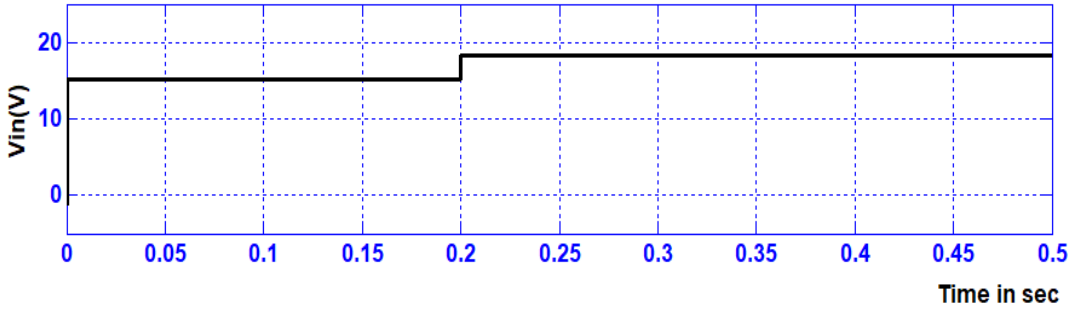

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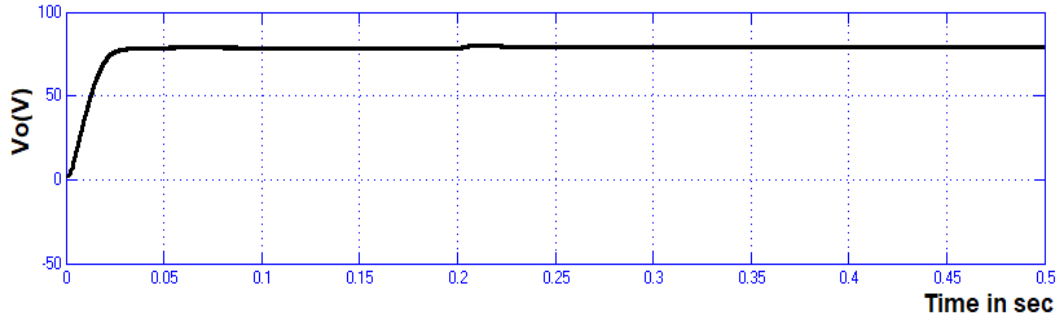

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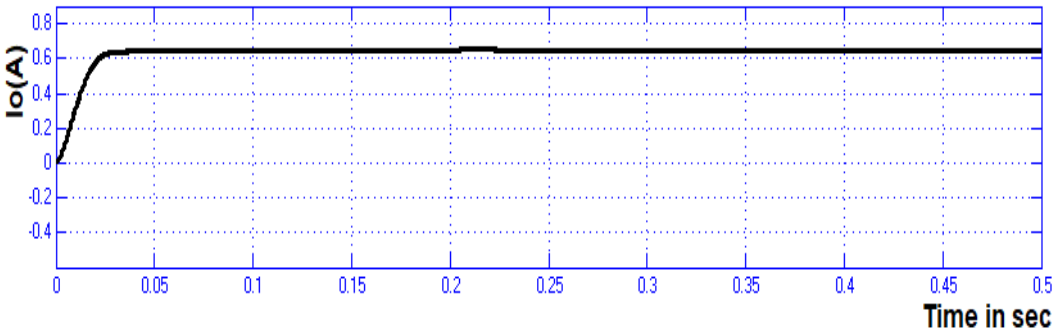

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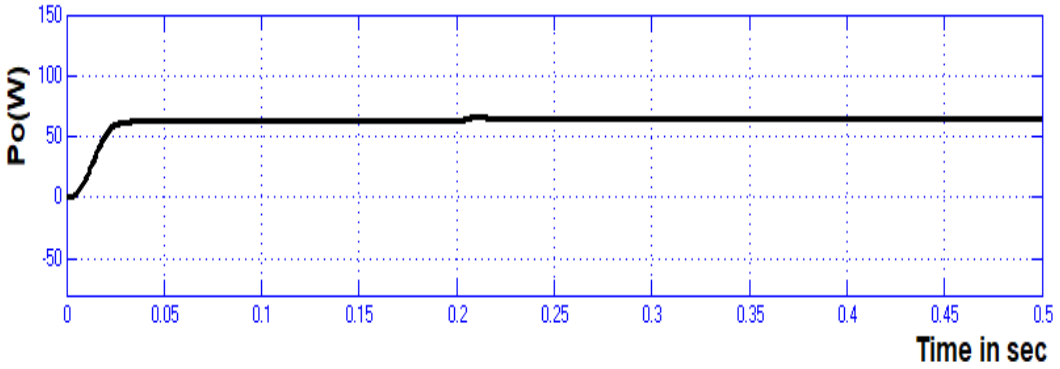

(g)

Figure 3. FOPID-HC-CLSRLCS: (a) Matlab Simulink model (b) power measured from solar source (c) re-lift circuit (d) output voltage from solar source (e) output voltage across R-load (f) output current through R-load (g) output power waveform

Table 1. Parameter Values Taken for Simulation Study

Parameters	Simulation
L_1	35 µH
C_1	6.6 µF
C_2	100 µF
R_L	100 Ohm
V_{in}	15-18 V

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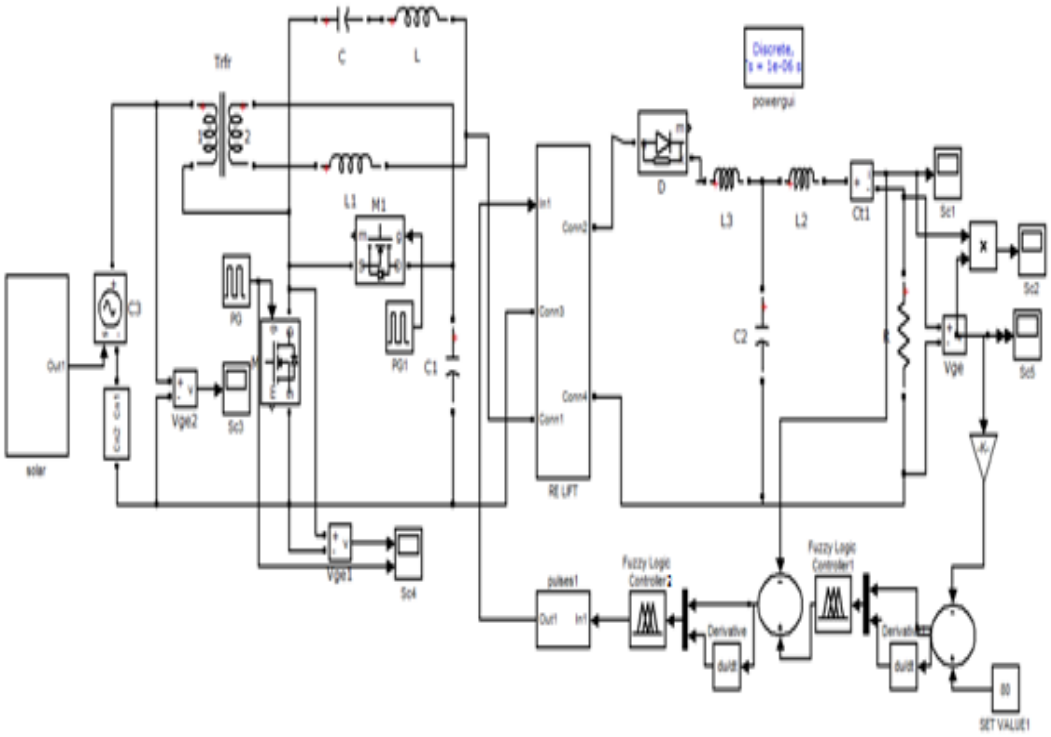
3.2 Closed Coop SEPIC-RLCS Using Fuzzy Controller

The Simulink model of FC-CLSRLCS is given in Figure 4(a). The FOPID-HC controller used in Matlab Simulink model of Figure 3(a) is replaced with fuzzy controller. The input and output variables of FC are shown in Figures 4(b), 4(c) and 4(d). Input voltage of 18V shown in Figure 4(e) is obtained from solar source and it is applied to FC-CLSRLCS. Fuzzy scheme need two inputs that is error and change in error. The change in error is obtained by taking derivative of error. The voltage error is obtained by subtracting actual value from converter with reference value. The output of FC in first loop gives reference current and it is compared with current signal obtained from measurement block. Current error is one of the inputs to FC in second loop and another input is derived by differentiating the current error signal. The output of FC in second loop is applied to generate pulses required by the switch of re-lift converter. The output waveforms appearing across R-load are presented in Figures 4(f), 4(g) and 4(h). Their values are found to be 80V, 0.65A and 76W. Rule base of FC is provided in Table 2.



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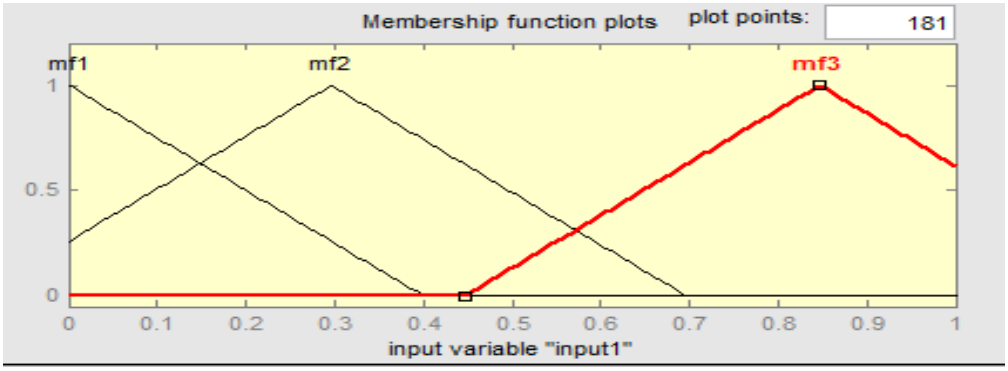

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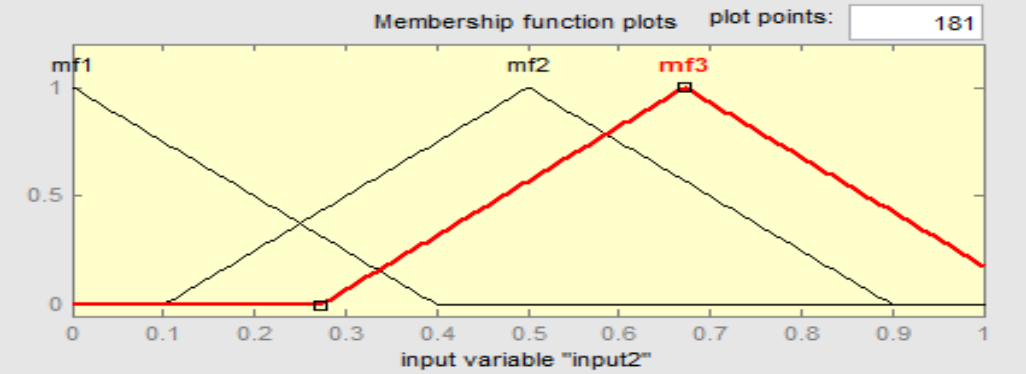

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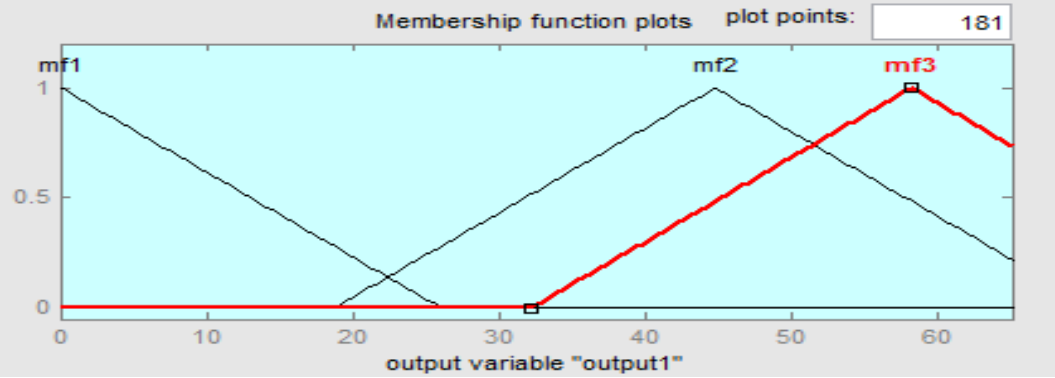

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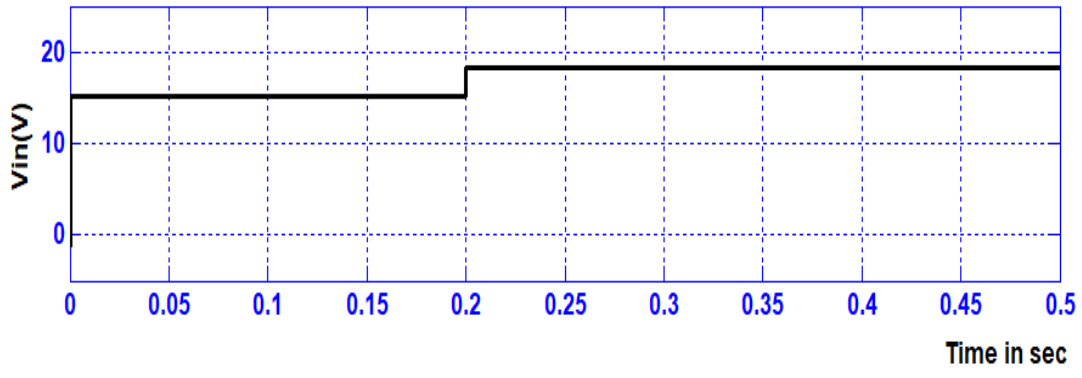

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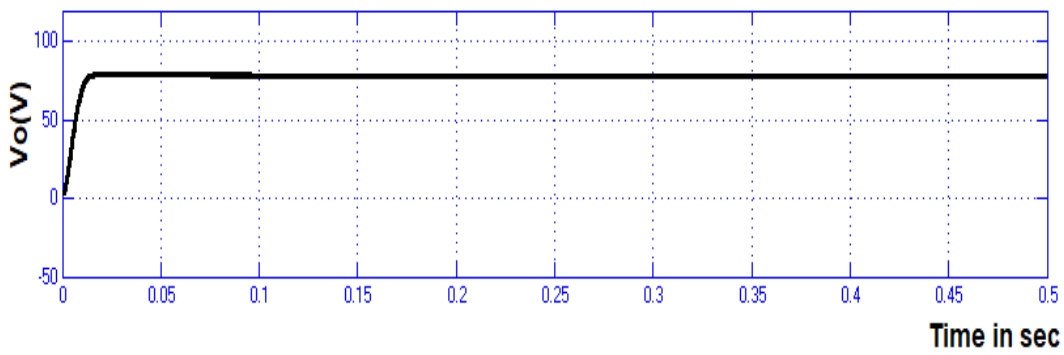

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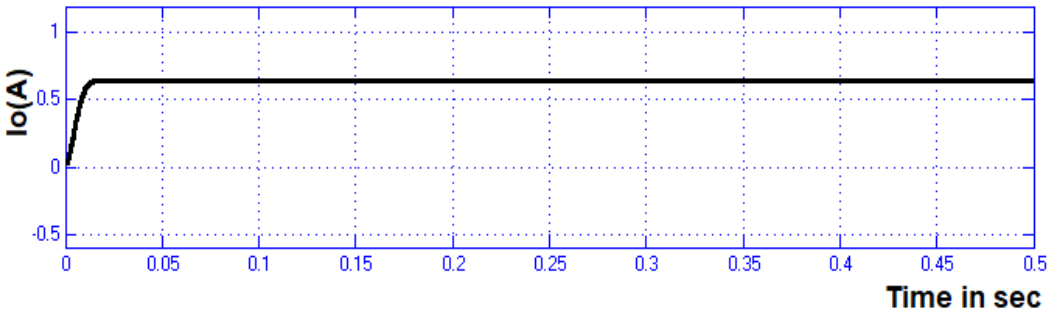

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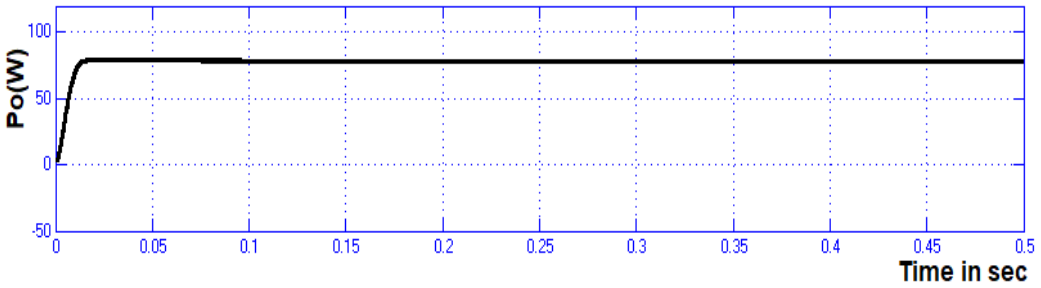

(h)

Figure 4. FC-CLSRLCS: (a) circuit diagram (b) fuzzy input 1 (c) fuzzy input 2 (d) fuzzy output (e) input voltage to SSSEPIC (f) output voltage across R-load (g) output current through R-load (h) output power waveform

Table 2. Rule Base of Fuzzy Scheme

e/Δe	NL	Z	PS
NS	PS	NS	PB
PS	NB	PB	PS
NL	Z	NL	NS
PB	NL	PB	NB

3.3 PI/PID/FOPID Controlled Closed Loop SEPIC Converter with Re-lift System

The Matlab Simulink model of dual loop PI, PID and FOPID controlled SEPIC-RLCS is shown in Figure 5(a). The input of SEPIC shown in Figure 5(b) is fed from solar panel which generates 18V. A dual loop is provided in Simulink model presented in Figure 5(a). Voltage loop will ensure that the load voltage is equal to set voltage and the current loop provides protection to converter and load. Load voltage is sensed and it is applied to the voltage comparator. A set voltage of 80V is applied using constant block. Voltage error signal generated is applied to PI/PID/FOPID controller and its output represents the set value of current. Actual current is measured using a current measurement block and it is compared with reference current. The error between actual and reference value is applied to PI/PID/FOPID controller. The output of current loop in PI/PID/FOPID is one of the inputs to PWM generator and other input is saw tooth carrier wave. The output pulses from PWM generator are applied to re-lift circuit so that output voltage

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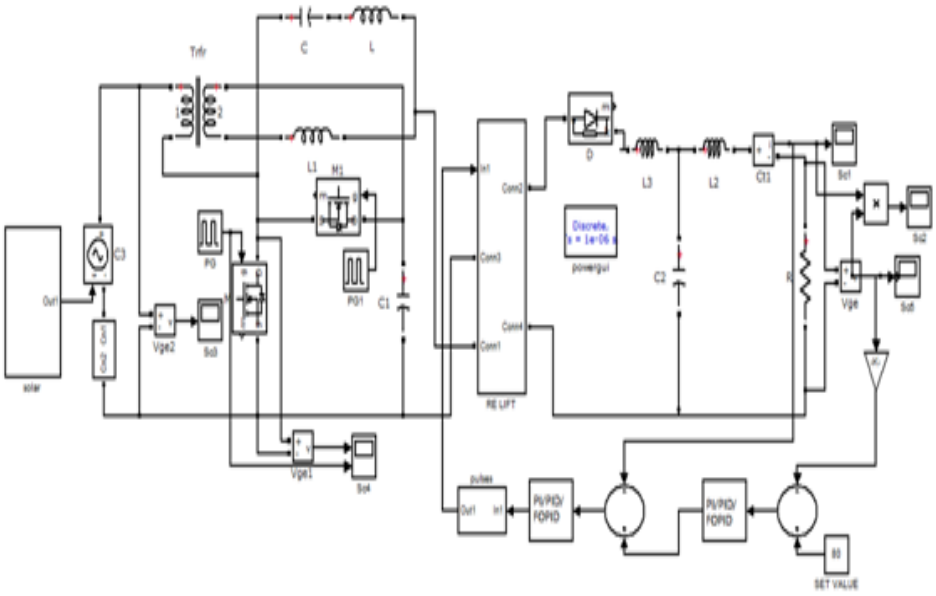
can be reduced to a nominal value. The output waveforms of dual mode PI controller are shown in Figures 5(c), 5(d) and 5(e). Simulation results of two loop PID and FOPID controllers are presented in Figures 6(a), 6(b) and 6(c) and Figures 7(a), 7(b) and 7(c) respectively. The time domain parameters values of various dual loop controlled SEPIC re-lift converters are tabulated in Table 3 and Table 4. The voltage and current controller bar charts are shown in Figures 7(d) and 7(e). It is clearly evident from Table 4 and 4 that the time domain response is very much improved with the use of fuzzy controller.



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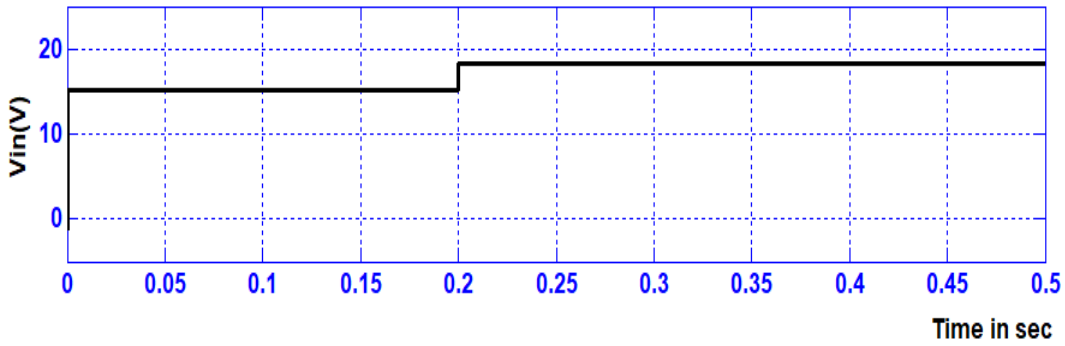

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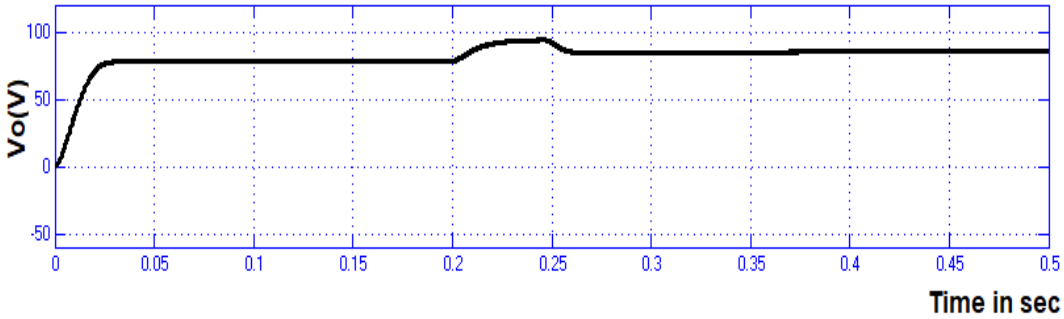

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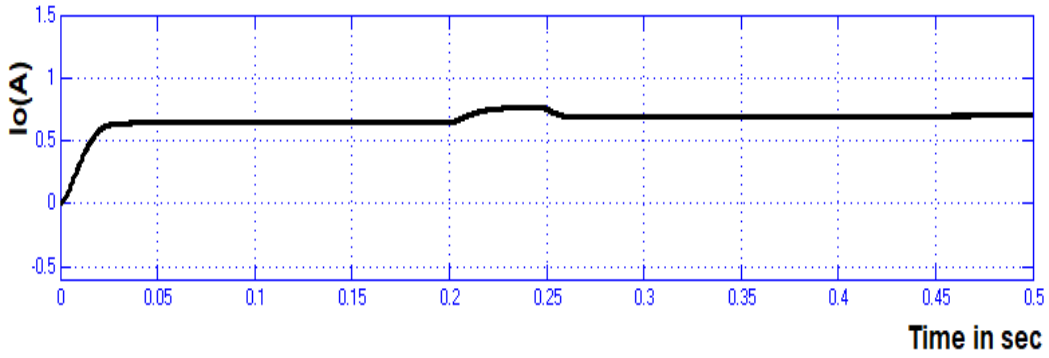

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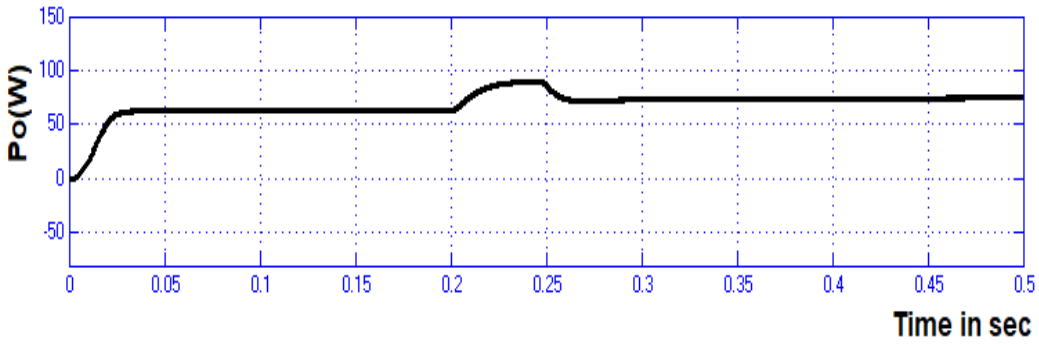
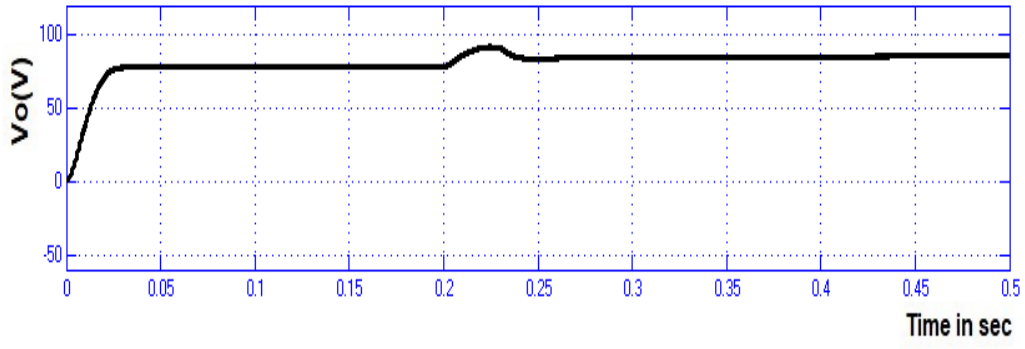


(e)

Figure 5. PI-CLSRLCS: (a) Matlab Simulink model (b) output voltage from solar source (c) output voltage across R-load (d) output current through R-load (e) output power waveform



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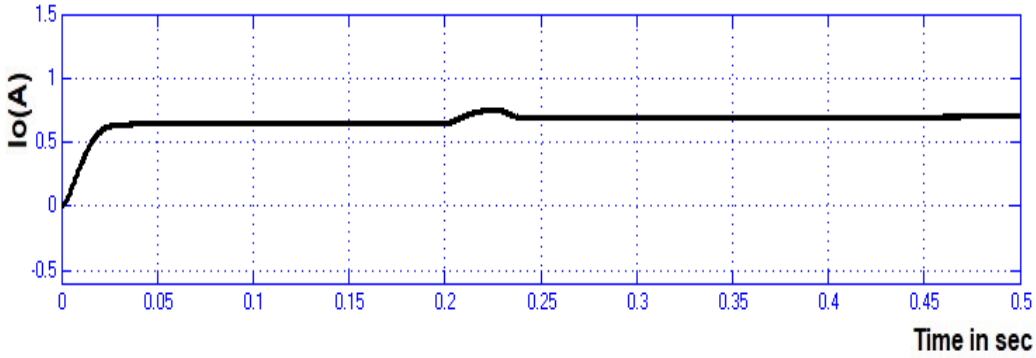

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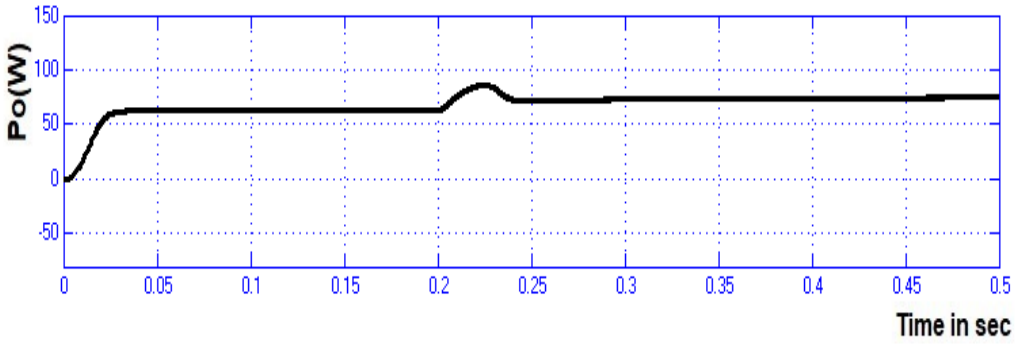
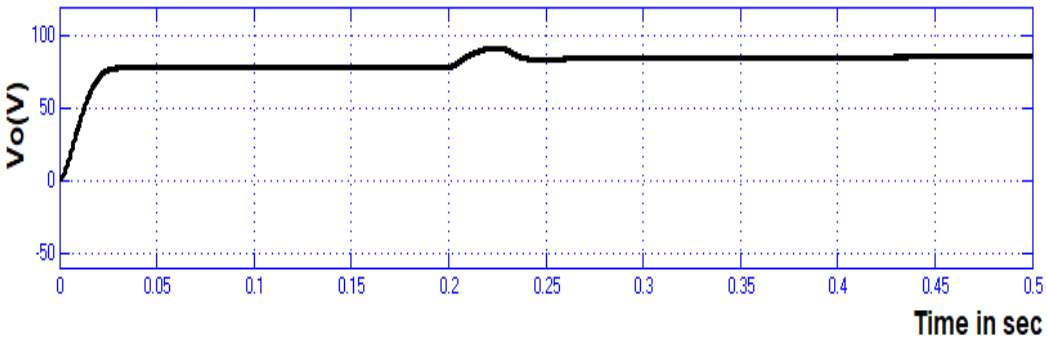


(c)

Figure 6. PID-CLSRLCS: (a) output voltage across R-load (b) output current through R-load (c) output power waveform



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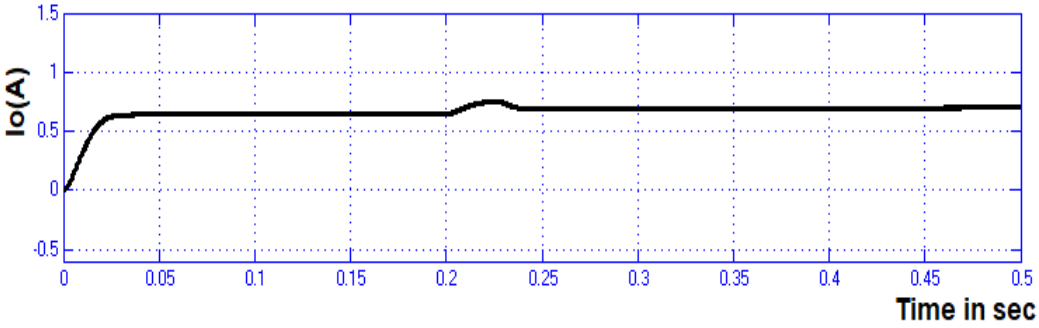

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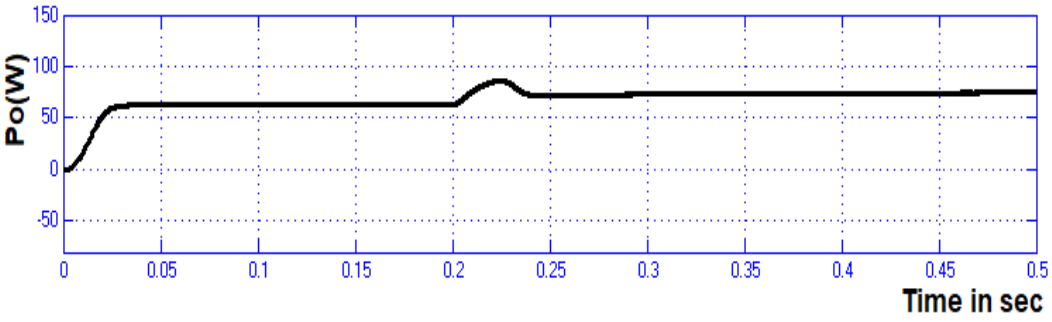

(c)

Figure 7. FOPID-CLSRLCS: (a) output voltage across R-load (b) output current through R-load (c) output power waveform (d) voltage bar chart and (e) current bar chart

Table 3. Comparison of Time Domain Parameters (Voltage Controller)

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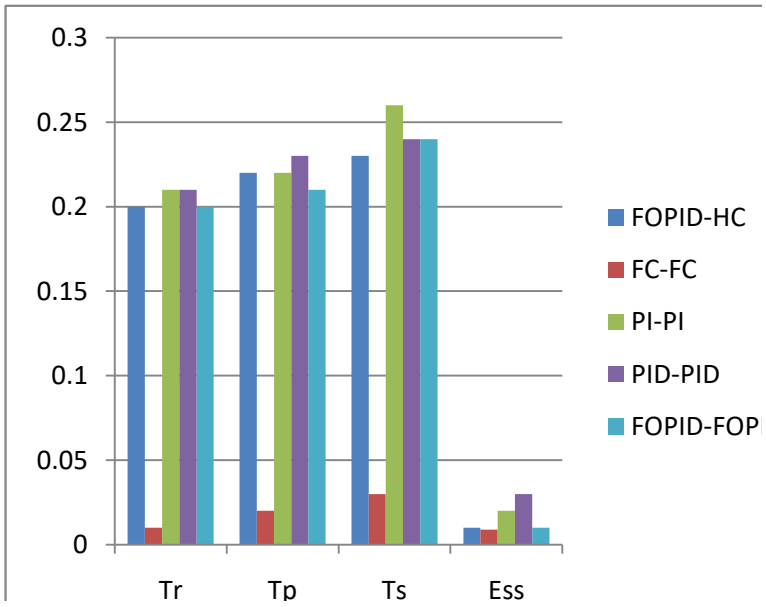
Controller	T_r(Sec)	T_p(Sec)	T_s(Sec)	E_{ss}(Volts)
FOPID-HC	0.20	0.22	0.23	0.01
FC-FC	0.01	0.02	0.03	0.009
PI-PI	0.21	0.22	0.26	0.02
PID-PID	0.21	0.23	0.24	0.03
FOPID-FOPID	0.20	0.21	0.24	0.01



(d)

Table 4. Comparison of Time Domain Parameters (Current Controller)

Controller	T_r(Sec)	T_p(Sec)	T_s(Sec)	E_{ss}(Volts)
FOPID-HC	0.21	0.22	0.24	0.007
FC-FC	0.012	0.023	0.031	0.004
PI-PI	0.23	0.22	0.27	0.009
PID-PID	0.21	0.23	0.247	0.006
FOPID-FOPID	0.20	0.21	0.26	0.008

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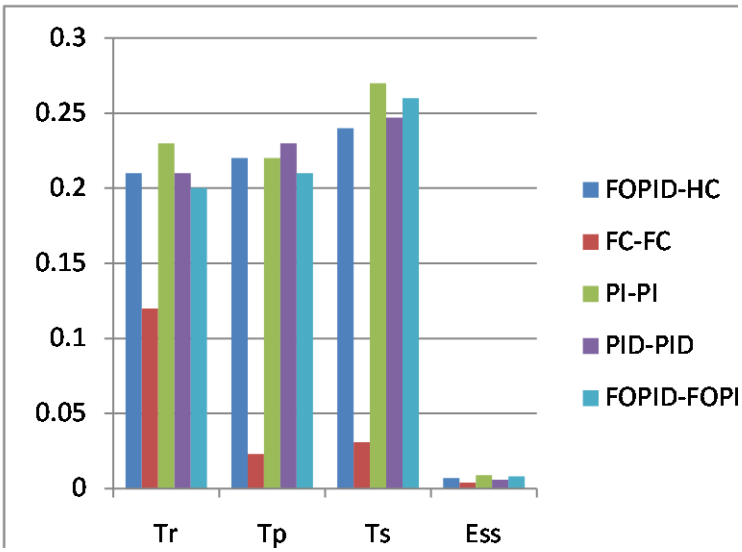

(e)

4. Conclusion

The performance of soft-switched SEPIC re-lift converter employing PI, PID, FOPID, FOPID-HC and fuzzy controller are analyzed in dual loop mode of operation by developing Matlab Simulink models. Soft switching operation is achieved by adding an auxiliary switch with clamped capacitor into SEPIC converter. Time domain analysis is carried out comprehensively and comparative results show an enhancement in time domain parameters of FC system. Results reveal that combination of SEPIC with FC-CLSRLCS has less rise time and error at steady-state and hence it can be used as a substitute for the existing dc-dc converters.

References

[1] Yiyang Li and Swamidoss Sathiakumar, "Improved quadratic boost converter based on the voltage lift technique," 2017 Asia Modelling Symposium, pp. 139–44, **(2017)**. DOI 10.1109/AMS.2017.30

[2] Hyun-Lark Do, "Soft-switching SEPIC converter with ripple-free input current," IEEE Trans. Power Electron., vol. 27, no. 6, pp. 2879–87, June **(2012)**.

[3] Ki-Bum Park, Gun-Woo Moon and Myung-Joong Youn, "Nonisolated high step-up boost converter integrated with sepic converter," IEEE Trans. Power Electron., vol. 25, no. 9, pp. 2266–75, Sep. **(2010)**.

[4] S.-K. Changchien, T.-J. Liang, J.-F. Chen and L.-S.Yang, "Step-up dc-dc converter by coupled inductor and voltage-lift technique", IET Power Electron., vol. 3, iss. 3, pp. 369–78, May **(2010)**.

[5] Giulia Di Capua and Nicola Femia, "A critical investigation of coupled inductors SEPIC design issues," IEEE Trans. Power Electron., vol. 61, no. 6, pp. 2724–34, June **(2014)**.

[6] Marcos Prudente, Luciano L.Pfitscher, Gustav Emmendoerfer, Eduardo F.Romaneli and Roger Gules, "Voltage multiplier cells applied to non- isolated DC–DC converters," IEEE Trans. Power Electron., vol. 23, no. 2, pp. 871–87, Mar. **(2008)**.

[7] Sanghyuk Lee, Pyosoo Kim and Sewan Choi, "High step-up soft-switched converters using voltage multiplier cells", IEEE Trans. Power Electron., vol. 28, no. 7, pp. 3379–87, July **(2013)**.

ISSN: 2233-7857 IJFGCN

[8] Yi-Ping Hsieh, Jiann-Fuh Chen, Tsorng-Juu Liang and Lung-Sheng Yang, "Novel high step-up DC-DC converter with coupled-inductor and switched-capacitor techniques," IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 998–1007, Feb. **(2012)**.

[9] M. Zhu and F. L. Luo, "Series SEPIC implementing voltage-lift technique for DC–DC power conversion," IET Power Electron., vol. 1, no. 1, pp. 109–21, April **(2008)**.

[10] Y. Jiao, F.L. Luo and B.K. Bose, "Voltage-lift split-inductor-type boost converters," IET Power Electron., vol. 4, iss. 4, pp. 353–62, April **(2011)**.

[11] Mojtaba Forouzesh, Yam P. Siwakoti, Saman A. Gorji, Frede Blaabjerg and Brad Lehman, "Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications," IEEE Trans. Power Electron., vol. 32, no. 12, pp. 9143-78, Dec. **(2017)**.

[12] F.L.Luo, "Re-lift converter: design, test, simulation and stability analysis," IET Proc.-Electr. Power Appln., vol. 145, no. 4, pp. 315–24, July **(1998)**.

[13] Miao Zhu, Tao Wang and Fang Lin Luo, "Analysis of voltage-lift-type boost converters," 7th IEEE Conf. on Ind. Electr. and Appln. (ICIEA), pp. 214–19, July **(2012)**.

[14] Mustafa A.Al- Saffar, Esam H. Ismail, Ahmad J. Sabzali and Abbas A. Fardoun, "An improved topology of SEPIC converter with reduced output voltage ripple," IEEE Trans. Power Electron., vol. 23, no. 3, pp. 2377–86, Sep. **(2008)**.

[15] Y.Jiao, F.L. Luo and M. Zhu, "Generalised modeling and sliding mode control for n-cell cascade super-lift DC-DC converters," IET Power Electron., vol. 4, iss. 5, pp. 532–40, May **(2011)**.

[16] Ahmad El Khateb, Nasrudin Abd Rahim, Jeyraj Selvaraj and Mohammad Nasir Uddin, "Fuzzy logic controller based SEPIC converter for maximum power point tracking," IEEE Trans. Ind. Appl., vol. 50, iss. 4, pp. 2349–58, Feb. **(2014)**.

ISSN: 2233-7857 IJFGCN