International Journal of Future Generation Communication and Networking
Vol. 13, No. 3, (2020), pp. 3982–3989

FPGA implementation of low power 16x16 bit Vedic Multiplier

S. Ravi [*1], P. Murugapandian [2], T. Lavanya Devi [3], D. Venkata Anil [4], B. Ravi Teja [5], P. Maneesha [6]

[*1]*Associate Professor, Department of ECE, Gudlavalleru Engineering College, Krishna District, Andhrapradesh.*

[2]*Associate Professor, Department of ECE, Anil Neerukonda Institute of Technology & Sciences, Visakhapatnam, Andhrapradesh.*

[3, 4, 5, 6] *Final year B.Tech, Department of ECE, Gudlavalleru Engineering College, Krishna District, Andhrapradesh.*

E-mail: ravi.vlsi29@gmail.com

Abstract

This paper proposes a vedic multiplier based on Urdhwa Tiryagbhyam sutra. This sutra can be used to perform multiplication on large size input in a very fast manner. The implementation follows hierarchical approach, that is the design process starts with 2x2 multiplier design, then it is used in the implementation of 4x4 multiplier. The same thing continues for 8x8 and 16x16 multipliers design. As a part of the implementation in FPGA process, synthesis report of the proposed system is obtained and the hardware utilization details are presented.

Keywords: *Array multiplier, FPGA, low power multiplier, Urdhva Tiryagbhyam sutra, Vedic multiplier.*

1. Introduction

Multiplication operation is one of the performance deciding operations in DSP processors, Image processsors, and general purpose processors [1]. It requires more hardware in terms of number of adders [2]. Particularly in signal processing operations such as Multiply and Accumulate (MAC), Discrete Fourier Transform (DFT), convolution, filter implementation, and Fast Fourier Transform [3], multiplication operation plays a key role. In general purpose processor, high speed multiplier is used for performing multiplication. Vedic multiplication follows array multiplier structure with improvement in speed. Vedic Mathematics is an ancient approach of doing calculations in a fast manner using mind calculations. These techniques are now applied in processor design so that it performs the operations efficiently as well as using less hardware. Vedic mathematics has totally 16 sutras. It can be done with mind calculations without using pen [4]. Urdhva Tiryakbhyam is a kind of sutra for multiplication and it can also be used for division of large numbers [5].

This paper proposes a simple 16 x 16 bit binary multiplier using Urdhwa Tiryakbhyam (Vertically and Crosswise) Sutra, which is one of the efficient sutra of the Vedic Mathematics, especially used for multiplication. Considering two binary numbers (each of size 16-bits), and applied to Vedic multiplier produces 32 bit result. The same sutra can be extended for binary numbers of any size. Verilog HDL coding is used and the proposed architecture is implemented on FPGA from Xilinx Inc.

ISSN: 2233-7857 IJFGCN

2. Related work

A 4 x 4 multiplier using one of the most popular Vedic multiplication technique called Urdhwa Tiryakbhyam (Vertically and crosswise) method is presented in [5]. This approach has the advantage of less increase in delay when the size of the operands increases. An 8 x 8 Vedic Multiplier using the same technique and making use of 4 x 4 multiplier is presented in [7]. This approach uses ripple carry adder way of combining two 4 bit multiplication results to obtain 8 bit multiplier results. The delay of this 8 – bit Vedic multiplier is low when compared to the Array, and Wallace tree multipliers. Another 8 x 8 bit BCD multiplier using Vinculum method is described in [8]. It claims that the execution time for multiplication less compared to normal BCD multiplier. A low hardware area focused Vedic multiplier using carry select adder at the adder stage of partial products addition is illustrated in [9]. It also provides the speed advantage due to the selection of carry instead of ripple action to propagate the carry through the full adder stages. A review on Various Vedic multipliers is described in [10]. This paper describes various low power and high speed multipliers based on Vedic mathematics.

This proposed work is to implement 16x16 Vedic multiplier using Urdhwa Tiryakbhyam method and it is implemented in FPGA from Xilinx Inc. Verilog HDL is used as a modeling language to describe to the Xilinx ISE software.

3. Urdhwa Tiryagbhyam method

Urdhva Tiryakbhyam Sutra is a fast and efficient sutra for carrying out multiplication, among the 16 sutras (or techniques) in the Vedic Mathematics. This Urdhwa Tiryakbhyam means "Vertically and Crosswise", which is the method of multiplication [11]. Typical example which illustrate the procedure to perform multiplication of two decimal numbers (523 x 837) using this method is given in Figure 1. Followed by this a line diagram that illustrates how the same multiplication is performed on binary numbers is given in Figure 2.

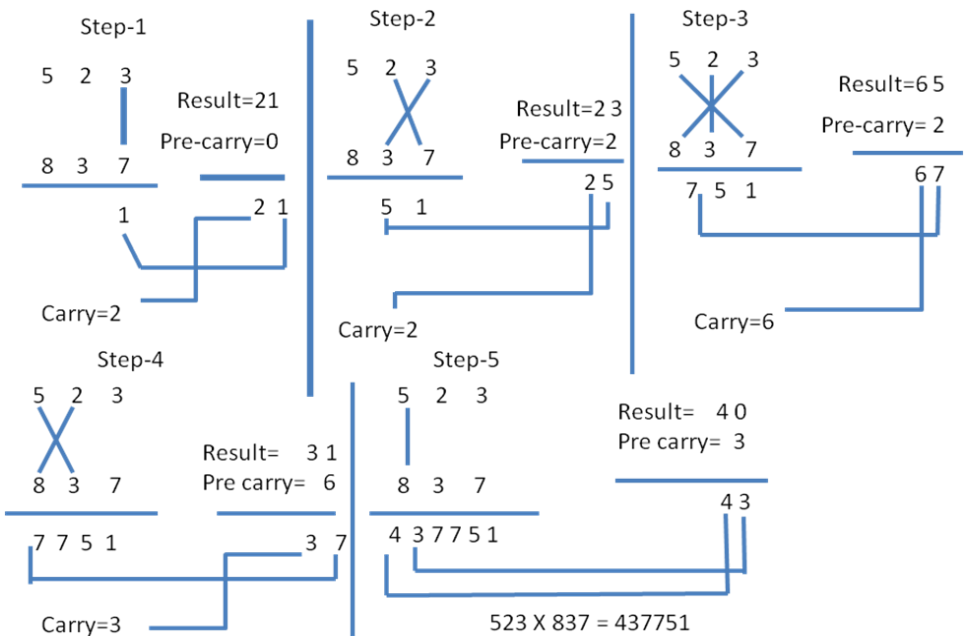

Figure 1. Illustration of Multiplication of two decimal numbers

ISSN: 2233-7857 IJFGCN

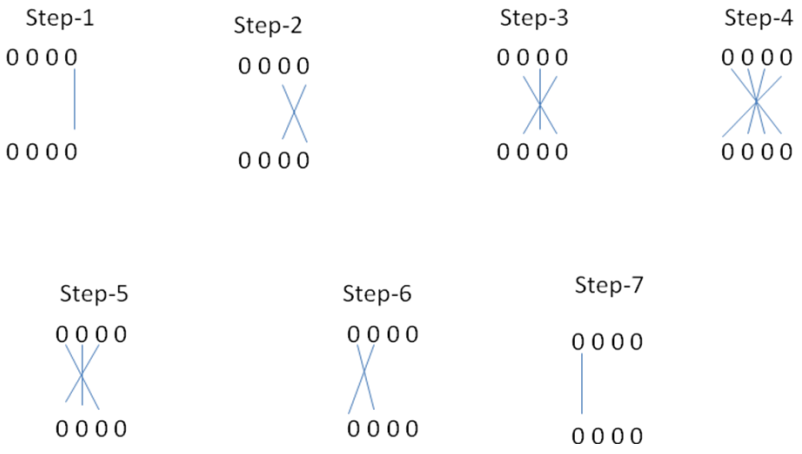

Figure 2. A 4x 4 binary Multiplication process Line diagram

The proposed 16 x 16 bit Vedic multiplier design commences from a 2×2 bit multiplier, which is the basic block using which all the higher level multipliers are implemented. The proposed system uses hierarchical approach that means once we complete 2 x 2 bit multiplier design we use that as a module in building 4 x 4 bit multiplier. The basic structure of a 2 x 2 bit multiplier is shown in Figure 3. When we design the 4 x 4 bit multiplier, there are options to use different adder structures in the addition of partial products. To name some of the most commonly used adder techniques, carry look ahead (CLA) adder, ripple carry adder (RCA), Carry select Adder, or carry save adder (CSA), etc. The block diagram of 4 x 4 bit multiplier using RCA adder is presented in Figure 4.

The above procedure is repeated for implementing 8x 8 bit multiplier using 4 x 4 bit multipliers and then implementing 16 x 16 bit multiplier from its lower level hierarchical counterpart called 8 x 8 bit multipliers. The implementation details of 8 x 8 bit and 16 x 16 bit multipliers are shown in Figure 5 and Figure 6, respectively.

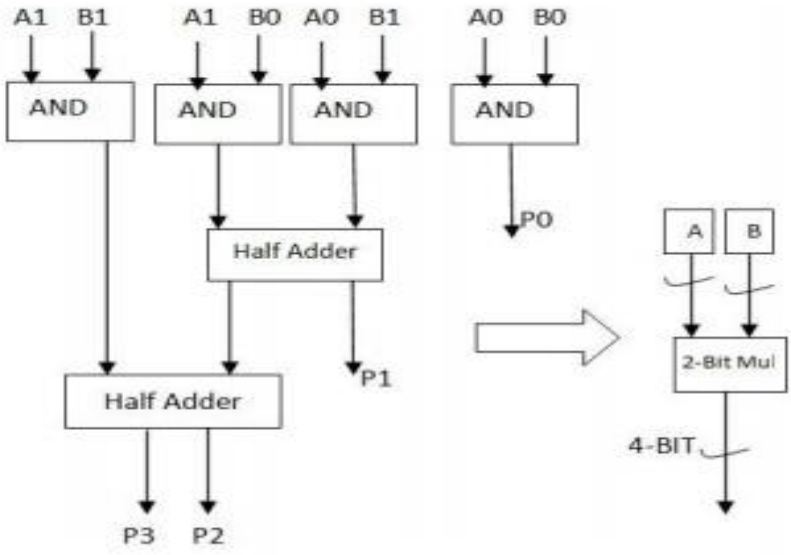

Figure 3. A 2x2 Multiplier using Urdhwa Tiryakbhyam Sutra & its symbol

ISSN: 2233-7857 IJFGCN

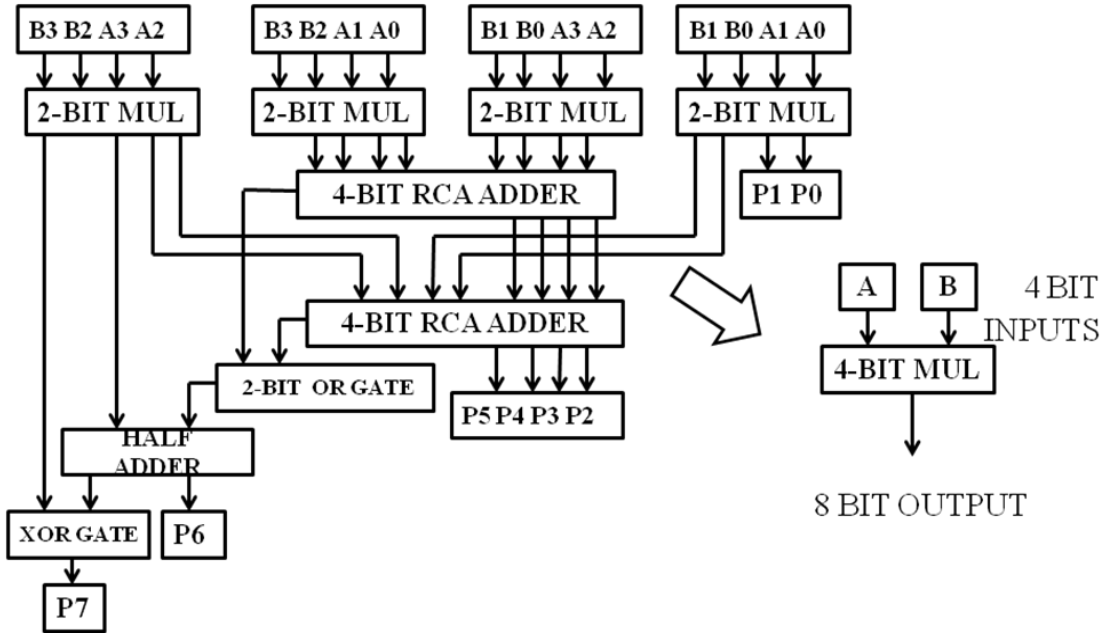

Figure 4. 4 x 4 multiplier using Urdhwa Tiryakbhyam Sutra and its symbol

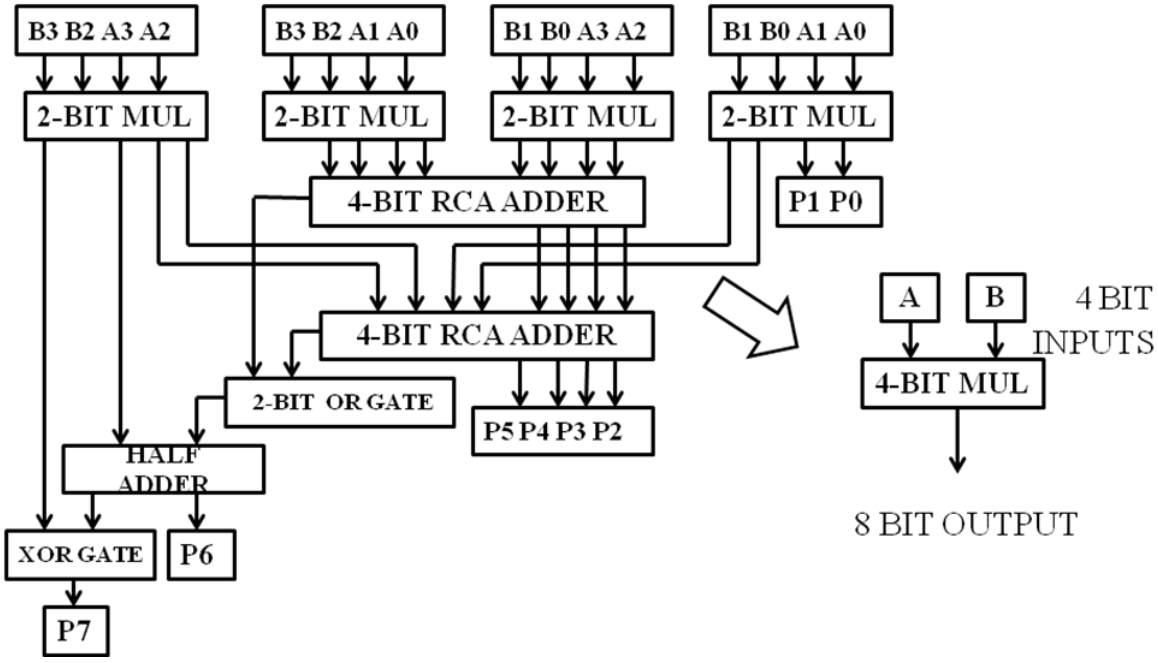

Figure 5. An 8-bit Multiplier using Urdhwa Tiryakbhyam Sutra and its symbol

ISSN: 2233-7857 IJFGCN

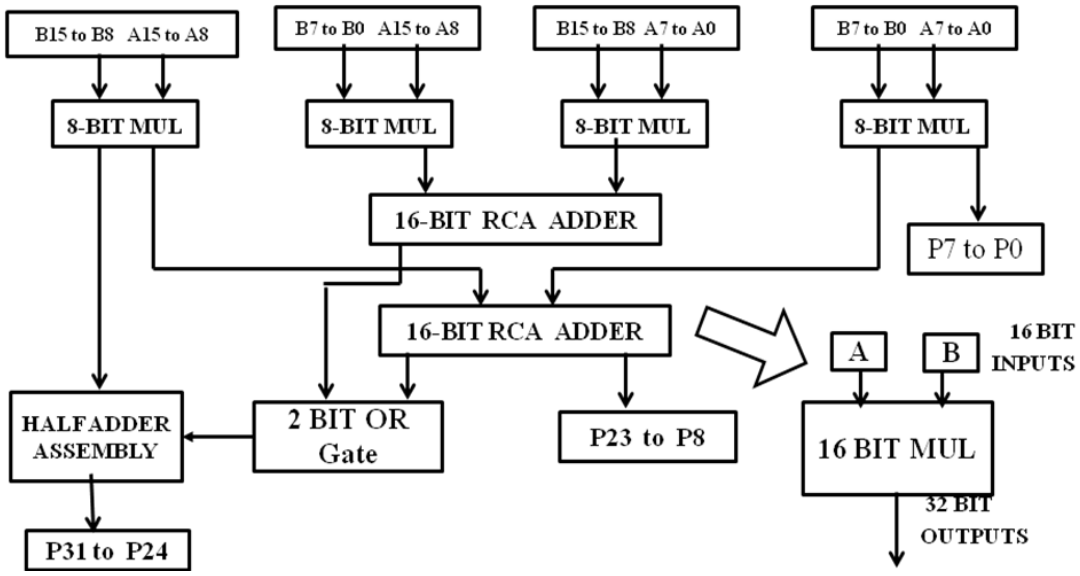

Figure 6. 16-bit multiplier using Urdhwa Tiryakbhyam sutra and its symbol

4. Results and Discussion

Figure 7. shows the RTL view of 16x16 bit Vedic multiplier using Ripple carry adder, which is implemented in Xilinx ISE 14.2i. Logic synthesis to obtain the hardware utilization details, and simulation to verify its functional behavior are done using Xilinx ISE 14.2i. The target device family selected for Synthesis is Spartan 3E and the device used is XC3S500e-5pq208. The HDL used for describing the hardware to the Xilinx ISE tool is that Verilog HDL. Figure 8 shows the internal view of the same.

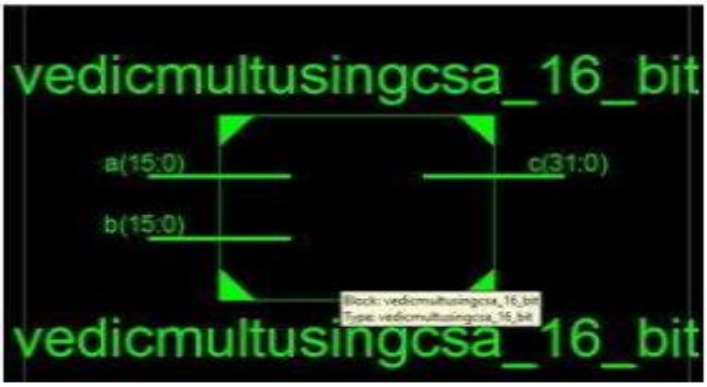

Figure 7. RTL view for Vedic Multiplier using Ripple carry Adder

ISSN: 2233-7857 IJFGCN

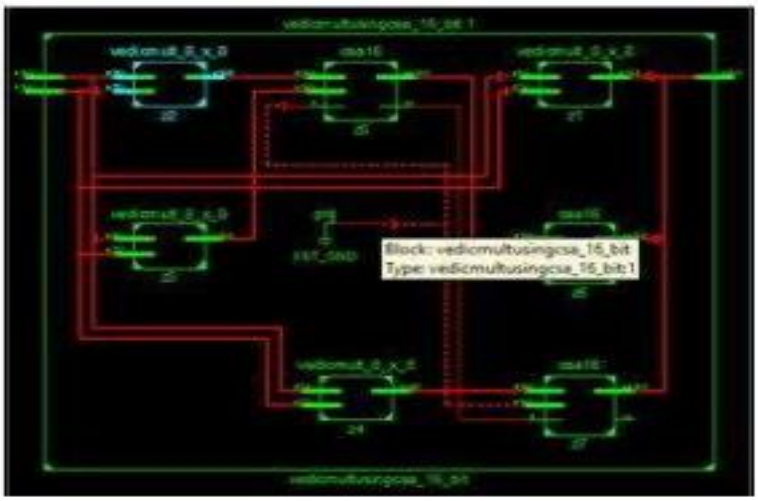

Figure 8. Internal View for Vedic Multiplier using Ripple carry Adder

The device utilization summary of the proposed 16x16 bit multiplier using xc3s500e-5pq208 is given in Table 1. Also the delay estimated for the Vedic multiplier considering the logic and interconnect routing is given in Table 2.

Table 1. Device utilization summary

	Used	Total	Used percentage
Number of slices	409	4656	8 %
Number of 4 input LUTs	716	9312	7 %
Number of bonded IOBs	64	158	40 %

Table 2. Delay summary of the proposed method

	Delay in ns
Logic Delay	21.077
Route delay	13.97
Total delay	35.07

A 16x16 bit Vedic Multiplier is implemented using Verilog HDL and simulated on Xilinx ISE 14.2i. The simulation results are shown in Figure 9. Taking two 16 bit numbers as input, the product of two numbers is generated as output by the circuit.

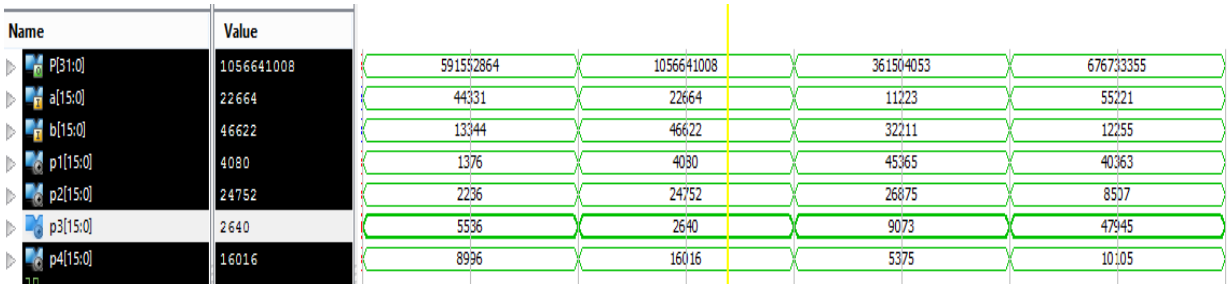

Figure 9. Simulation result for 16 x 16 Vedic Multiplier

ISSN: 2233-7857 IJFGCN

5. Conclusion

The Verilog HDL code is written for Urdhwa Tiryagbhyam Sutra based Vedic multiplier and it has been implemented and tested on Xilinx ISE 14.1i. The code has been synthesized and simulated successfully. The adder is Vedic Multiplier is implemented using Ripple carry Adder. We simulated this adder and analyzed the circuit in terms of the two major performance parameters of VLSI, namely Area, and Delay. Comparison with other multipliers like Array multiplier, Wallace tree multiplier, serial multiplier, and Booth multiplier can be taken as future work. Also the same multiplier can be extended for 32 x 32 bit numbers and 128 x 128 bit numbers multiplication [12] that are suitable for many computation intensive applications.

References

[1] K. Kalai Selvi, R. Arun Sekar , S .Prabu venkateswaran, and S. V. Ramanan "Competent Urdhva Tiryakbhayam (UT) Vedic multiplier using Reversible gate", International Journal of Advanced Science and Technology, Vol. 29, No. 03, (2020), pp. 7026-7035

[2] Vandana Shukla, O. P. Singh, G. R. Mishra, and R. K. Tiwari, "A Novel Approach for Reversible Realization of 4 × 4 Bit Vedic Multiplier Circuit", Proceedings of Int. conf. on Advances in VLSI, Communication, and Signal Processing, Lecture Notes in Electrical Engineering, Vol. 587, Springer, Singapore, (2019) pp. 733- 745.

[3] Yogendri, and Anil Kumar Gupta, "Design of High Performance 8-bit Vedic Multiplier", Proc. Of IEEE International Conference on Advances in Computing, Communication, & Automation (ICACCA) (Spring), Dehradun, India, (2016), April 8-9, pp. 1-6.

[4] Amish Jais, Prasanna Palsodkar, "Design and Implementation of 64 Bit Multiplier using Vedic Algorithm", Proc. Of International Conference on Communication and Signal Processing, Melmaruvathur, India, April 6-8, (2016), pp. 0775-0779.

[5] Swami Bharati Krishna Tirthaji Maharaja," Vedic Mathematics", Motilal Banarsidass Publishers, (1965).

[6] Pushpalata Verma, "Design of 4x4 bit Vedic Multiplier using EDA Tool", International Journal of Computer Applications, Volume 48, No.20, June (2012), pp. 32- 35.

[7] Premananda B.S., Samarth S. Pai, Shashank B., and Shashank S. Bhat, "Design and Implementation of 8-Bit Vedic Multiplierm International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 2, Issue 12, December 2013, pp. 5877 – 5882.

[8] G.Sree Lakshmi, Kaleem Fatima, and B.K.Madhavi, "Implementation of High speed Vedic BCD Multiplier using Vinculum method", Proc. of IEEE Region 10 Conference (TENCON), 22-25 Nov. (2016), Singapore, pp. 147 - 151.

[9] G. R. Gokhale, and P. D. Bahirgonde, "Design of Vedic-Multiplier using Area-Efficient Carry Select Adder", Proc. of IEEE Int. conf. on Advances in Computing, Communications and Informatics (ICACCI), 10-13 Aug. (2015), Kochi, India, pp. 576 – 581.

[10] Yogita Bansal, Charu Madhu, and Pardeep Kaur, "High speed Vedic multiplier design : A review", Proceedings of 2014 Recent Advances in Engineering and Computational Sciences (RAECS), Chandigarh, India, 6 – 8 March, (2014), pp. 1-6.

[11] Monisha Yuvaraj, Nandita Bhaskhar, and Binsu J Kailath, "Design of Optimized MAC Unit using Integrated Vedic Multiplier" Proc. of IEEE International conference on Microelectronic Devices, Circuits and Systems (ICMDCS), Vellore, India, 10-12 Aug. (2017), pp. 1-6.

ISSN: 2233-7857 IJFGCN

[12] Preyesh Dalmia, Vikas, Abhinav Parashar, Akshi Tomar and Neeta Pandey, "Novel High speed Vedic Multiplier proposal incorporating Adder based on Quaternary Signed Digit number system", 31th International Conference on VLSI Design *and 2018 17th International Conference on Embedded Systems (VLSID)* Pune, (2018), pp. 289-294.

ISSN: 2233-7857 IJFGCN