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Implementaion of RISC Processor on FPGA

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Abstract

RISC (Reduced Instruction Set Computer) is a design methodology which supports small and simple set of instructions that all requires the same amount of time to get execute. The proposed processor been carried out with the Harvard Architecture which use separate storage and signal pathways for instructions and data whereas in the other architecture by Von Neumann architecture ,has only one shared memory for instruction and data with one data bus and address bus with between data memory and process memory.. The RISC processor consists of different blocks such as ALU, control unit (controller), register files and data memory unit. In RISC processor, the one instruction per clock cycle is provisioned. Xilinx ISE design suite is used to implement and analyze 16 bit RISC processor on FPGA.

Keywords— *RISC processor, Harvard Architecture, FPGA*

I. INTRODUCTION

The computer systems are one in all the foremost important parts for carrying out any add universe applications. Hence with increase in use of computer systems furthermore as its applications the mandatory changes are done .Due to immense growth within the VLSI technology furthermore as reducing the worth of integrated circuits promotes the employment of RISC processors in computer systems. the provision of simplified instruction set furthermore as less chip space enhances the performance of RISC processor. The employment of RISC processor in smart phones and tablet computers like iPad and android phones provides an oversized user base for RISC based systems.

The RISC processors have simple instructions taking about one clock cycle per instruction. The average per clock cycle per instruction is 1.5. The performance of RISC processor is optimized as the instruction set is reduced. It has only few instructions in the instruction set. These instruction set has variety of different instructions that can be used for complex operations. The RISC processor have multiple register set. The decoding of instructions in RISC processor is very simple. The codes can be programmed and compiled with the help of design suite. The programs will be dumped on FPGA board and results can be obtained.

The rest of the paper is organized as follows. Section II gives idea about then architecture of RISC processor. Section III presents the simulation outputs of blocks of RISC processor. Section IV is about the conclusion.

II. LITERATURE SURVEY

The proposed 16bit RISC processor can be carried out with two methodologies / architecture. The processor can be carried out with Von-Neumann architecture and it can also be carried out with Harvard architecture.In Von-Neumann architecture, there is only one shared memory for instruction and data[6].The 16bit RISC processor can also be carried out with Harvard architecture where there is

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provision of separate memory for instruction and data[4].The basic units of processor can be modelled using behavioral programming and are combined using structural programming[2].The four stage pipelining can also be used to improve overall CPI(clocks per instruction)[2].This 16bit RISC processor with high number of general purpose registers orthogonality and communicates to peripheral devices via serial bus[3].The use of Harvard architecture can be used to increase the reliability and speed of the processor[5].All the modules in the design are coded in VHDL to ease the description ,verification, simulation and hardware implementation[1].
In this paper we have proposed 16bit RISC processor implementation on FPGA(Field Programmable Gate Array) using Harvard Architecture.

III. METHODOLOGY

The proposed processor is of 16bits which supports the Harvard architecture. The Harvard architecture is a computer architecture with separate storage and signal pathways for instruction and data. The processor have load and store structure in which operations will be carried on registers not on memory locations. The RISC processor also have pipelining advantage. The processor will respond to instructions in four phases which are Decode, Read, Process, Write to. Pipelining is defined as the method of fetching the next instruction when the current instruction is being executed. The instruction fetch and execute as pipelined such that fetch takes one instruction per clock cycle while decode and execute take another clock cycle.

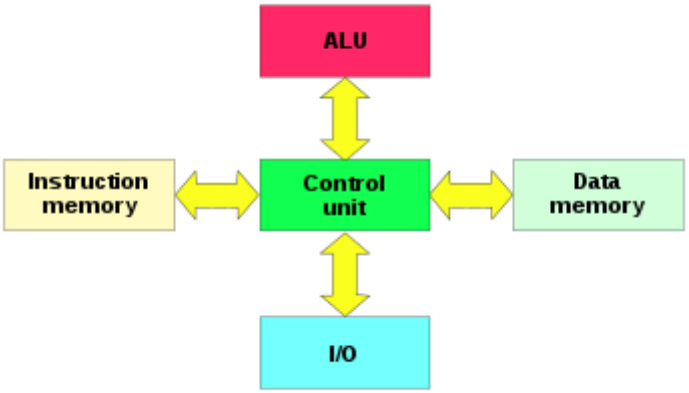

Fig. 1Block diagram of Harvard Architecture

The RISC processor consist of various blocks such as ALU, Register file, program counter, memory address register, multiplexer, instruction register, control unit.

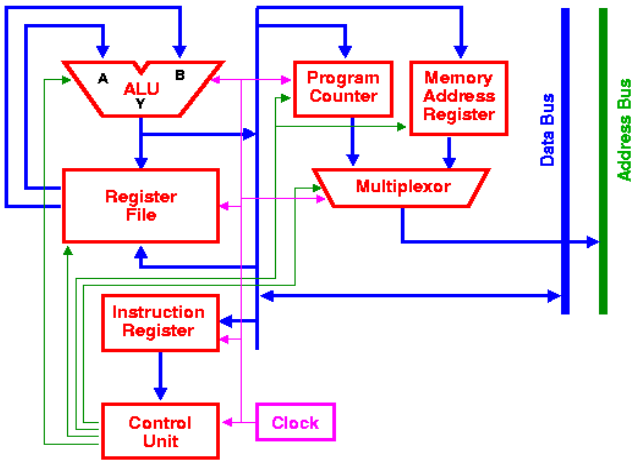

Fig. 2Block diagram of RISC processor

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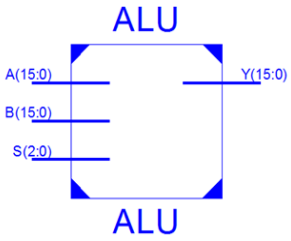
- ALU:- ALU block have 16 operations which consists of AND, NAND, OR, XOR, XNOR, NOT. The arithmetic operations performed by ALU are add, subtract, multiply, divide.
- UNIVERSAL REGISTER:-The Universal Shift Register perform operations consists of right shift operation , left shift operation.
- MULTIPLEXER:-Multiplexer is that the block that selects between several analog or digital input signals and forwards it to one output line.

- PROGRAM COUNTER:- The Program Counter could be a register in an exceedingly compute processor that contains the address of the instruction being executed at this time. Intrinsically instruction get fetched the program counter increases by 1. After each instruction is fetched, the program counter points to next instruction within the sequence.

- CONTROL UNIT:- In this block, instruction, fetch, decode and execute takes place. The instruction which is currently fetching have the contents stored within the program counter(PC).In the first phase ,the instruction and necessary data is obtained within the second phase, the info and directions drawn get separated and activates path to be executed within the execution phase, instruction is executed.

IV. RESULTS

1) ALU:-



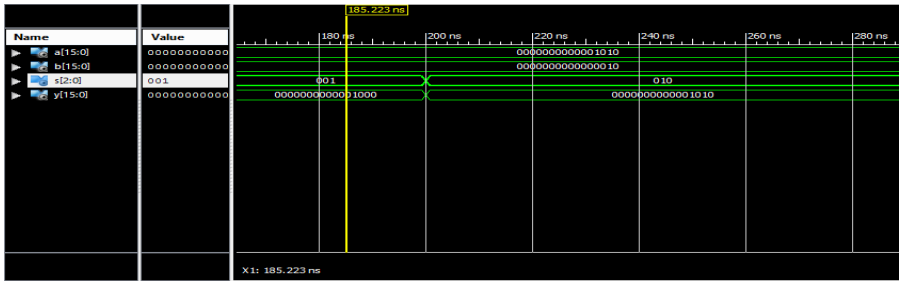
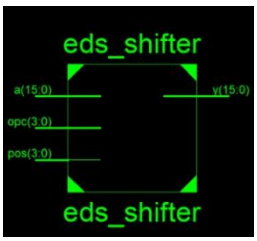


Fig. 3RTL Schematic and test bench output.

2) BARREL SHIFTER:-



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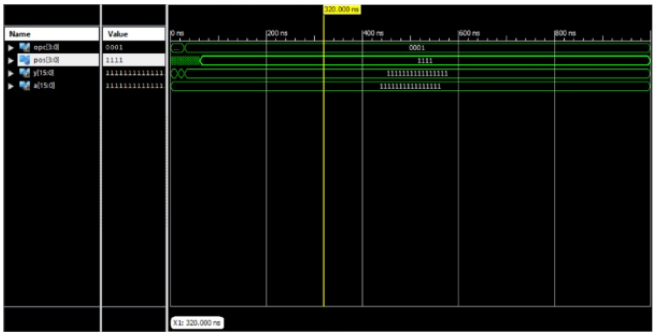
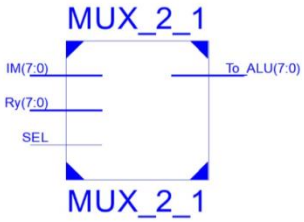


Fig. 4RTL Schematic and Test bench output.

3) MUX:-



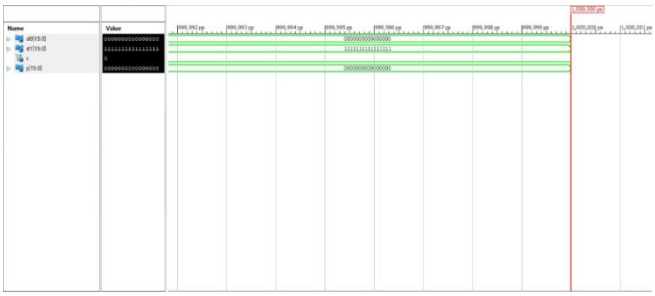


Fig. 5RTL Schematic and Test bench output.

4) USR:-

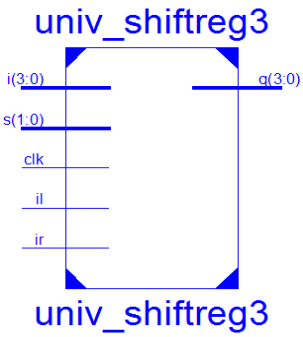


Fig. 6RTL Schematic.

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V. CONCLUSION

16bit RISC processor have been implemented and simulated with help of design tool. Various operations are performed on the designed processor and results are recorded. The synchronization of various operations is done using the clock signal. The designed processor can be implemented on FPGA.

REFERENCES

[1] Karansingh P. Thakor,and Ankushkumar Pal, "*Design of a 16-bit RISC Processor Using VHDL*", International Journal of Engineering Research & Technology (IJERT), ISSN: 2278-0181, Vol. 6 Issue 04, April-2017
[2] Pravin Mane and IndraGupta, "Implementation of Risc Processor on FPGA",1-4244-0726-5/06/$20.00 '2006 IEEE
[3] Jarrod D. Luker and Vinod B. F'rasad, "RISC System Design in an FPGA", Bradley University, 0-7803-7150-X/01/$10.00@200I1E EE
[4] SeungPyo Jung, Jingzhe Xu, DonghoonLee, "Design & Verification of 16 Bit RISC Processor" International SoC Design Conference,978-1-4244-2599-0/08/$25.00 ©2008 IEEE
[5] Chandran Venkatesan and Thabsera Sulthana M "Design of a 16-Bit Harvard Structure RISC Processor in Cadence 45nm Technology", 2019 5th International Conference on Advanced Computing & Communication Systems (ICACCS),978-1-5386-9533-3/19/$31.00 ©2019 IEEE
[6] Shradhha Bhagat and Sheetal Bhandari,"Design and Analysis of 16-bit RISC Processor", Fourth International Conference on Computing Communication Control and Automation (ICCUBEA), 978-1-5386-5257-2/18/$31.00©2018IEEE
[7] Samippa Sakthikumaran and S.Salivahanan,"16bit RISC Processor Design for Convolution Application",Internatonal Conference On Recent Trends in Information Technology,978-1-4577-0590-8/11/$26.00 ©2011 IEEE
[8] Mohammad Zaid and Prof. Pervez Mustajab,"Design And Application Of RISC Processor",978-1-5090-6674-2/17/$31.00 ©2017 IEEE
[9] Akshatha S Patil,B G Shivaleelavathi, "Design and Implementation of Pipelined 8-Bit RISC Processor using Verilog HDL on FPGA",International Research Journal of Engineering and Technology (IRJET),Volume: 04 Issue: 06 June -2017
[10] Jagrit Kathuria, M. Ayoubkhan, Arti Noor, "A Review of Clock Gating Techniques", MIT International Journal of Electronics and Communication Engineering vol 1,no. 2, August 2011

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