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Application of Vedic Mathematics in Multipliers

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Abstract

*Vedic mathematics is the name given to the ancient Indian system of mathematics based on Vedic sutras. Vedic multiplier is based on these Vedic Sutras. The proposed multiplier which uses the concepts of Vedic Mathematics is designed to reduce delay, design complexity, increase speed as well as to decrease power consumption in comparison to conventional multipliers. The project is about high speed Vedic multiplier architecture which is quite different from the Conventional multiplier. A multiplier is an important element in DSP systems, which acts as a building block in most computational digital systems, therefore, speed and power consumption are two important parameters of design. The Vedic Multiplier computed the partial products in a simultaneous manner and the carry was propagated using adders. The high speed multipliers are needed in DSP applications for fast execution. Therefore in this project we implement a 4*4 bit multiplier using Urdhava Tiryagbhyam algorithm using VHDL coding and the output is observed on FPGA kit(Spartan 3E).*

Keywords: *Urdhava Tiryagbhyam, Vedic Multiplier, Carry look-ahead adder, Vedic Mathematics*

I. INTRODUCTION

Multiplication is the key operation in several DSP's for performing operations like convolution, filtering, Fast Fourier Transforms (FFT) and in the ALU units. Multiplication dominates the computational requirements of DSP systems, marking the need for a high speed multiplier system that is efficient in terms of power considerations as well. The demand for high speed processing has seen a constant increase over the years, as a result of expanding signal and computer processing applications. Arithmetic operations with higher throughput are essential to achieve the required performance in many real-time signal and image processing applications.

The reduction of time delay and power consumption forms an essential requirement for many applications. In order to realize these requirements, the multiplier proposed here uses the concept of Vedic Mathematics. Applying the concept of Vedic Mathematics significantly reduce the number of partial products computed, thereby raising the speed of operation of the multiplier. In the case of the Array Multiplier, the products are computed sequentially, raising

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the computational delay. In case of the Booth Multiplier, repeated operations of add or subtract and arithmetic shift are performed, leading to computational delay.

An algorithm in Vedic Mathematics is referred to as Sutra. With respect to multiplication, two main Sutras are put forth to perform multiplication, namely, the Urdhava Tiryagbhyam Sutra. The multiplier proposed here used the concept of Urdhava Tiryagbhyam. This rule puts forth the "vertical and crosswise" concept of performing multiplication of two numbers. Under this algorithm, "crosswise" products are added and are concatenated with the "vertical" products. This parallel computation of products frees the multiplier from the constraint of the processor's clock frequency.

There are four types of ancient mathematics, the Vedas and Vedic mathematics is one of part the four Vedas. The Atharva Veda, the Sthapatya Veda, Yajur Veda, Rig Veda. The Atharva Veda consists of arithmetic, trigonometry geometry, quadratic equations, calculus factor. Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884 - 1960) was the founder of these sutras.After all research in Atharva Veda, Swami Ji described 16 sutras (formulae) and 16 Upa sutras (sub formulas). In present text of Atharva Veda these formulas are not much found because they were implemented by Swami Ji himself. The simplicity in Vedic Mathematics is that calculations can be carried out mentally.

II. LITERATURE SURVEY

There are four types of ancient mathematics, the Vedas and Vedic mathematics is one of part the four Vedas. The Atharva Veda, the Sthapatya Veda, Yajur Veda, Rig Veda. The Atharva Veda consists of arithmetic, trigonometry geometry, quadratic equations, calculus factor.Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884 - 1960) comprised all this work together. After all research in Atharva Veda, Swami Ji described 16 sutras (formulae) and 16 Upa sutras (sub formulas). In present text of Atharva Veda these formulas are not much found because they were implemented by Swami Ji himself.

The simplicity in Vedic Mathematics is that calculations can be carried out mentally. There are many advantages of using mental system.The Vedic mathematics has been divided into sixteen different Sutras which can be applied to any branch of mathematics like algebra, trigonometry, geometry etc.The Sanskrit word "VEDA" is derived from the word "VID", which means to know without limit. It based on the 16 sutras which deals with various fields of mathematics such as algebra, geometry, calculus, and more. The Vedic math's converts complex calculations into easy calculations. The 16 Vedic Sutras are as follows:

- EkhadhikenaPurvena – By one more thanthe previous one.
- NikhilamNavatascaramamDasatah – All from 9 and the last from 10.
- Urdhava-Tiryagbhyam – Vertically and crosswise.
- ParavartyaYojayet – Transpose and adjust
- ShunyamSamayasamuccaye – when the sum is the same that sum is zero.
- (Anurupye)Shunyamanyet – If one is ratio, the other is zero.
- SankalanaVyavakalanabhyam – By addition and by subtraction.
- Puranapuranabhyam – By the completion or non-completion.
- Chalana-Kalanabhyam – differences and similarities.
- Yaavadunam – Whatever the extent of its deficiency.
- Vyashtisamanstih –Part and whole.
- ShesanyankenaCharamena – The remainders by the last digit.

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- Sopaantyadvayamantyam – The ultimate and twice the penultimate.
- EkanyunenaPurvena – By one less than the previous one.
- Gunitasamuchayah – The product of the sum isequal to the sum of product.
- Gunakasamuchayah – The factors of the sum is equal to the sum of factors.

Table1: of Literature Survey

Sr. No.	Reference	Algorithm	Implementation	Delay
1]	FPGA Implementation of Efficient Vedic Multiplier (MukeshD.Patil)[1]	Urdhava Tiryagbhyam	The Vedic multiplier is implemented using ripple carry adder and carry select adder. The main drawback of the adder is speed operation is delay by propagation delay	14.620 ns
2]	High speed multiplier based by Vedic Mathematics (SandyaSubramani)[6]	Urdhava Tiryagbhyam	The implementation is done by breaking down the block of two and each multiplication is propagated using 4bit ripple carry adder	18.64ns**.**
3]	Performance analysis of 4bit Vedic multiplier (VaithiyanathanGurumoorthy)[7]	Nikhilam Sutra	This multiplier is implemented using nikhilam sutra . It is suitable for conventional mathematics.	5.35 ns
4]	FPGA Implementation of Vedic multiplier (Nagaraju.N, Vidyashree)[3]	Urdhava Tiryagbhyam	The multiplier is implemented using design full of compressor instead of full adder	30.02 ns (for 8 bit)
5]	VHDL Implementation of Vedic Multiplier (Siba Kumar Panda. TapasaRanjanSahoo.) [5]	Urdhava Tiryagbhyam	4bit multiplier is implemented by using VHDL code. It is design by using nine full adder and 4 bit special adder	30 ns
6]	FPGA Implementation of 4 bit Vedic Multiplier (S.R.Panigrahi , O.P. Das, T.K. Dey) [4]	Urdhava Tiryagbhyam	The multiplier is implemented by using adder multiplier and MAC	15.88 ns

			unit. They implemented MAC unit using Vedic multiplier.	
7]	Design and analysis of 4 bit vedic Multiplier using carry save adder (Prof. PrasheelThakre.AnkurMaloo. JyotiprakashChowdhary.) [9]	Urdhava Tiryagbhyam	4 bit multiplier is implemented using carry save adder and the partial product is computed using 2 bit adder	2.496 ns
8]	Design and implementation of 4 bit multiplier (Samiksha Dhole , Tirupati Yadav) [10]	Urdhava Tiryagbhyam	In this implementation, Multiplier module is implemented using the four input AND gate and two half adder. It divides number of bits in the input equally in two part.	9.173 ns.
9]	Survey of Performance of Vedic Multiplier (Elakkiya . J Manthan . N) [8]	Urdhava Tiryagbhyam	The 4 bit Vedic Multiplier is implemented by using reversible logic gates.	11.06ns
10]	Novel Delay Efficient Approach for Vedic Multiplier with Generic Adder(N.G.Nirmal , Dr. D.T.Ingole) [15]	Urdhava Tiryagbhyam	This project is implemented by using ripple carry adder and kogge stone adder for verifying various input bits	23.43ns
11]	Design and implementation of high speed 4x4 Vedic multiplier (A DebasishSuhudi, Kanhucharangauda)[11]	Urdhava Tiryagbhyam	The project is implemented using the speed of digital circuit like multiplier using adder in high performance system DSP, Microprocessor	12.82ns
12]	Design , Implementation and performance of vedic multiplier (Vishikha Sharma[1] , *Aniket Kumar [2])[12]	Urdhava Tiryagbhyam	The project is implemented by using ripple carry adder which is one of the digital adder used in many logic Circuits	7.94ns
13]	Design of Vedic multiplier using UrdhvaTiryagbhyam Sutra (Harsha R. , Anilkumar S.R) [13]	Urdhava Tiryagbhyam	The project is implemented by using Urdhava Tiryagbhyam sutra that means vertically and crosswise. It has numerous advantages in terms of area, power, delay, complexity	208.7x10-9
14]	Design And Implementation Of High Speed Vedic Multiplier	Urdhava Tiryagbhyam	This project is implemented by using ripple carry adder	14.79ns

	(HitansuSekhar Sahu[1], Khirod Kumar Sethi[2], Tejesh Kumar Chaudhary)[14]		in which all full adder are cascaded in series	
15]	Vedic Mathematics or Sixteen Simple Sutras From The Vedas(Jagadguru Swami Sri Bharath, Krishna Tirathji) [2]	Vedic Sutras	This paper represents the study of all the Vedic Sutras.	

III. IMPLEMENTATION

The algorithm is written for the 4x4 Vedic Multiplier and the general method is shown in FIG 1. In the first step, the two numbers are broken down, and each number is divided into two parts of 4 bits each. A vertical as well as crosswise multiplication operation is performed, which involves the vertical multiplication of the LSBs together and the MSBs together. The crosswise multiplication operation is performed between the LSBs and the MSBs.

The carries generated in are propagated through the system and added to the next corresponding bit using respective carry look-ahead adders. The product of MSBs and LSBs are passed through two separate carry look ahead adders and added with the carry and sum of the previous stages. Thus, the final product that is obtained is a collection of sum and carry bits of the last stage adders.The parallelism in generation of partial product improves the speed of multiplication.

For computing big multiplication of N X N, the number is divided in to small blocks and utilize for design. For higher number of bit some modification is required. Divide the number in to two equal parts. Let's analyze 4 x 4 multiplication, Say $X_3X_2X_1X_0$ and $Y_3Y_2Y_1Y_0$. The result of multiplication of these two numbers is given by $M_7M_6M_5M_4M_3M_2M_1M_0$.

Let's divide the X and Y into two parts say X_3X_2 and X_1X_0 for X and Y_3Y_2 and Y_1Y_0 for Y. For the proposed Vedic multiplication method consider 2 bit at a time and perform the multiplication by using 2bit multiplier. The FIG 1 structure shows the multiplication of 4 x 4 number using Vedic multiplier. Each block as shown above is 2 x 2 multiplier. X_3X_2 and Y_3Y_2 are given as input to first 2 x 2 multiplier.X_3X_2 and Y_1Y_0 is given as input to second block. X_1X_0 and Y_3Y_2 is given as input to the third block of multiplier. X_1X_0 and Y_1Y_0 is given as input to last block. The final result of multiplication is of 8 bit say $M_7M_6M_5M_4M_3M_2M_1M_0$, calculated as given below in FIG 1.

Assuming the output of each multiplication is as given above. For the final result, the multiplication result of each 2x 2 multiplier block is arranged in specific manner as shown in the FIG 2. Add the middle product term along with the term shown below. The first two outputs M_0 and $M1$ are same as M_00 and M_01. One 4bit full adder is used to add the ($M_23M_22M_21M_20$) and ($M_13M_12M_11M_10$).

The result of addition of the 1st adder is added with the ($M_31M_32M_03M_02$). The result of addition of the 2nd full adder gives $M_5M_4M_3M_2$bit of final multiplication. The carry generated during first full adder operation is added using half adder with carry generated during second full adder operation. The final sum and carry of half adder is added with M_33M_32 which gives M_7M_6 bit of final multiplication result.

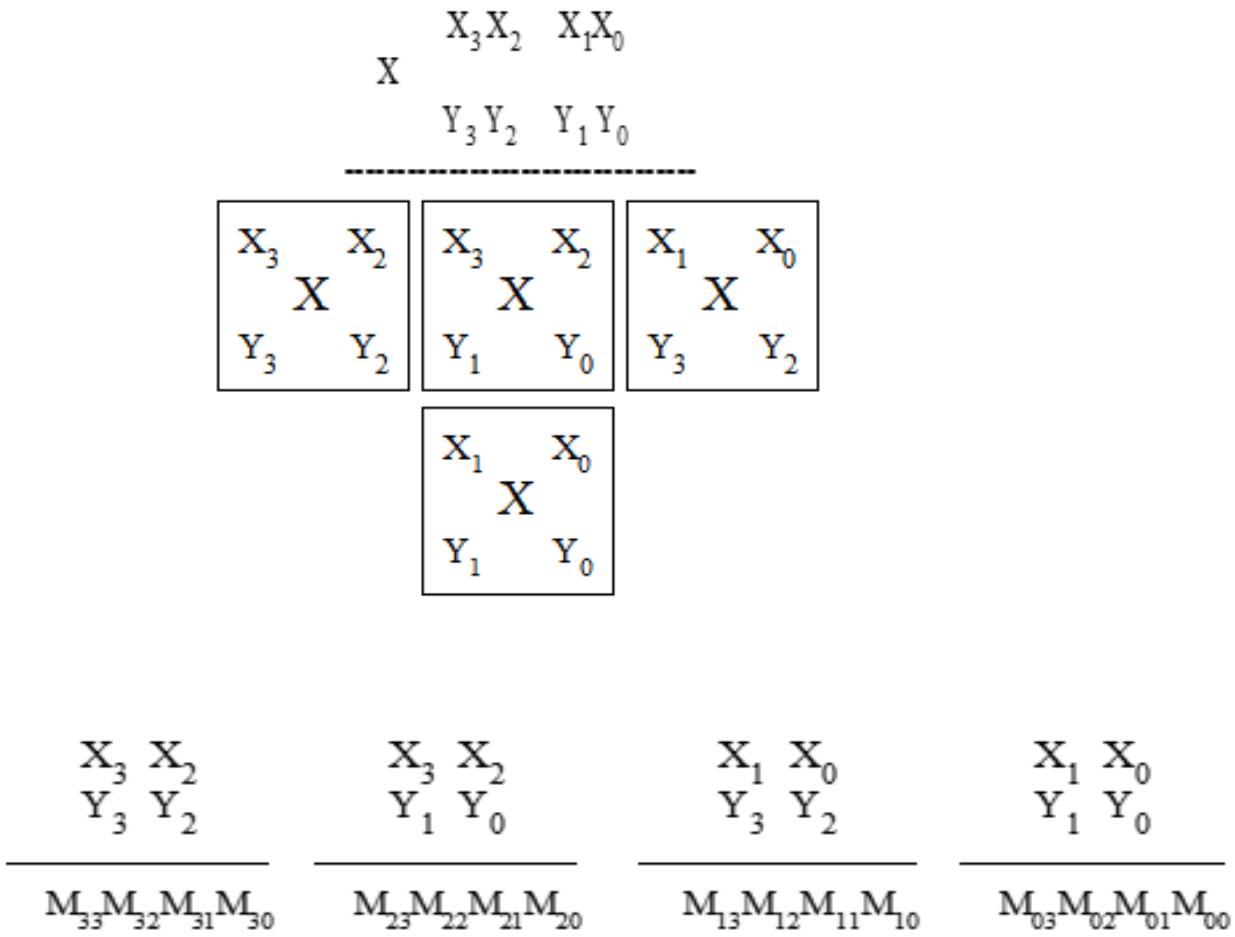

FIG 1. URDHAVA TIRYAGBHYAM STEPS FOR 4 BIT MULTIPLICATION

$$M_{33}\,M_{32} \quad M_{31}\;M_{30}\;\;0\;\;0\quad M_{01}M_{00}$$

$$M_{23}\;M_{22}\;M_{21}\;M_{20}$$

$$M_{13}\;M_{12}\;M_{11}\;M_{10}$$

$$0\quad 0\quad M_{03}\;M_{02}$$

FIG 2. STEPS FOR MULTIPLICATION.

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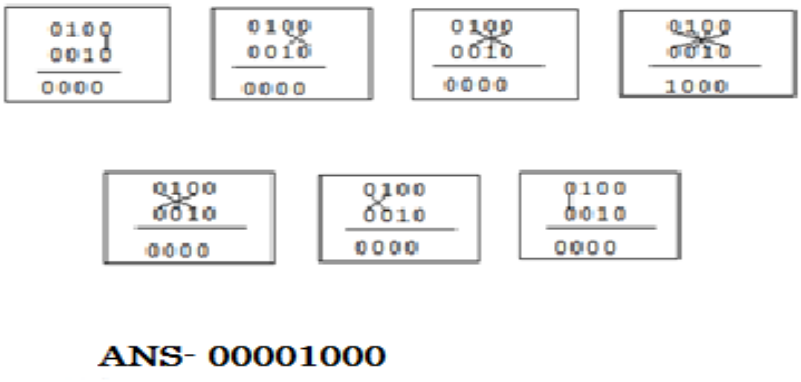

ANS- 00001000

FIG 3. EXAMPLE OF URDHAVA TIRAGBHYAM ALGORITHM

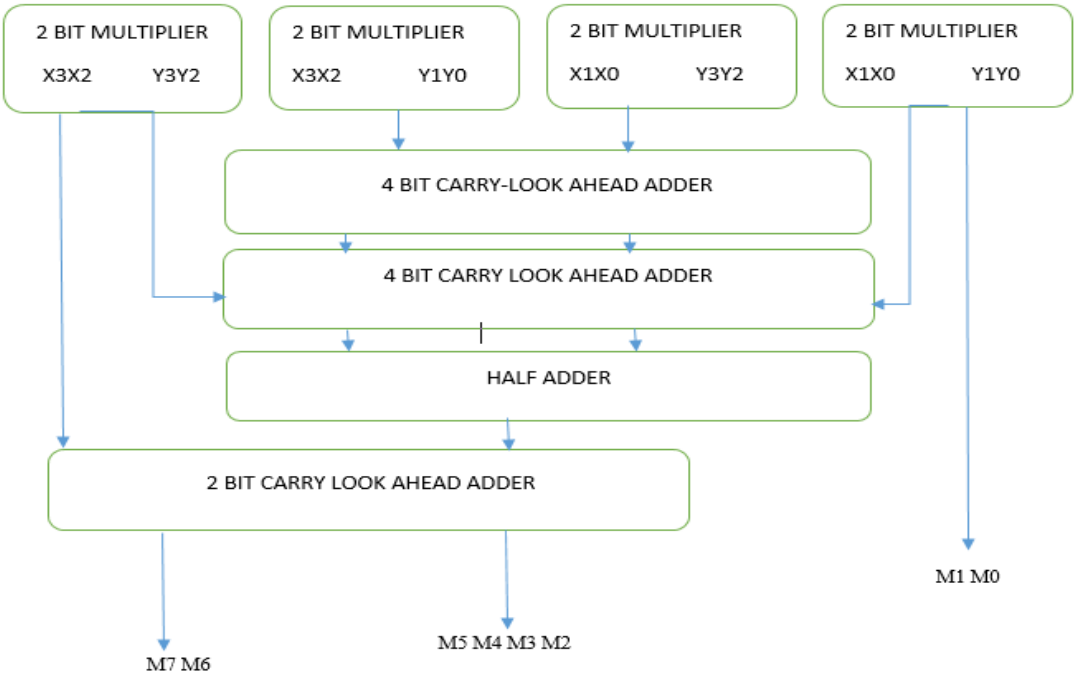

FIG 4. ARCHITECTURE OF 4 BIT VEDIC MULTIPLIER

IV. RESULTS

The results of 4bit multiplier is shown below:

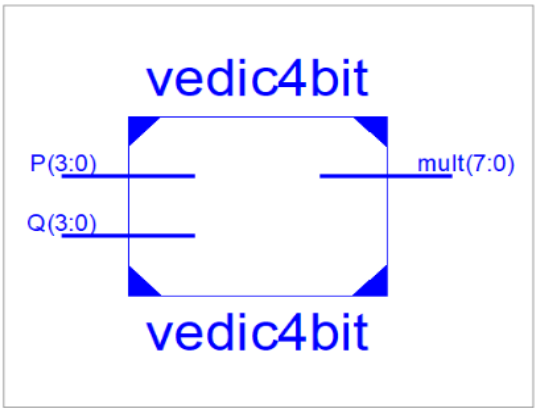

FIG 4(a). 1ST LEVEL RTL SCHEMATIC DIAGRAM OF 4x4 VEDIC MULTIPLIER

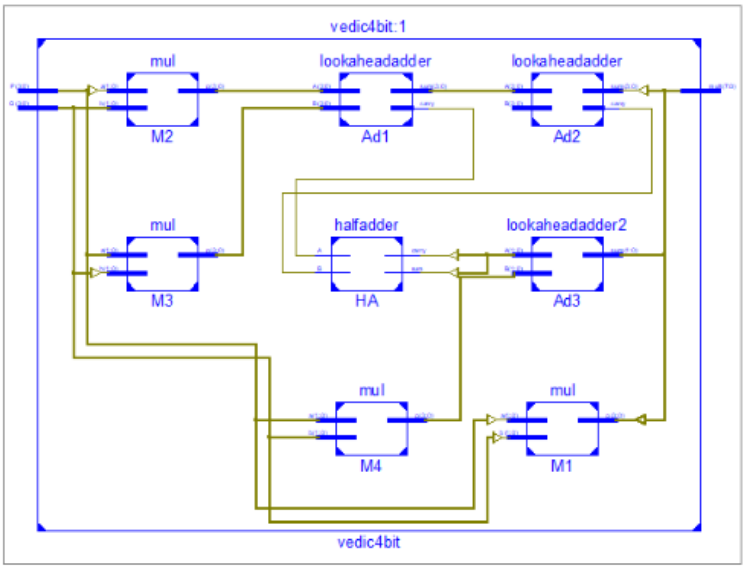

FIG 4(b): 2ND LEVEL RTL SCHEMATIC DIAGRAM OF 4x4 VEDIC MULTIPLIER

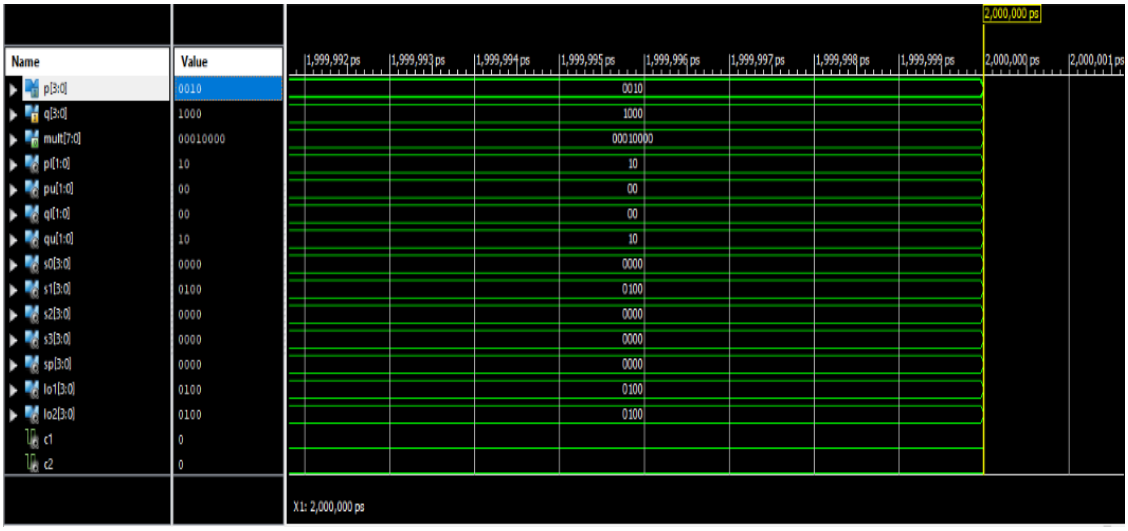

FIG 5. SIMULATION DIAGRAM OF 4x4 BIT VEDIC MULTIPLIER

THE TIMING RESULTS ARE SHOWN BELOW:

Timing constraint: Default path analysis
Total number of paths / destination ports: 414 / 8

Delay: 11.823ns (Levels of Logic = 8)
Source: P<1> (PAD)
Destination: mult<6> (PAD)

Data Path: P<1> to mult<6>

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	10	1.106	0.902	P_1_IBUF (P_1_IBUF)
LUT2:I0->O	5	0.612	0.690	M2/q1 (M2/q)
LUT4:I0->O	3	0.612	0.520	Ad1/Mxor_p<1>_Result2 (lo1<1>)
LUT3:I1->O	1	0.612	0.426	Ad2/c_3_or000027_SW0 (N11)
LUT4:I1->O	2	0.612	0.532	Ad2/c_3_or000027 (Ad2/c<3>)
LUT4:I0->O	2	0.612	0.449	Ad2/c_4_or00001 (c2)
LUT4:I1->O	1	0.612	0.357	Ad3/Mxor_p<0>_Result1 (mult_6_OBUF)
OBUF:I->O			3.169	mult_6_OBUF (mult<6>)

Total 11.823ns

Table 2: for Device Utilization Summary

LOGIC UTILIZATION	USED	AVAILABLE	UTILIZATION

Number of slices	21	960	2%
Number of 4 input LUTs	37	1960	1%
Number of Bonded IOBs	16	66	24%

V. CONCLUSION

Vedic multiplier can be used for many applications. Multiplication is the most fundamental operation in several DSPs for performing operations like convolution, filtering, Fast Fourier Transforms and in the ALU units. In this project a 4bit Vedic multiplier using Urdhava Tiryagbhyam algorithm is implemented. The proposed 4x4 bit Vedic multiplier has computational delay path of 11.823ns. Thus it is proved that Vedic multiplier is much faster than the conventional multipliers.

VI. FUTURE SCOPE

Vedic Mathematics developed about 2500 years ago, gives us a clue of symmetric computation. Vedic mathematics deals with various topics of mathematics. If Vedic mathematics are used to implement hardware, it will reduce the computational speed drastically. Therefore, it could be possible to implement to complete ALU using Vedic Mathematics methods. The methods can also be used in FFT's and the IFFT's. By using these ancient methods world can achieve new heights of performance and quality for the cutting edge technology devices.

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