# PLD Based Hardware Realization Of Digital Clock 

Umashankar More ${ }^{\# 1}$, Biswajeet Sahoo ${ }^{\# 2}$, Sherly Shroff ${ }^{\# 3}$, Vineet Mehta ${ }^{\# 4}$<br>\# Department of Electronics and Communication Engineering, MIT School of Engineering<br>${ }^{1}$ umashankar.more@gmail.com<br>${ }^{2}$ biswajeet.1999sahoo@gmail.com<br>${ }^{3}$ shroffsherly@gmail.com<br>${ }^{4}$ vineetmehta26@gmail.com


#### Abstract

A Digital Clock is a type of Clock that displays the time digitally, unlike the analog clock, where the time is indicated by the positions of rotating hands. TIME is a fundamental concept that it is very difficult to define. To measure time is needed something that will repeat itself at regular intervals. The number of intervals counted gives a quantitative measure of the duration [1]. The earliest references for the measurement of the time were the moon and sun. When the sun and the moon were not visible, it was impossible to know the exact time. So, clocks were developed to measure out the hours between checks with the sun and the moon. The process of measuring time has progressively become more accurate, and the devices more localized ever since. In today's modern era, the time is predominately measured by mechanical, and recently by electronic clocks. In this project the attempt is made to realize digital clock hardware from reference of crystal oscillator clock input using Field Programmable Gate Array (FPGA) based prototyping method [2].


Keywords- Field Programmable Gate Array (FPGA), Application Specific IC(ASIC), Binary Coded decimal (BCD), Hardware Description Language (HDL), Verilog Hardware Description Language (VHDL).

## I. Introduction

The objective of the digital clock is to display time digitally using seven segment display on FPGA Board. The digital clock designed is in 24hour format. It displays the time in format of hours: minutes: seconds.

Figure 1.1 shows System Block Diagram. These days numerous applications in electronics and other technology are using digital technique to perform operations that were once performed by analogue methods. Digital systems are more versatile and superior to that of the analogue method as they do not get affected by spurious fluctuation in voltage, have greater precision and accuracy and can store billions of bits of information in relatively small space [3]. Many developments have been done in designing prototypingplatforms so as to provide single chip solution for variety of applications. FPGA platform is of same kind to provide better performance and flexibility while implementation.


Figure 1.1. System Block Diagram
The FPGA arrangement, specified using HDL is similar to one used for Application Specific IC(ASIC)[4]. This project intends use of FPGA for the hardware implementation of Digital Clock. The FPGA and on-board clock generate timing signals. The proposed digital design uses processes viz. counting, comparing, incrementing and displaying clock output[3]. System block diagram shows that actually it is precise division of the clock of crystal oscillator, generated on board. This clock is divided for generating 1 Hz clock frequency. Derived 1 Hz clock signal is now reference clock of the system. It is used as fundamental time unit of our Digital Clock.

Block diagram shows that 2 digits are used for displaying each time unit viz. second, minute and hour. This leads to display total 24 hours clock. Binary Coded decimal (BCD) counters are used for each digit so as to display corresponding digits in the range of $0-9$. 'Overflow signal' of preceding counter is clock of sub-sequent counter. Hence entire system is ripple BCD Counters having different threshold values. Interconnections between these counters is shown in figure 1.1. Each BCD counter data is displayed on 7 segment display with the help of BCD to 7 Segment Converter[1].

There are 3 blocks in total, namely Hours, Minutes and Seconds. Output of 1 second clock generator logic is 1 sec duration signal and applied to lower significant digit of seconds. Clock will become reset after 24 hours.

## II. METHODOLOGY

The clock of 50 MHz from the clock source of FPGA Board is divided using clock divider logic to get a period of 1 second. This 1 second signal is applied to our system as 1 second signal periods. When number of seconds becomes 59 (begins with ' 0 '), 'minutes' starts its counting. Consequently when 59 minutes (begins with ' 0 '), are over, 'Hour' starts progressing. It counts till 23:59:59. After this it would be 00:00:00 which is indication of 24 i.e. zero hour. Digit wise it has been explained below in Figure 2.1. Flowchart of digital clock


Figure 2.1. Flowchart of Digital Clock
Initialise the Least Significant Digit (LSD) and Most Significant Digit (MSD) of second, minute and hour to 00:00:00. Then clock pulse triggers an increase in the second's LSD. After every clock pulse an increment of unity is addition in the second's LSD. After getting the maximum value of 9, increment is in the second's MSD. Then again, we start the count at second's LSD Simultaneously LSD also keeps updating where it again increases till 9. After that there is again an increment in the MSD of second. After repeating the same loop in the MSD there is increment till the value is set to 5 . Then after that the loop will forward with LSD of minute. It will follow the same loop for the LSD and MSD of the minute and hour. The increment will be done when the LSD of minute reaches to 9 and MSD reaches to 5. Similarly, for hours LSD of hour reaches to 3 and MSD reaches to 2. After all the time reaches to 23:59:59 the clock will reset and all the LSD and MSD of second, minute and hour will initialise to 00:00:00 again. This Process continues.

## III. SYSTEM DESIGN

## A. CALCULATIONS:

On board clock of 50 MHz is working as master clock.
In 1 second of time $50 \times 10^{6}$ number of pulses of 50 MHz will be passed. Then, duration of 1 period of 50 MHz clock is $0.02 \mu \mathrm{~s}$. A pulse comprises of an 'ON' time of 0.5 Sec and 'OFF' time of 0.5 Sec . Therefore, number of pulses in each of them will be 2,49,99,999.

It implies that in a period of 1 second, we get two transitions and time between two successive transitions will be 0.5 Second and number of pulses passing through ON and OFF time is 2,49,99,999. Therefore, binary code of $2,49,99,999$ is 1011111010111100000111111 for on time (rising edge) of 0.5 sec and off time (falling edge) of 0.5 sec .

## B. RTL Schematic



Figure: - 3.1. RTL Schematic of Digital Clock
There are 2 input pins which are connected to FPGA board. The 'clock' is pin for the 50 MHz master clock of FPGA Board and the 'reset' is the master reset which connected to system.
At output side, we have 8 output signals. Six signals of 7 bits each are sec_LSD, sec_MSD, min_LSD, min_MSD, hour_LSD, hour_MSD. Each seven bits signal is seven segment output connected to seven segment display. Seven segment display is connected in common anode configuration. The pins receive the 7 -segment data from the BCD to seven segment block as shown in figure 1.1. Rest of the 2 pins are showing 'day' and 'one second clock' respectively.
The figure 3.1. shows the 8 -input pins which are connected to FPGA along with one clock for clock signal and a reset pin. Then there are 6 output pin that is connected to 7 segment led display. There are six registers in total which includes 2 separate register for each block i.e. 2 for hours (Hin0, H_in1), 2 for minutes ( $M \_i n 0, M_{-} i n 1$ ) and 2 for seconds (S_in0, S_in1) as well. When S_in0 is 9 and S_in1 is 5, then S_in1 and S_in0 values are made to zero and M_in0 value is incremented. If M_in1 is 5 and $M_{\_}$in0 is 9 then $M \_$in 1 and $M \_$in0 values are made to zero and $H \_i n 0$ is incremented. If $H \_i n 1$ is 2 and $H_{-}$in0 is 4 then $H_{-}$in 1 and $H_{-}$in0 is made to zero and thus the count continues.

In the figure 3.2. we get more detail explanation of the RTL schematic and a verification for the figure 1.1 i.e. the block diagram. By this figure we get to know that 1 sec clock is given to the BCD counter of 9 (sec LSD) then after these 9 counts the overflow signal is sent to the BCD counter of 5 (sec MSD) and the overflow signal becomes clock for the BCD counter 5. Same method is implemented for the minutes and hours. The BCD counter are of $5,9,2$ and 3 . After the overflow signal is generated by the MSD of hour (BCD counter of 3 ) the overflow signal is given to the day pin. Simultaneously the value stored in the BCD counters are shown in 7 segment led display by the output pins i.e. sec_LSD, sec_MSD, min_LSD, min_MSD, hour_LSD, hour_MSD.


Figure 3.2. Combination of all the blocks in Digital Clock
In Digital clock is consisting of 2 parts i.e. is the clock and bcd to hex converter. We see the RTL schematic in figure 3.1. and in figure 3.2. it shows detailing of RTL schematic and parts used. The 6 output pins receive the from bcd to hex block and the 1 sec clock output is received by the master clock which uses the 50 MHz clock of FPGA and converts it to 1 second which is used.

## IV. RESULT

Device utilization summary:
Selected Device: 3s250ecp132-5 FPGA

| Number of Slices: | 57 out of 2448 | $2 \%$ |
| :--- | :--- | :--- |
| Number of Slice Flip Flops: | 56 out of 4896 | $1 \%$ |
| Number of 4 input LUTs: | 110 out of 4896 | $2 \%$ |
| Number of IOs: | 46 | $50 \%$ |
| Number of bonded IOBs: | 46 out of 92 | $4 \%$ |
| Number of GCLKs: | 1 out of 24 |  |

Table 4.1. Device utilization summary
The waveform shows that there are various signals i.e. master clock, master reset, sec_LSD, sec_MSD, min_LSD, min_MSD, hour_LSD, hour_MSD, one_sec clock, day and clock period. The sec_LSD, sec_MSD, min_LSD, min_MSD, hour_LSD, hour_MSD are receiving the 7 -segment data.

Initially in the sec_LSD the value stored was 1000000 i.e. 0 on 7 segment sec_LSD and after a delay of $0.02 \mu \mathrm{~s}$, the value stored increases to 1111001 i.e. 1 .

In the second waveform we see that sec_LSD the value stored was 0010000 i.e. 9 on 7 segment sec_LSD and in next subsequent clock cycle it reset and there is advancement in the sec_MSD. The value of sec_MSD advances after 10 secs.


Figure 4.4. Waveforms of Digital Clock presenting 1 second in S_LSD


Figure 4.5. Waveforms of Digital Clock presenting increment in seconds S_MSD

## V. CONCLUSIONS

In this paper, Digital Clock displays time in secs, minutes and 24 hours. Digital Clock has implemented and verified in HDL language. By division of the counter maximum clock frequency of system is improved. The Digital Clock is designed by creating HDL codes and synthesizing them using a simulation and synthesis tool. Quite precisely 1 second clock is obtained from master clock of 50 MHz using clock divider by setting the 25-bit counter i.e. ' 1011111010111100000111111 ' and 24 hours digital clock is presented in $00 \mathrm{H}: 00 \mathrm{M}: 00 \mathrm{~S}$ display format.

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