International Journal of Future Generation Communication and Networking
Vol. 13, No. 3, (2020), pp. 974–981

Low Power Resource Efficient Ternary Content Addressable Memory Using Multiport SRAM

A.Vijayalakshmi
Department of Electronics and Communication Engineering
Sri Manakula Vinayagar Engineering College,Pondicherry University
Puduchery,India
vijilakshan@gmail.com

C.Sridhar
Department of Electronics and Communication Engineering
Sri Manakula Vinayagar Engineering College,Pondicherry University
Puduchery,India
sri.induss@gmail.com

S.Ramya
Department of Electronics and Communication Engineering
Sri Manakula Vinayagar Engineering College,Pondicherry University
ramya.subram@gmail.com

Abstract

A Ternary Content addressable memory (TCAM) performs search operation by comparing input string with the stored data at high speed. TCAM is popular in high speed packet classification, forwarding and network switches. TCAM functionality is emulated with SRAM to overcome the limitations of TCAM such as small storage quantity, complex memory structure and high energy consumption. Resource Efficient SRAM based TCAM (REST) architecture utilize the functionalities of TCAM using optimal resource. The low power REST architecture has been proposed with 72X28 multiport SRAM to improve the speed and to reduce the power consumption of TCAM. In this proposed architecture, the virtual blocks of multiport SRAM unit is used to store the address information given in the TCAM. A72x28 low power REST architecture is simulated using modelsim and Xilinx Vivado.

Keywords— *Ternary content addressable memory (TCAM), Random access memory (RAM), Resource efficient SRAM based TCAM (REST), multiport SRAM, Virtual block.*

I. INTRODUCTION

Ternary content addressable memory (TCAM) is a memory that analyses the input data with the preloaded contents and generates a matched address as output. The content stored in the memory is searched with respect to input data and provide the corresponding address as the output. The entire content is searched within a single clock cycle. It can match based on three states such as 0, 1 and X where X denotes don't care condition. The X state can be matched to both 0 and 1 during a comparison operation and it allows compressing the data entries. The X state storage features of TCAM provide the ability for storing variable size data in the tables. The most attractive feature of TCAM is construct tables for longest match searching such as routing tables. Most often the TCAM is used to perform partial matching of data.

The major advantages of TCAM are searching speed, simplicity and performance. The limitations are power dissipation, low storage density, complex circuitry and higher cost due to large number of transistor. Speed, area and power dissipation are the three important factors for designing the TCAM which become the challenges for the designer. TCAM is used in different applications such as network routers, real time analysis application, packet forwarding and classification. The possibility of design

ISSN: 2233-7857 IJFGCN

and implementation of native TCAM is high in the Application specific integrated circuit (ASIC) area. But in case of FPGA, there is no availability of TCAM feature. In order to make the presence of TCAM feature in FPGA world, functionality of TCAM is emulated using SRAM. Network devices oriented application requires this kind of features in FPGA implementation. In this paper, low power REST (Resource efficient SRAM based TCAM) using 72X28 multiport SRAM is designed and implemented on Xilinx vivado and modelsim. The proposed architecture improves the searching speed of the TCAM operation and reduces one of the major design factors of TCAM memory (i.e) power dissipation.

The rest of the paper is organized as follows section 2 explains the emulation of TCAM based on the SRAM. Section 3 elaborates the operation of TCAM and architecture of low power REST. Section 4 shows the implementation of low power REST architecture on Xilinx and modelsim. Section 5 provides the parameter analysis of proposed architecture and compares the proposed low power REST architecture with the existing REST architecture. Section 6 gives the conclusion and focus on the direction of future work of the proposed architecture.

II. RELATED WORK

SRAM based TCAM have been implemented on Xilinx to bring the availability of CAM into the FPGA platform. Low power RAM based hierarchical CAM [1] was implemented on FPGA for reducing the power consumption using power optimization techniques. Low power TCAM design using a segmented match line [2] was designed to reduce the match line power consumption. To improve the limit of implementing large TCAM, scalable Ternary Content Addressable memory implementation using FPGA [3] was proposed. Z-TCAM [4] has been proposed to emulate the functionality of TCAM by logically dividing the TCAM tables along column and row into hybrid table and large capacity of TCAM was ensured.

HP SRAM based TCAM [5] have been proposed to support the large input pattern. To improve the speed and reduce the power consumption, UE-TCAM [6] has been implemented on Xilinx Virtex-6 FPGA. Hybrid TCAM and SRAM scheme[7] was proposed to reduces the area, power consumption and also the search performance of the TCAM implemented on Xilinx. Resource efficient SRAM based TCAM architecture [11] [12] has been proposed to achieve the memory utilization that have the tradeoff between memory utilization and throughput. In this architecture, the functionality of TCAM was emulated in the virtual block of signal port SRAM.

III. PROPOSED WORK

A. TCAM operation

TCAM consist of core cell, match lines, search lines and priority encoder. The basic operations of TCAM are storage of bit and comparison operation. Usually TCAM cell are designed using NOR type or NAND type cell. The NOR type TCAM cell are implemented as NOR type that achieve high search speed with high power consumption. The TCAM cells are implemented as XNOR type in a NAND type TCAM which attains efficient power with low speed. Once the input data entry is made to the TCAM, data are loaded into the search line driver. The search line driver transmits the word on the search lines. At the same time, the match lines are precharged to high.

Fig.1. illustrates the function of TCAM[8].TCAM core cell compares the input data on the search lines with the stored bit. Once the match is found, match line remain high otherwise it will discharge to low. If more than one match is made, priority encoder is used to select highest priority match address. Each entry of TCAM comprise of value, mask and result. The field of value and mask are 134 bit in length and TCAM entries[9] are arranged based on the mask value.

ISSN: 2233-7857 IJFGCN

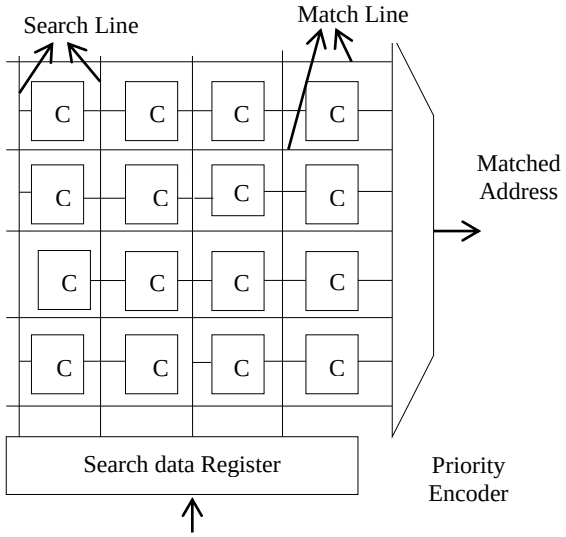

Fig .1 Functional Diagram of TCAM

Usually TCAM cell are designed using NOR type or NAND type cell. The NOR type TCAM cell are implemented as NOR type that achieve high search speed with high power consumption. The TCAM cells are implemented as XNOR type in a NAND type TCAM which attains efficient power with low speed.

B. Low power REST architecture

A low power REST block includes a 72X28 multiport SRAM with four VBs for a table, four number of distributed RAMs for early elimination (EE) tables, multiport SRAM memory, a priority encoder and AND gates to conduct the TCAM emulation

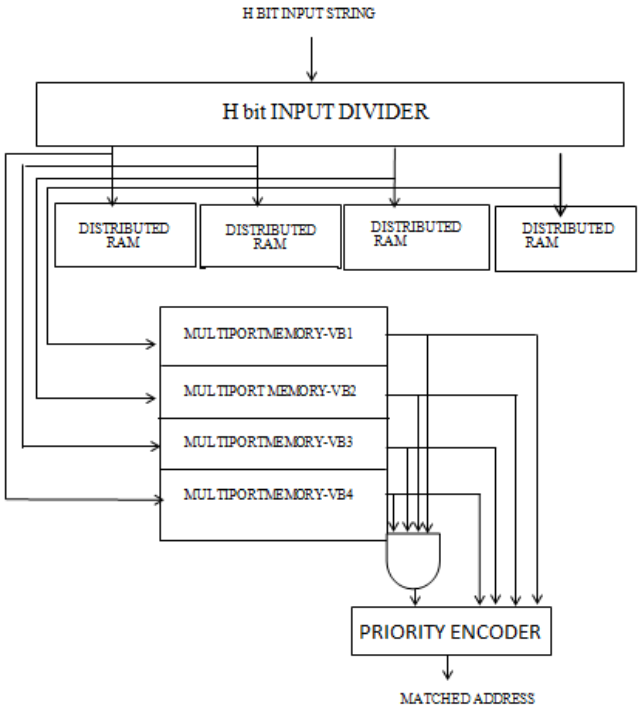

Fig 2. Block Diagram of Low Power REST Architecture

. For search operation, fixed length binary query string (QS) are required to access the SRAM. The H bit (28 bit) query string is the input to the low power REST architecture, the input H bit string (28

ISSN: 2233-7857 IJFGCN

bit) is partitioned into the four 7 bit substring using bit divider. The partitioned four 7 bit substring is applied to the distributed SRAM which is implemented using look-up tables available in each slice and size of the distributed SRAM is depend upon the size of the look up table.

The distributed SRAM in this architecture acts as elimination table that checks for the partitioned four 7 bit substring in multiport SRAM. If the partitioned four 7 bit substring is presented in the multiport SRAM, the process proceed for searching operation. If the partitioned four 7 substring is not present in the multiport SRAM, then the substring is stored in the multiport SRAM memory for future purpose.

The partitioned four 7 bit substring is applied to the multiport SRAM for storage or search operation. The multiport SRAM memory is logically divided into the virtual block for the storage of original address and data string in the TCAM table for the purpose of emulating TCAM with the same dimension. The size of the virtual block depends upon the dimension of the TCAM table[10]. As the number of VBs increases, ETB (emulated TCAM bits) also increases in low power REST. Then the matched address is sent to the AND gate that processes the matched address and produce the n number of W bit enable signal to the priority encoder. Among the multiple matching address, priority encoder selects the highest priority matching address and produce a single search operation. In the low power REST architecture, low matching address receives higher priority and high matching address receives lower priority.

To create and emulate the functionality of large TCAM into the FPGA, single low power REST architecture is arranged in array form structure. All low power REST blocks are arranged and executed in parallel and generate single matched address with the help of priority encoder.

IV. SIMULATION RESULTS

TCAM is an associate memory that is used to search the address location of the input data strings. The functionality of TCAM is emulated into SRAM for improving the performance, complex memory structure and power consumption. The low power REST architecture is implemented using the Modelsim and Xilinx vivado software. VHDL is hardware description language used to code the logic of low power REST architecture in the modelsim and Xilinx vivado software tool. The waveform result of low power REST architecture is obtained using modelsim Software. The analysis result of parameters such as delay, power, area and RTL view of architecture are obtained using Xilinx vivado software.

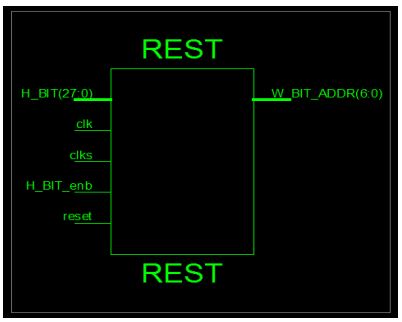

Fig .3. RTL View of Low Power REST

The simulation part of low power REST[13] architecture is categorized as simulation of H Bit divider, distributed RAM, The simulation part of low power REST architecture is categorized as simulation of H Bit divider, distributed RAM, multiport, virtual block, AND gate and priority encoder. All the simulation part is combined into single part to obtain the low power REST and compared the power, area and delay of low power REST with the existing REST architecture. The RTL view of low power REST architecture obtained using Xilinx vivado is shown in the Fig.3.

The internal RTL view of low power REST architecture shown in Fig.4.It consumes the bit divider with input of 28 bit string. The 28 bit string is divided into the four 7 bit substring and feeded into individual distributed RAM for early elimination of divided 7 bit substring. After elimination

ISSN: 2233-7857 IJFGCN

stage, the search operations will being for the 7 bit substring stored in the TCAM table that is feeded on the virtual block of the multiport SRAM.

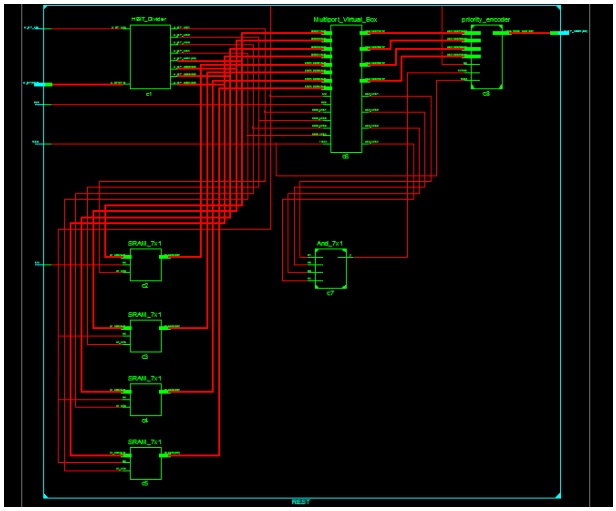

Fig.4. Internal RTL View of Low Power REST

The 7 bit substring does not present in the TCAM table will be stored. The substring is compared with the stored TCAM table in the virtual block of SRAM and matched address is sent as output of multiport SRAM. Among the multiple matched addresses, single matched address is selected with the help of priority encoder.

The simulation result obtained for the low power REST architecture using modelsim is shown in Fig.5 and Fig.6. The input data string (0400000) and bit enable signal (1) is given to the low power REST system. The input data string is divided into four sub string as h_bit_data1 as 0000000, h_bit_data2 as 0000000, h_bit_data3 as 0000000 and h_bit_data2 as 0000010 using h bit divider.

The distributed RAM checks the data with the memory for early elimination. The divided input data string is compared with the stored data string in the virtual box of the multiport SRAM. Priority Encoder selects single matched address of 0000010 as 1.

Table.I. Comparison of single SRAM and multiple port SRAM with REST

PARAMETERS	SINGLE PORT SRAM (REST)	MULTIPORT SRAM (LOW POWER REST)
Number of Slice Registers	390	199
Number of Slice LUT	130	232
BRAM	1	8
Total power (mW)	112.83	15

ISSN: 2233-7857 IJFGCN

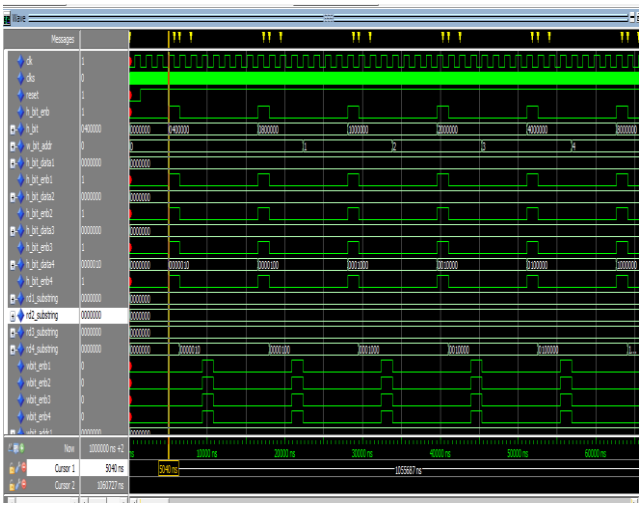

Fig.5. Simulation of Input Data String of Low Power REST

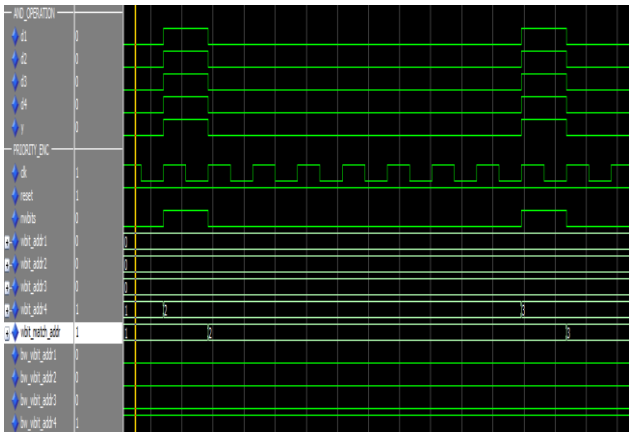

Fig.6.Simulation of Priority Encoder of Low Power REST in Modelsim

V. RESOURCE UTILIZATION COMPARISON OF LOW POWER REST ARCHITECTURE WITH REST

The comparison for various parameters like power, area, number of Look Up Table, number of slice register and BRAM are listed in the Table 1.These parameters analysis are obtained by implementing the architecture in the Xilinx vivado software and power consumption is measured using Xilinx power analyzer tool.

From the below tabulation it shows that proposed Low power REST architecture is more efficient in power, when compared to the existing REST system[12].Due to 72 X 28 multiport SRAM usage for emulating the TCAM functionality, area occupied by the proposed architecture is high than the existing work architecture. The delay measured for the low power REST architecture is 5.558ns.

VI. CONCLUSION

Low power resource efficient SRAM based TCAM architecture has been proposed to emulate the functionality of TCAM into the 72x28 multiport SRAM for increasing the speed and reduce the power consumption of the TCAM search operation. For any application that requires a fast memory search, TCAM can provide a solution. The design of this architecture was implemented successfully on the Xilinx vivado FPGA. The sample design has been synthesized using Xilinx synthesizer and functionality of the design has been verified extensively by using Modelsim verification tool over a large set of test cases. This architecture works better than the existing system in terms of speed, power consumption and delay.

ISSN: 2233-7857 IJFGCN

The speed of this architecture is increased by using multiport SRAM in the place of single port SRAM of existing architecture and power consumption of TCAM is reduced to 15mW which is analyzed using the Xilinx power analyzer. The area utilization is more in the proposed architecture when compared to the existing REST architecture. This work can be further developed for designing the low power REST architecture with 512x32 multiport SRAM to increase the searching operation of TCAM for improving the address translation in the application of packet network routers for packet forwarding and packet classification. The power consumption, area and delay parameters of multiport system with the existing architecture can be analyzed.

REFERENCES

[1] Zhuo Qian, Martin Margala, "LowPower RAM-Based Hierarchical CAM on FPGA", International conference on Reconfigurable computing and FPGAs, vol. 38, Issue.15, pp. 554–558, Sep2014.
[2] SanghyeonBaeg,"Low-PowerTernary content-Addressable Memory Design Using a Segmented Match Line", IEEE transactions on circuits and systems, vol. 55, Issue.6, pp. 1485-1494,July 2008.
[3] WeirongJiang," scalable Ternary Content Addressable memory implementation using FPGA ", IEEE conference on Architectures for Networking and Communications Systems, vol. 55, pp. 71-82,2013.
[4] Zahid Ullah, Manish K. Jaiswal, "Z-TCAM: An SRAM-based Architecture for TCAM", IEEE transactions on very large scale integration systems, vol. 23, Issue. 2, pp. 402-406, Feb 2015.
[5] Zahid Ullah, Kim Ilgon,"Hybrid Partitioned SRAM-Based Ternary Content Addressable Memory", IEEE transactions on very large scale integration systems, vol. 59, Issue. 12, pp. 2969-2979, Dec2012.
[6] Zahid Ullah, Manish K. Jaiswal, "UE-TCAM: An Ultra Efficient SRAM-based TCAM", IEEE transactions on very large scale integration systems, vol. 17, Issue. 8, pp. 330–336, Sep2015.
[7] Zahid Ullah , Kim Ilgon ,"Hybrid Partitioned SRAM-Based Ternary Content Addressable Memory", IEEE transactions on very large scale integration systems, vol. 59, Issue. 12, pp. 2969-2979, Dec 2012.
[8] Telajala Venkata Mahendra, Sandeep Mishra, and Anup Dandapat, "Self-Controlled High-Performance Precharge-Free Content-Addressable Memory", IEEE transactions on very large scale integration systems, vol. 25,Issue. 8, pp. 2388-2392, Sep2017.
[9] Binu K. Mathew,Neethu Anna Issac,"Ternary Content Addressable Memory", International Journal of Recent Trends in engineering and Research", vol.2,issue 5, pp. 149-153,May2016.
[10] Yu-Chieh Cheng, Pi-Chung Wang, "Scalable Multi-match Packet Classification Using TCAM and SRAM", IEEE transactions on computers, vol. 65, Issue. 7, pp. 2257-2269, July 2016.
[11] Bo-Cheng Charles Lai, " Efficient Designs of Multiport Memory on FPGA", IEEE transactions on very large scale integration systems, vol. 25, Issue 1, pp. 139-150, Sep2017.
[12] Ali Ahmed, Kyungbae Park, and SanghyeonBaeg "Resource-Efficient SRAM-based Ternary Content Addressable Memory", IEEE transactions on very large scale integration systems, Vol 25,issue 2017.

ISSN: 2233-7857 IJFGCN

[13] S.Parkavi (1) And S.Bharath " Resource Efficient Multi Ported SRAM Based Ternary Content Addressable Memory", IOSR Journal of Engineering, , ISSN (e): 2250-3021, ISSN (p): 2278-8719 , PP 11-18,2018.

ISSN: 2233-7857 IJFGCN