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A Low Voltage Narrowband CMOS Low-Noise Amplifier for L-1 Band GPS RF Receivers

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Abstract

A minimal CMOS low clamor speaker for Global Positioning System collectors is top to bottom examined and proposed in this paper. The outlined speaker works at particular 1.575 GHz GPS L-1 band recurrence, in this way a restricted band intensifier configuration approach is favored. Proposed configuration includes CMOS inverter circuit, one-sided to work experiencing significant change locale of activity, to give high pick up at a specific recurrence. To achieve better switch detachment, cascode outline systems are utilized. Reproduced execution shows transconductance gain of 19.94 dB, 1.74 dB Noise Figure with soundness factor more noteworthy than solidarity. The near investigation demonstrates that the proposed intensifier has practically identical execution with accessible GPS beneficiary ICs, made utilizing distinctive procedures, for example, GaAs and BiCMOS. This is very critical since the proposed configuration is comprised of minimal effort MOS gadgets as it were.

Keywords: *CMOS Low noise amplifier, GPS, narrow-band, noise figure, S-parameters.*

1. Introduction

The worldwide situating framework/Global positioning system (GPS) gives time and area data which can be separated by clients with the assistance of GPS accepting gear. The GPS working frequencies are extending from the L1 band (1.575 GHz) to L5 band (1.17GHz), having particular applications in electronic interchanges. A normal engineering of GPS recipient is appeared in Figure 1.

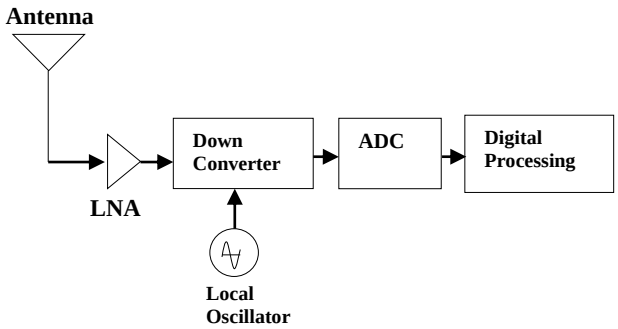

Figure 1: **Typical architecture of GPS receiver**

Flag quality gotten by GPS reception apparatus is little, running from few nano-volts to milli-volts. Consequently, a low noise amplifier(LNA), or, in other words first flag preparing square of beneficiary area, must have the capacity to raise flag level over the commotion floor. For better commotion execution, GPS

collector intensifiers are ideally comprised of GaAs or BiCMOS process advances. Be that as it may, these advances endure the disservice of higher expense due to included process complexities [1]. While, a CMOS innovation offer different focal points, for example, low power dissemination, less assembling expense and great pressing thickness. In such situation, the plan of reduced low commotion narrowband speaker utilizing CMOS innovation, having similar execution with enhancers planned utilizing different advances, is trying for simple originators, or, in other words issue tended to by this paper.

The utilization of more detached parts and transistors in circuit results in expanded silicon zone, clamor and power dissemination. It influences the reason for research i.e. outline for manufacturability. The proposed configuration uses not very many aloof segments and dynamic gadgets. This has added to all the more likely commotion execution of proposed LNA.

The schematic outline of proposed LNA is appeared in Figure 2. The cascode setup is picked because of its benefits of info coordinating, high increase, great clamor execution, low power utilization and high invert disengagement [2]. As outlined in [3], the static CMOS inverter has a genuinely high gain when one-sided to work in its progress locale of activity and can be utilized as a simple intensifier; As the proposed configuration is expected to work at correct 1.575GHz recurrence, CMOS inverter based plan approach is utilized in outline and recreation of LNA in Figure 2.

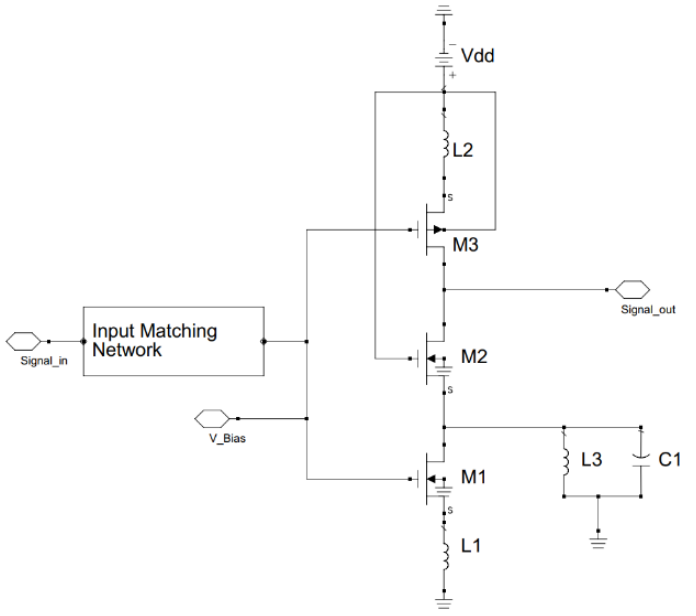

Figure 2: **Schematic of proposed CMOS LNA**

This paper shows a CMOS narrowband LNA for L1 band GPS collector which has tantamount clamor execution with monetarily accessible BiCMOS/GaAs based GPS L1 band enhancers [4-6] and preferred execution over alluded CMOS circuits [7-9].

2. DESIGN CONSIDERATIONS

Transistors M1 and M3 frame CMOS inverter, one-sided to work in the progress locale of task. The gain of an inverter-based speaker is genuinely high whenever one-sided at a convergence purpose of PMOS and NMOS on its dc trademark bend. High gain decreases clamor and in addition mutilations, or, in other words of GPS recipient enhancers. A cascode gain organize contains transistors M1 and M2 that outcome in better invert disconnection. The LC full circuit at the yield of M1 goes about as clamor trap to weaken commotion accordingly upgrading framework commotion figure. The linearization in resistive source degeneration method enhances the framework linearity, be that as it may, expands clamor and power scattering [12]. Along these lines, proposed LNA make utilization of source degeneration inductor L2 to limit commotion, enhance linearity and strength of an intensifier.

Appropriate narrowband impedance coordinating is vital in LNA plan. As the flag possesses a tight data transmission, we just need to give impedance coordinating and also enhancement in this thin transfer speed. This can be accomplished successfully by utilizing a guideline of reverberation. In the proposed plan, the responsive piece of the impedance is controlled and invalidated at the reverberation recurrence, leaving just the resistive part to be coordinated to the resistive source opposition. Since the enhancement factor is a result of the gadget transconductance and load impedance, when the heap impedance is controlled to top up by means of the reverberation procedure, the intensification factor crests up as a result[10]. In proposed LNA, LC tank circuit is utilized for this reason. Utilizing such circuit results of additional inductance, parasitic capacitances with the end goal to accomplish reverberation.

Appropriate narrowband impedance coordinating and low clamor enhancing at the info results in low commotion execution and results in the decrease in DC control by a significant sum. At the yield, a LC tank circuit is utilized to amplify the gain with the goal that we can discard the extra gain stage and make the circuit straightforward.

Albeit conventional cascode engineering is utilized in the proposed outline, the oddity lies in the cautious choice of transistor angle proportions and coordinating systems, utilization of cascode and source degeneration methods, utilization of LC full circuit for accomplishing wanted recurrence at ideal commotion figure. The game plan has brought about low clamor, thinking about CMOS innovation.

For investigating circuit impedances and an exchange capacity of transconductance organize, consider a small signal model of the speaker appeared in Figure 3.

In order to evaluate gain of transconductance stage, following equations are considered where Zout Total in(1) signifies total output impedance of transconductance stage.

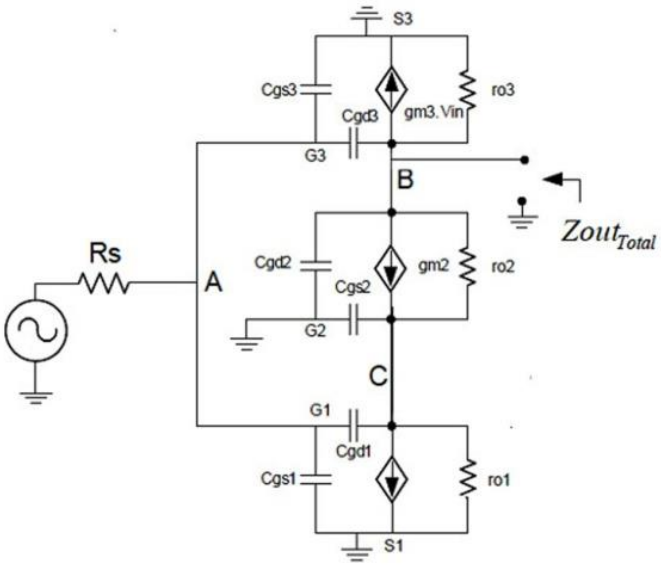

Figure 3: **Small signal model of transconductance stage**

$$Zout_{Total} = Zout_{M3} \| Zout_{Cascode} \quad (1)$$
$$= (gm_2 ro_2 ro_1 + ro_2 + ro_1) \| ro_3 \cong ro_3$$

The voltage gain of the circuit in Figure 3, is as expressed in equation (2).

$$A_V = -(g_{m\,cascode} + g_{m3}) Z_{OUT\,total} \quad (2)$$
$$\cong -(g_{m1} + g_{m3}) r_{03}$$

Equation (3) is resultant transfer function, where CA and CB indicate total capacitance at a node, at nodes A and B respectively in Figure 3.

$$A_{V_{Gm}}(jw) = \frac{V_B}{V_{in}} \quad (3)$$
$$= \frac{(g_{m3} + g_{m1}) r_{03}}{(1 + jwC_A R_S)(1 + jwC_B r_{03})}$$

Equation (3) signifies that the transfer function of circuit dependents upon transconductance of CMOS inverter stage.

For noise analysis of the transconductance stage, in order to make equations simple, the gate noise of MOSFET and parasitic capacitances are ignored and only channel noise is considered. This results in derived noise factor equations which are frequency independent and which gives relation with transconductance and the channel noise parameters. The noise factor for the source degenerated transistor is given by equation (4)

As a portion of split channel noise current of source node flows through the output gets subtracted from split channel noise current of drain node, the degeneration inductor suppresses some amount of the channel noise current of the transistor. A source degenerated NMOS transistor and simple noise model for a MOSFET is shown in Figure 4.

$$F = \frac{4kT\frac{\gamma_1}{\alpha_1} gm_1 \frac{(1/gm_1)^2}{(1/gm_1)^2 + (wL_s)^2}}{4kTR_s gm_1^2} \quad (4)$$

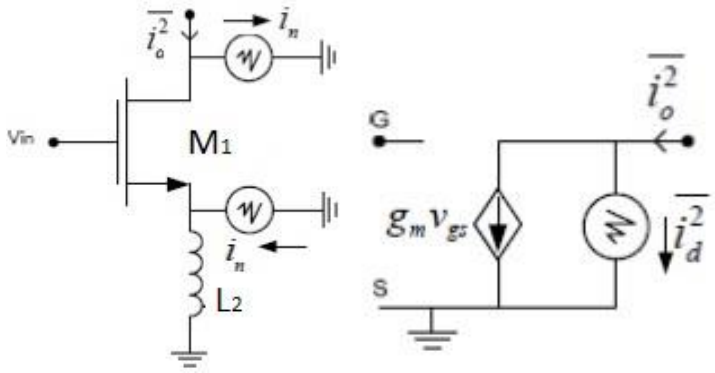

Figure 4: **A source degenerated NMOS transistor and simple noise model for a MOSFET**

In LNA circuits, higher the value of transconductance, lower is the value of noise factor. Theoretically, such situation can be achieved by increasing the bias current, decreasing the overdrive voltage and increasing width of transistors. But tradeoffs have to be made in designing the practical LNAs. Considering channel noise of the PMOS transistor, the equation (4) becomes

$$F = 1 + \frac{4kT\left(\frac{\gamma_1}{\alpha_1} g_{m1} \frac{\left(\frac{1}{g_{m1}}\right)^2}{(\frac{1}{g_{m1}})^2 + (wL_{ss})^2} + \frac{\gamma_2}{\alpha_2} g_{m3} \frac{\left(\frac{1}{g_{m3}}\right)^2}{(\frac{1}{g_{m3}})^2 + (wL_{ss})^2} + \frac{\gamma_f}{\propto_f} g_{mf}\right)}{4KTR_s(gm_1^2 + gm_3^2)} \quad (5)$$

It is evident from equation (5) that Noise figure of proposed LNA is inversely proportional to gain of inverter stage of an amplifier. This confirms the fact that higher gain of LNA results in lower noise figure. The noise figure of proposed LNA depends upon the selection of passive circuit components, particularly L4 & L1 in Figure 2. The experimental analysis indicates that overall noise figure increases if we increase the value of inductor L2 and decrease the value of L4, around its optimum value.

Since inductors size is main concern for Si chip area, thus size of passive components should be chosen of minimum value [11]. Design constraints considered for circuit components are 60 ≤ W1 ≤ 100 [μm] for transistor width; 0.1 ≤ L ≤ 5 [nH] for inductors and 1 ≤ C ≤ 5 [pF] for capacitors used. The technology parameter based constants are: Cox (fF/μm2)= 8.632, Rs=50 Ω, RL= 50 Ω, f0 = 1.575 GHz, γ=2.5, L (μm)= 0.18, Vth = .51, Vdd = 1.8 V. The

transistor aspect ratios (W/L ratio in µm) are: M1=26/0.18, M2=47/0.18 and M3=60/0.18.

3. Simulation result

The target performance parameters of the L1 band GPS receiver LNA are listed in table 1 below.

Table I. L1 band GPS receiver LNA target performance parameters

GPS L1 receiver LNA parameters	**Unit**	**Typical**
Operating frequency	GHz	1.575±1.024MHz
IIP3 at 1.575 GHz	dBm	≥1 dBm
1dB compression point	dBm	≥- 6 dBm
S11 Input return loss	dB	Better than 10-dB
S22 Output return loss	dB	Better than 11-dB
S21 Forward Power Gain	dB	≥14
Stability	-	k>1
Noise figure	dB	≤1.5 dB

The aspect ratios for PMOS and NMOS transistors are obtained mathematically by using (5) and (6) respectively.

$$I_{Pmos} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(Vgs - Vt)^2 \quad (5)$$

$$I_{Nmos} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(Vgs - Vt)^2 \quad (6)$$

S-parameter analysis is used in RF and microwave circuits to represent reflection functions of the travelling wave in multiport networks. The circuit is recreated utilizing 180nm innovation and reproduced forward gain is around 19.94 dB at 1.575GHz recurrence, as appeared in Figure 5. The arrival misfortunes at info and yield are - 15.62 dB and - 7.19 dB individually, which demonstrate satisfactory coordinating over the coveted recurrence go. Utilization of source degeneration system, legitimate info coordinating system and LC thunderous device at transistor M1 results in better clamor execution when contrasted with alluded plans, showed in Figure 6. A littler estimation of reflection coefficients adds to steadiness improvement of LNA, or, in other words 1.575GHz recurrence.

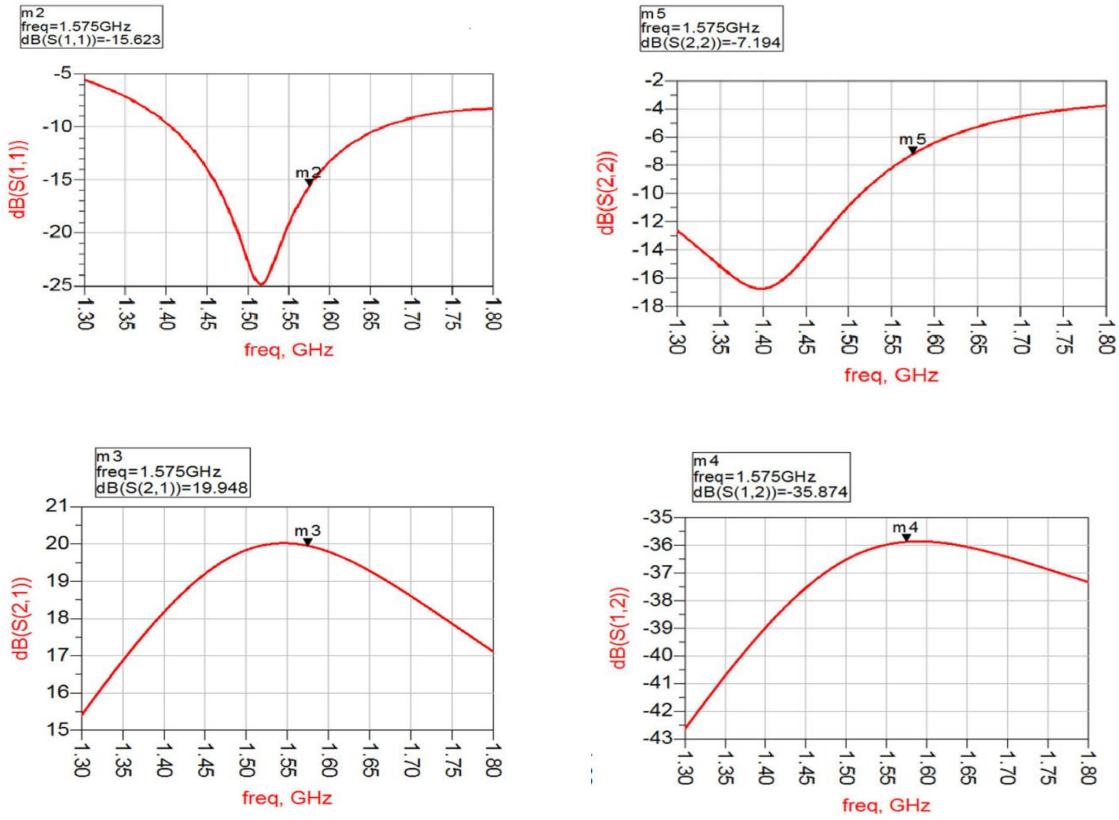

Figure 5. S-parameter analysis

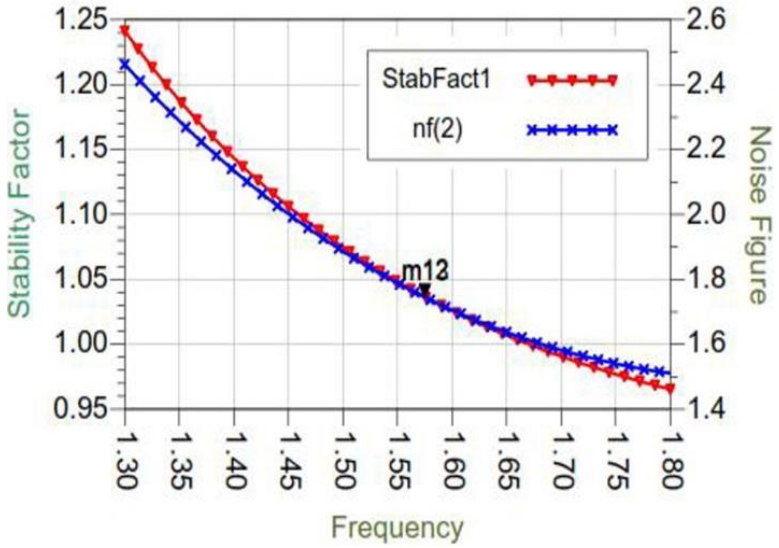

Figure 6: Noise Figure & stability analysis

Stability Factor (K) is validated mathematically using S- parameter analysis and Stren's stability equation (7).

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 \cdot |S_{21}| \cdot |S_{12}|} \qquad (7)$$

For unconditional Stability, K should be greater than 1 (K>1). As the calculation indicates K>1, proposed LNA is unconditionally stable. The validation of LNA designed is realized using the Agilent's ADS software suite. The performance has been verified at all four process corners in addition to the typical case at different temperature ranges. The corner analysis of noise and stability of proposed design is indicated in Table II.

TABLE II. STABILITY AND NOISE FIGURE CORNER ANALYSIS

PARAMETER	TYPICAL 25^0C	SF 0^0C	SF 100^0C	FS 0^0C	FS 100^0C	SS 0^0C	SS 100^0C	FF 0^0C	FF 100^0C
STABILITY	1.64	5.25	5.06	0.92	1.27	21.28	19.7	0.938	0.918
NOISE FIGURE	1.78	2.31	3.13	1.44	1.97	3.31	3.6	1.83	2.52

Process corners speak to the furthest points of manufacture parameters varieties at which the circuit capacities effectively. As demonstrated in Table II, the proposed configuration works at all procedure limits and in this manner it tends to be closed to have satisfactory plan edges from the clamor and dependability point of view.

Table III demonstrates execution examination of proposed plan with audited writing while Table IV shows execution correlation with L1 band GPS beneficiary speaker ICs. To the best of my insight, this paper speaks to the best clamor execution among the alluded CMOS LNA papers for L1 band GPS beneficiaries. The sole reason for Table IV is to underscore the tantamount execution of proposed LNA with business GPS beneficiary LNAs, which are made utilizing distinctive process innovations, for example, GaAs and BiCMOS.

TABLE III. PERFORMANCE COMPARISONWITH REVIEWED LITERATURE[14].

Parameters	This Work	[8]	[9]	[10]	[13]
Frequency (GHz)	1.575	1.57	1.57	1.57	1.15 -1.6
Technology(μm)	0.18	0.18	0.18	0.18	0.13
Power Supply(Volts)	1.8	1.8	1.8	0.7	1.2
Power Gain (S21) (dB)	19.94	18.75	14	17	
Input Return Loss (S11)(dB)	-15.62	-10.4	-10	-8	<10
Reverse isolation(S12)(dB)	-35.87	-	-	-	
Noise figure(dB)	1.74	2.52	3.2	4.2	<7

TABLE IV. PERFORMANCE COMPARISON WITH GPS RECEIVER ICS

Parameter	This Work	[5]	[6]	[7]
Technology	CMOS	BiCMOS	GaAs	-
Gain (dB)	19.94	20.5	14	16

NF[a](dB)	1.74	0.8	1.55to 1.95	1.56 to 2
Typical V_{DC}	1.8 V	2.85V	3.6V	1.8V
1 dB CP[b]	-10 dBm	-12 dBm	-6 dBm	-13 dBm
S11 (dB)	-15.62	-10	-7.5	11
S22(dB)	-7.19	-10	-14	- 35
S12(dB)	-35.87	-32	-24	-
Stability	1.037	-	-	>1

A: NOISE FIGURE B: COMPRESSION POINT

4. Conclusion

A novel plan of reduced 1.575 GHz CMOS LNA for GPS L1 band RF recipients is illustrated. Reproduction result shows transconductance gain of 19.94 dB, soundness factor of 1.03, sufficient info and yield reflection coefficients with empowering 1.74 dB Noise Figure, considering 0.18 µm CMOS process innovation. Similar examination demonstrates that proposed LNA has preferred clamor execution over looked into writing while relatively indistinguishable execution with accessible GPS beneficiary ICs which are comprised of unexpected procedures in comparison to CMOS. This is very critical since the LNA in Figure 1 is comprised of just MOS gadgets. Accordingly, LNA proposed in this paper may profit the significant calling regarding its minimization and cost-viability.

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